Multidimensional Nano Heat Conduction in Cylindrical Transistors

Mohamed Fadhel Ben Aissa, Faouzi Nasri, and Hafedh Belmabrouk

***Abstract*— A 3-D non-Fourier heat conduction in a cylindrical surrounding-gate (SG) MOSFET including phonon-wall collisions effects has been developed and presented. The obtained results are verified with the existent data. The various thermal characteristics of the device are obtained from the solution of the dual-phase-lag model coupled with a 3-D second-order temperature jump boundary condition. We find that, when the Fourier law ceases to be valid, the presented model is able to predict the nano heat transfer in cylindrical devices. After switching off the device, we show that the temperature is more thermally stable then that given in MOSFET and tri-gate silicon on insulator-MOSFET. We show also that the radius of the cylindrical SG drastically changes the temperature and heat flux distributions within the transistor devices.**

***Index Terms*— Cylindrical surrounding-gate (SG) MOSFET, dual-phase-lag (DPL) model, nano conduction, second-order jump temperature.**

I. Introduction

THE reduction in device size has led to several problems such as thermal problem [1]. One of the challenges for 3-D integrated circuit is the self-heating inherent to 3-D transistors [2]. Multigate transistors such as tri-gate and cylindrical surrounding-gate (SG) MOSFET [3], [4] are feasible solutions to the heat generation problem. A 3-D nano thermal study is recommended to investigate the thermal stability in those devices, especially in a cylindrical SG MOSFET. Double-Gate MOSFET, tri-gate MOSFET, and cylindrical SG MOSFET are the best architecture to reduce the self-heating problem [5].

Many works have treated the electrical part of the cylindrical SG MOSFET. Kumar *et al.* [6] have used an analytical model in a cylindrical gate all around MOSFET and found that the high-k material is very useful for the design and optimization for high current and improved the device performance. Xu *et al.* [7] have developed a quasi-analytical model to predict the current–voltage characteristics of a cylindrical SG nanowire MOSFET. They found that reasonable agreements with numerical simulations were achieved for nanowires with various radius and orientations.

To better explain the performance of these devices, it is required to investigate their thermal stability. From macro to nanoscale regime, many works have studied the classical thermal stability of electronic devices [8], [9]. In nanoscale regime and when the Fourier law ceases to be valid, many works have investigated heat conduction based on non-Fourier law [10], [11]. The phonon Boltzmann equation (BTE) is the famous equation to describe the heat transfer process due to phonon transport from macro to nanoscale regime [1], [12]. Cattaneo [13] and Vernotte [14] proposed a thermal wave model (Cattaneo-Vertnotte wave model). However, this model describes only a microscopic response in time. Another theory was proposed by Tzou [15], [16] about the dual-phase-lag (DPL) model. This model proves that the heat flux precedes the temperature gradient. Liu and Wang [17] investigate the thermal damage for a laser irradiated tissue. They used the 1-D DPL model of heat transfer in Cartesian coordinates with convective heat loss and internal heat generation. Nasri *et al.* [18], [19] used the 2-D DPL model in Cartesian coordinates to investigate the temperature distribution in a 2-D MOSFET. Ho *et al.* [11] analyzed the heat conduction problem in a two-layered structure using lattice Boltzmann method in Cartesian coordinates. In a previous work [20], we investigate the phonon transport in a tri-gate silicon on insulator (SOI) MOSFET using the single phase lag model coupled with the temperature jump boundary condition. We found that the proposed model is able to predict the nano heat conduction in a tri-gate SOI MOSFET. Torabi and Saedodin [21] have numerically investigated the DPL model in cylindrical coordinates system. Nevertheless, 3-D numerical investigation of the DPL model coupled with a temperature jump boundary condition in cylindrical coordinates applied to a nano cylindrical SG MOSFET has not been considered in the literature. The aim of this paper is to investigate the ability of the 3-D DPL model coupled with temperature jump boundary condition to predict the phonon transport in a cylindrical 3-D SG-MOSFET in cylindrical coordinate system.

II. Device Architecture

The SG MOSFET presents the best possible control of gate region and consequently the best possible electrostatic

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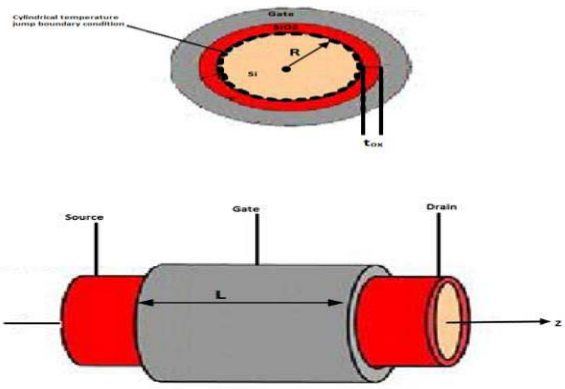

Fig. 1. (a) Cross-sectional view coordinate system of the surrounding-gate MOSFET. The gate length and radius of the silicon body are given by L and R, respectively. t_{ox} represents the thickness of gate oxide. (b) Schematic view of the 3D surrounding-gate MOSFET structure.

integrity. In this survey, we test the capability of the DPL model in a 3-D cylindrical surrounding MOSFET compared to the tri-gate devices. Also in this paper, we investigate thermal stability of a SG MOSFET given in Fig. 1(a) and (b) compared to tri-gate SOI-MOSFET.

Fig. 1(a) and (b) shows the geometry and a cross-sectional view of a 3-D SG MOSFET, respectively.

III. Mathematical Model

DPL model in a cylindrical coordinate especially in a cylindrical transistor is given by

$$\tau_q \frac{\partial q(r,z,t)}{\partial t} + q(r,z,t) = -\lambda\left(\frac{\partial T(r,z,t)}{\partial r} + \frac{\partial T(r,z,t)}{\partial z}\right) - \lambda\tau_T \frac{\partial}{\partial t}\left(\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2}\right). \quad (1)$$

τ_q is the phase lag of the heat flux and τ_T is the phase lag of the temperature gradient. r is the radial coordinate ($0 \le r \le R$), R is the radius of the transistor, Z is the longitudinal coordinate, T is the temperature, λ is the heat conductivity, and q is the heat flux.

τ_T and τ_q were introduced to take into account the effect of the phonon speed propagation, thereafter to describe the effect and the cause of the temperature raising. After combination of (1) with the balance equation [22], we obtain the DPL model in cylindrical coordinate

$$\frac{1}{\alpha}\frac{\partial T}{\partial t} + \tau_q \frac{1}{\alpha}\frac{\partial^2 T}{\partial t^2} = \frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2} + \alpha Q + \tau_T \frac{\partial}{\partial t}\left(\frac{\partial^2 T}{\partial r^2} + \frac{1}{r}\frac{\partial T}{\partial r} + \frac{\partial^2 T}{\partial z^2}\right) \quad (2)$$

where α is the thermal diffusivity and Q is the volumetric heat generation rate.

In order to simplify the numerical simulation, we normalize the DPL model and we use the following dimensionless variables [19]:

$$T^* = \frac{T - T_0}{T_0}, \quad t^* = \frac{t}{\tau_q}, \quad Kn = \frac{\Lambda}{L}, \quad z^* = \frac{z}{L}$$
$$B = \frac{\tau_t}{\tau_q}, \quad r^* = \frac{r}{R}$$

where Λ is the phonon mean free path, L is the channel length, and Kn is the Knudsen number.

The DPL model in the dimensionless form can be rewritten as

$$\frac{\partial T}{\partial t} + \frac{\partial^2 T}{\partial t^2} = \frac{1}{R^2}\frac{\partial^2 T}{\partial r^2} + \frac{1}{R^2 r}\frac{\partial T}{\partial r} + \frac{1}{L^2}\frac{\partial^2 T}{\partial z^2} + Q + B\Lambda^2 \frac{\partial}{\partial t} \times \left(\frac{1}{R^2}\frac{\partial^2 T}{\partial r^2} + \frac{1}{R^2 r}\frac{\partial T}{\partial r} + \frac{1}{L^2}\frac{\partial^2 T}{\partial z^2}\right). \quad (3)$$

IV. Initial and Boundary Conditions

The cylindrical transistor is considered to be initially at the ambient temperature (300 K). Hence, the initial conditions are

$$\frac{\partial T(r,z,0)}{\partial t} = 0, \quad T(r,z,0) = 300 \text{ K}.$$

In order to compare the thermal stability of the two types of transistors, we simulate the cylindrical SG MOSFET on the same conditions that used in a previous work [20]. The drain and the source sides are assumed to be adiabatic; the ending part of the source and the drain are exposed to the ambient.

The important boundary condition in this paper is located on the oxide semiconductor interface, this condition expressed as

$$T - T_w = -d_1 Kn \nabla_n T + d_2 \frac{Kn^2}{2}\Delta T \quad (4)$$

where Kn is the Knudsen number, and d_1 and d_2 are an adjustable coefficient [23]. In this paper, we suppose that there is no temperature diffusion due to phonon-wall collisions ($d_2 = 0$).

To calculate the parameter d_1 we propose the following method:

Gad-el-Hak gave an expression to the temperature jump boundary condition [24]

$$T_s - T_w = \frac{2\beta}{\beta+1}\frac{2-\sigma_T}{\sigma_T}\frac{\Lambda}{\text{Pr}}\left.\frac{dT}{dy}\right|_{\text{wall}} \quad (5)$$

where T_s is the system temperature and T_w is the wall temperature, σ_T is the thermal accommodation coefficient, β is the ratio of specific heats, Λ is the MFP, and Pr is the gas (phonon) Prandtl number.

The dimensional temperature jump boundary condition given by [23]

$$T_S - T_w = -d_1 \cdot Kn \cdot L_c \cdot \left.\frac{dT}{dy}\right|_{\text{wall}}. \quad (6)$$

The phonon temperature gradient is equal to the wall temperature gradient [25]

$$\frac{dT}{dy} = \frac{dT_w}{dy} = \frac{dT_s}{dy} \quad (7)$$

where T_s represents the system temperature and T_w represents the wall temperature.

At the oxide semiconductor interface, the constant heat flux is assumed at the wall by [26]

$$q_w = \lambda \left.\frac{\partial T}{\partial y}\right|_{\text{wall}}. \quad (8)$$

We note also that the temperature jump condition given by [27]

$$\Delta T_{\text{Jump}} = R_{\text{Jump}} * q \quad (9)$$

where R_{Jump} is the thermal boundary resistance defined as the resistance at the phonon (gas)-solid interface [28] then at the Si-SiO_2 interface.

The temperature jump is given by

$$\Delta T_{\text{Jump}} = -R_{\text{Jump}} * \kappa_{\text{eff}} * \frac{\partial T}{\partial y} = -R_{\text{Si-SiO}_2} * \kappa_{\text{eff}} * \frac{\partial T}{\partial y} \quad (10)$$

where κ_{eff} is the effective thermal conductivity.

Combining (10) with (6), the adjustable coefficient d_1 given by

$$d_1 = \frac{R_{\text{Si-SiO}_2} * \kappa_{\text{eff}}}{Kn * L_c}.$$

For the Si-SiO_2 interface [29]

$$R_{\text{Si-SiO}_2} = 0.503 * 10^{-9}\ \text{m}^2\text{K/W}$$
$$\kappa_{\text{eff}} = \frac{\kappa_{\text{bulk}}}{(1 + 4 * Kn)}.$$

For $L_c = 30$ nm, $Kn = 3.33$, $\kappa_{\text{eff}} = 10.46\ \text{Wm}^{-1}\text{k}^{-1}$, and $d_1 = 0.0526$.

The first-order temperature jump boundary condition is used to predict phonon-wall collisions in the transistor. During the phonon-wall collisions in a classical MOSFET, phonons are assumed to be absorbed at the oxide/semiconductor interface. On the other hand, the phonons are not fully absorbed after phonon-wall collisions process in a cylindrical SG MOSFET, a part of them is reflected on the interface and propagate into the cylindrical channel region.

V. Numerical Method

The proposed nonlinear model is solved using the finite-element method [30]. Equations (3) and (5) are coupled with initial and boundary conditions. A triangular mesh is given in Fig. 2. We note that in the channel region, the oxide-semiconductor interface is refined with a finer mesh and a higher number of elements.

Fig. 2 shows the temporal temperature evolution of 20-nm SG MOSFET for different meshes. In order to verify that the convergence has been reached and the computed results are independent of the mesh size, we have tested many mesh cases, namely, 17 000, 19 000, 33 000, and 35 000 elements. The nonuniform mesh used in this paper contains 35 000 triangular elements. To better explain the phonon-wall collisions, the oxide-semiconductor interface contains 12 000 boundary elements and all other boundary contains 1056 quadrilateral elements.

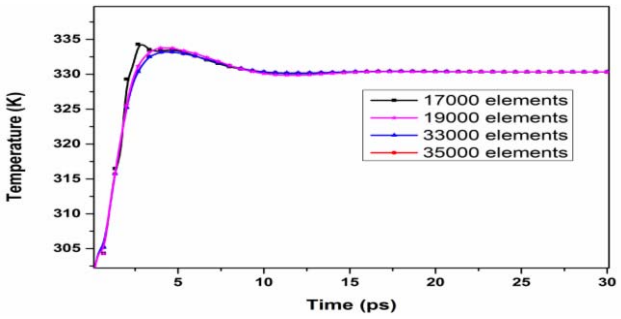

Fig. 2. Temporal temperature evolution of 20-nm SG MOSFET for several meshes.

TABLE I
THERMAL PROPERTIES OF Si AND SiO_2 MATERIALS

Symbol	V (m/s)	Λ (nm)
Si	3000	100
SiO2	5900	0.4

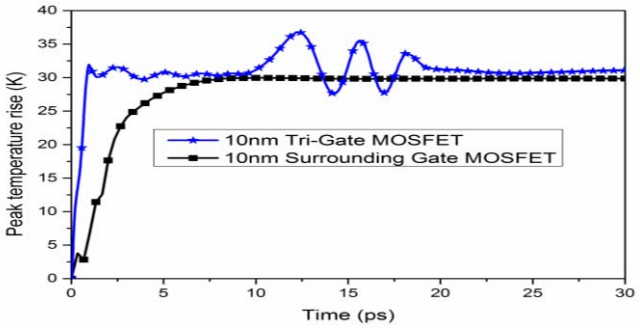

Fig. 3. Comparison of the temporal temperature distribution in the centerline of the transistor with 2-D BTE and 3-D tri-gate MOSFET.

VI. Results and Discussion

The goal of this paper is to investigate phonon transport in SG MOSFET and to demonstrate the important role of the radius of the transistor for the phonon transport. The materials involved in the investigated structures are silicon and silicon dioxide. The thermal properties of these materials are listed in Table I [1], [31].

In order to verify the validity of the proposed model, the results are compared to a tri-gate MOSFET.

Fig. 3 illustrates the temporal temperature distribution in the centerline of the transistor for 3-D tri-gate MOSFET and the 3-D SG MOSFET predicted by the DPL model. As shown in Fig. 3, the temperature rise is more rapid for 3-D tri-gate MOSFET. Using the DPL model, the temperature has an oscillating variation between zero and 23 ps for the tri-gate MOSEFT. On the other hand, the temperature predicted in the SG MOSFET achieved the saturation after 10 ps.

A. Channel Length Effects

Fig. 4 shows the effect of the length of the channel on the temperature in the centerline. The temperature tends to the

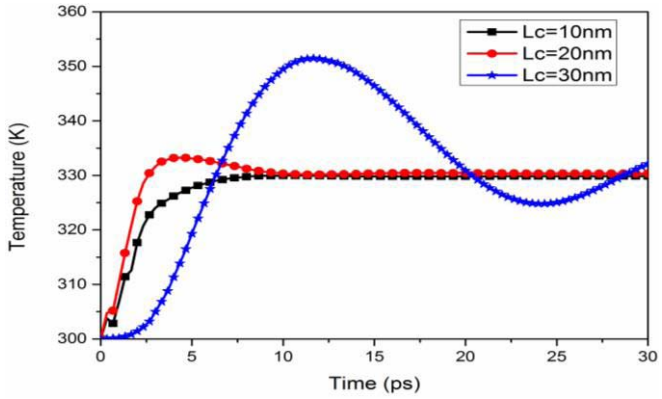

Fig. 4. Comparison of the temporal temperature profile in the centerline of the transistor with variation of the channel length L_C.

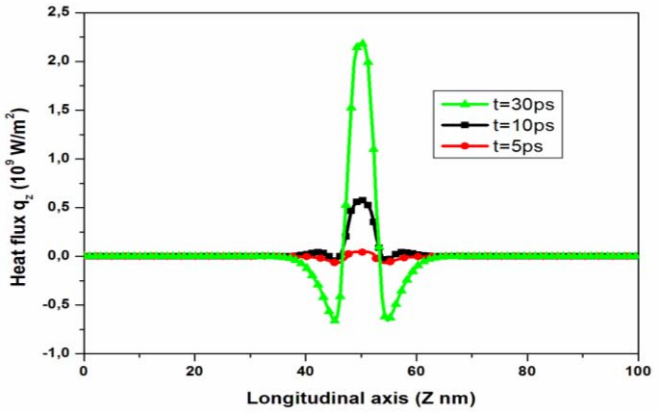

Fig. 6. Comparison of the longitudinal heat flux profile in the centerline of the transistor at different times.

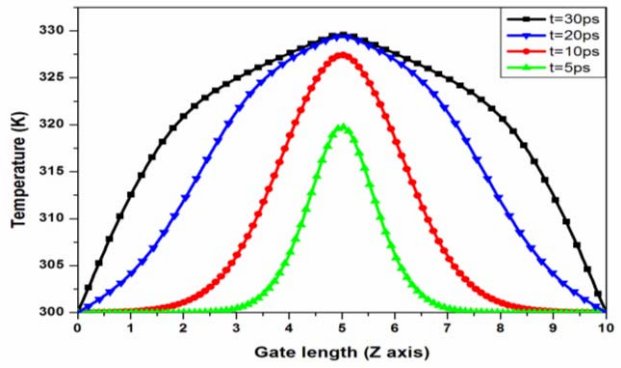

Fig. 5. Temperature profile versus longitudinal axis (Z) at different times.

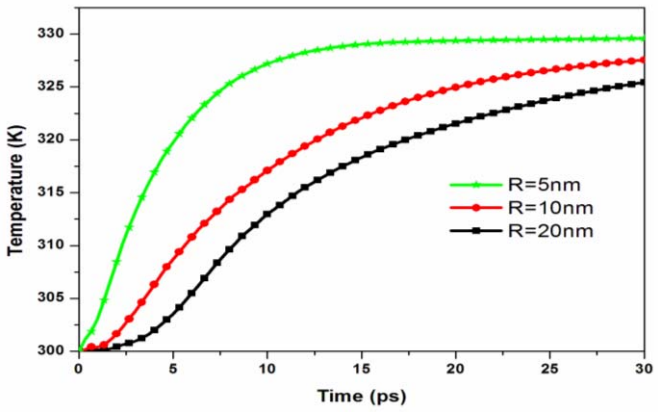

Fig. 7. Comparison of the temperature profile in the centerline with variation of radius of the transistor.

same threshold of 330 K for $L_c = 10$ and 20 nm. However, for 10 nm, the temperature rises regularly to the threshold within a period of 7 ps. For $L_c = 20$ nm, a temperature pick is observed at 4 ps. For $L_c = 30$ nm, we show that the temperature oscillates with an important magnitude and tends slowly to the saturation.

From Fig. 4, we can conclude that the channel length have an important role on the temperature variation of the SG MOSFET.

Fig. 5 shows the temperature variation versus the gate length at different time. It is clear that temperature have a maximum value in the middle of the channel, this position of the maximum caused by the phonon variation that focuses amidst the active region. We note also, that when the time increases, there is an increasing of the area affected by the temperature. For example, only 2 nm of the active zone is affected by the temperature at $t = 5$ ps, while, the entire active zone is affected at $t = 30$ ps.

Fig. 6 exhibits the heat flux in the centerline of the transistor along the longitudinal axis for different times. It is clear that, for different times, the heat flux is maximal in the active zone (caused by the volumetric heat source that existed only in the active zone) and decreases until it vanishes when we move away to the drain and source sides. We show that for $t = 5$ ps the heat flux q_z achieved 10^8 W/m^2; on the other hand, it achieved $2 \cdot 10^8$ W/m^2 for $t = 30$ ps.

B. Radius Effects

In this part, we investigate the role of the radius of the heat zone for the increasing of the temperature and the heat flux distribution.

Fig. 7 shows the comparison of the temporal temperature distribution in the centerline of the transistor for a radius value of 5, 10, and 15 nm. The channel length considered is 10 nm. Fig. 7 shows that the temperature reached the saturation only for a 5 nm of radius. We show also that when the radius decreases, the temperature increases slightly and keeps the saturations. This trend is explained by the rise of the thermal inertia due to the rise of the mass and the dimensions of the transistor when the radius is extended.

Fig. 8 shows the peak temperature rise within the transistor at 30 ps for a diameter value of 10, 20, and 30 nm. From Fig. 8, the temperature peak is higher for lower radius because the heat is trapped in smaller volume. We also observe that the temperature is almost constant in the channel region for lower radius and has a parabolic shape for a 20 and 30 nm of diameter.

Fig. 9 represents a comparison of the heat flux profile for different radii at 30 ps. The heat flux increases exponentially from the middle to the outside of the transistor. We note also that when the volume of the active region is higher the heat

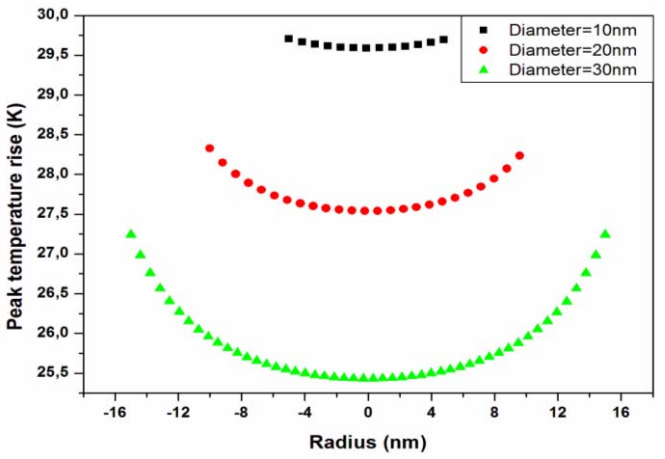

Fig. 8. Peak temperature rise versus diameter of the cylindrical surrounding MOSFET at 30 ps.

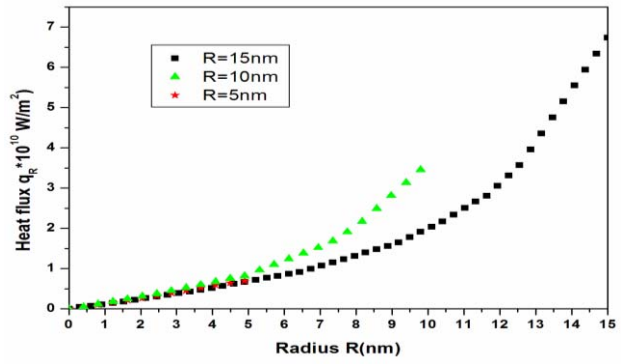

Fig. 9. Comparison of the heat flux profile in the centerline of the transistor at $t = 30$ ps with different radii.

flux increases and achieved $7 \cdot 10^{10}$ and 10^{10} W/m^2 for a radius of 15 and 5 nm, respectively.

VII. Conclusion

The non-Fourier heat conduction in SG MOSFET has been studied by using the DPL model coupled with a temperature jump boundary condition in cylindrical coordinates. Using the finite-element method, the temperature field within the heat flux distribution was obtained. It is deduced that, transistor form (tri-gate or SG), may make a difference in the shape and the amplitude of temperature and heat flux distributions. In addition, it was observed that the radius and the channel length of the cylindrical transistor have an important role for the stability and the increasing of the temperature. According to our study, we can conclude that the stability of SG MOSFET is optimal for 5 nm of radius and a 10 nm of channel length.

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