A 1-V 8-Bit 0.95μW Successive Approximation ADC for Biosignal Acquisition Systems

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***Abstract* — In this paper, a 1-V 8-bit 10 kS/s successive approximation (SA) analog-to-digital converter (ADC) with ultra-low power characteristic is implemented for biosignal acquisition systems. To decrease power consumption, a passive sample-and-hold (SH) circuit and an opamp-free, capacitor-based digital-to-analog converter (DAC) are utilized. The only active circuit, a comparator, is implemented in the sub-threshold region to preserve the required bias current. According to the measured results, the ADC has a signal-to-noise distortion ratio (SNDR) of 45.2 dB, and peak spurious free dynamic range (SFDR) of 54 dB for a 1 kHz 500 mV_{pp} input sine wave. The effective number of bits (ENOB) is 7.2. Its differential nonlinearity (DNL) and integral nonlinearity (INL) are -0.41/+0.38 and -0.89/+0.6 LSB, respectively. The total power consumption is 950 nW, and the figure of merit (FOM) is 3230 fJ/conversion-step. The active area, which is 0.93 x 0.93 mm^2, is determined by using TSMC 0.18μm 1P6M CMOS process.**

I. INTRODUCTION

Analog-to-digital converters (ADCs) are required for interfacing analog signals with digital circuits in various mix-signal systems to maximize the advantages of digital signal processing. Thanks to rapid developments in integrated circuit (IC) technology, increased numbers of ADCs are being integrated with complex digital circuitry on a single chip, such as biosystems [1], [2]. In such systems on chips (SOCs), the requirements for energy consumption are particularly stringent because majority of these systems are portable devices. The power consumption must remain as low as possible for long-term use. Since the ADC is the key component in this system, an energy-efficient ADC is necessary for the applications.

Among the existing ADC architecture, successive approximation (SA) ADC is widely known for processing accurate and medium-speed conversion. Compared with other types of ADC, the SA ADC's structure is not complicated, and only one comparator is required for data conversion. By nature, SA ADC is preferred for biomedical applications because of its low power consumption [3].

To decrease the SA ADC's power consumption further, the sub-threshold technique is adopted in this paper [4]. However, though the low-power characteristic guarantees long-term use, it constrains the circuits' performance, including required speed and signal-to-noise ratio (SNR). Fortunately, the biosignals are low-frequency by nature. The required specifications are not as strict in such biomedical systems. Hence, the degraded performance due to the low-power design considerations for analog circuits is not a critical point for the proposed SA ADC design.

By merely focusing on the low power consumption issue, a passive sample-and-hold (S/H) circuit and an opamp-free, capacitor-based DAC are utilized in the presented SA ADC architecture, along with simple digital logic circuits and a switching network to execute the search algorithm. The single active circuit is the comparator. Hence, the power consumption can be kept as low as possible.

This paper is organized as follows: Section II presents the biosignal physical characteristics, and describes the circuit design and implementation of the SA ADC in detail; Section III presents the measurement results; Finally, Section IV briefly concludes this paper.

II. DESIGN OF SA ADC

Table 1 summarizes the characteristics of a number of common physical signals [5]. The biosignals' bandwidth is usually below 10 kHz, thus an ADC with high operation speed is not required. On the other hand, biosignals are, by nature, variable amplitude waveforms that occur in an exceedingly noisy environment, the demanded resolution of the ADC with analog filter in such a biosignal processing system is usually only between 8 to 10 bits. In this paper, a low-power SA ADC with 8-bit resolution and 10-kHz sampling frequency is designed to meet the biosignal processing requirement.

The basic architecture of an SA ADC is illustrated in Fig. 1. The converter consists of an S/H circuit, a comparator, a successive approximation register (SAR) controller, and an 8-bit DAC. Using a binary searching algorithm, the input sample voltage can be successively approximated by the DAC output voltage.

For an N-bit SA ADC, N cycles are required to convert the analog signals into digital codes. Obviously, the DAC dominates the accuracy and the speed of the SA ADC. To conform to the system specification, a low-power, opamp-free, capacitor-based DAC with 80 kHz sampling rate is implemented. The sub-circuit design of the SA ADC will be described in the following subsections in detail later.

TABLE I. CHARACTERISTICS OF THE COMMON PHYSICAL SIGNALS

Parameter	Amplitude	Frequency (Hz)
Electrocardiography (ECG)	0.5~4mV	0.01~250
Electroencephalography (EEG)	5~300μV	dc~150
Electromyography (EMG)	0.1~5mV	dc~10,000
Electroneurography (ENG)	0~100μV	250~5,000

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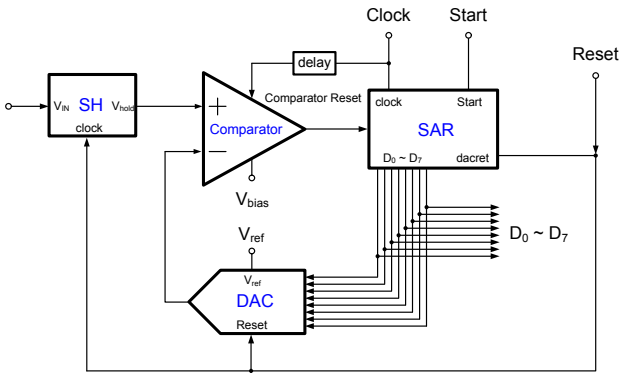

Fig. 1. Block diagram of a successive approximation ADC.

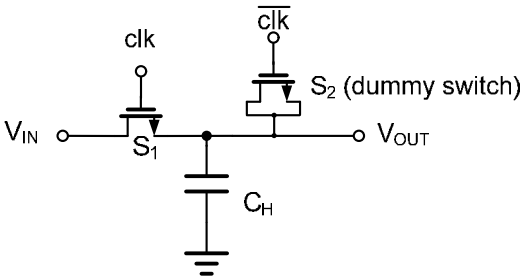

Fig. 2. Passive S/H circuit with dummy switch.

A. S/H circuit

To decrease the SA ADC's power consumption, a passive S/H circuit illustrated in Fig. 2 is adopted. It consists of the NMOS switch S_1 and the sampling capacitor C_H. A dummy switch S_2 is adopted to circumvent the problem of the charge injection and the clock feedthrough, and to compensate for the charge error. It will meet the accuracy requirements for 8-bit resolution.

B. Comparator circuit

The comparator used in the SA ADC is illustrated in Fig. 3; it is a track-and-latch stage. Because the comparator's accuracy plays a critical role in the SAR ADC, the transistors M_{s1} and M_{s2} are included to avoid hysteresis or delayed response on resetting phase. The operational principle is as follows. When the clock is high, the comparator is operated in the resetting mode and both outputs (V_{OUT+} and V_{OUT-}) are pulled to V_{DD} (high). On the other hand, when the clock is low, the circuit will execute the comparison of differential input, and the outputs level (V_{OUT+} or V_{OUT-}) of the comparator will depend on the difference between V_{IN+} and V_{IN-}.

The design of the bias current I_b is critical for the performance of the comparator, including speed, noise, and power consumption. For speed considerations, the frequency response of the comparator depending on the dominant pole should be analyzed. The dominated pole of the comparator is located at node P and can be described as follows:

$$\omega_P = \frac{g_{m1}}{C_P} \quad , \quad C_P = C_{gs3} + C_{db2} + C_{db4} + C_{db\_s2} + C_{buffer} \qquad (1)$$

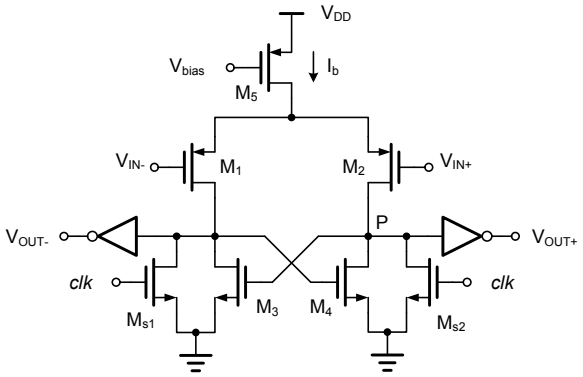

Fig. 3. Comparator circuit.

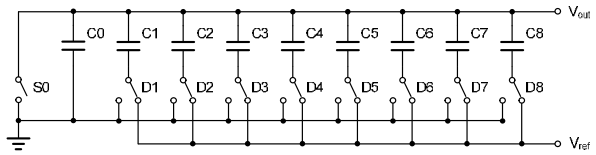

Fig. 4. Architecture of an 8-bit capacitor-based DAC.

where C_p is the total capacitance at node P. To fit the 10 kS/s sampling rate of the 8-bit SA ADC, the speed of the comparator must be operated at no less than 80 kHz. However, for settling within the 0.1% accuracy, the required unity-gain bandwidth of the comparator must satisfy seven times its time-constant. Therefore, a comparator with the unity-gain bandwidth of 1 MHz is implemented. Hence, the comparing time of less than 1 μs can be achieved.

Since the comparator's operational speed is at a low frequency, flicker noise will dominate the input-referred noise. Hence, a low bias current with large channel width is appropriate to decrease power consumption. In this paper, a bias current with only 400 nA is adopted to let the comparator be operated in sub-threshold region under the 8-bit and 10-kHz requirement.

C. Capacitor-based DAC

There are various structures, including resistor string, current-mode approach, and capacitor array, which can be adopted to implement the internal DAC in the SA ADC. Among these, the capacitor-array structure is most suitable for the low-power approach [6]. Therefore, in this paper, an opamp-free, capacitor-based approach as shown in Fig. 4 is used to implement the DAC. Based on the binary-weighted capacitor array, the output voltage of the DAC can be described as follows:

$$V_{out} = V_{ref} \frac{C_i + \sum_{j=i+1}^{8} D_j C_j}{C_{total}} \qquad (2)$$

where C_{total} is the total capacitance of the DAC, and the value of i is from 0 to 7.

The power source of the abovementioned passive capacitor array is dominated by the reference voltage, V_{ref}. It can be analyzed by calculating the required charge of all the capacitors during charging and discharging periods [6]. A relative equation described below can be used to estimate the power:

$$P_{Vref} = \frac{f_{clk}}{9} 2^8 C_0 \left(\frac{5}{6} {V_{DD}}^2 - \frac{1}{2} {V_{in}}^2 \right) \quad (3)$$

where f_{clk} is the operational frequency of the DAC, V_{in} is the sampling voltage of the S/H circuit, and C_0 is the unity capacitor. According to (4), a smaller capacitor, C_0, can save on power consumption. However, it will also contribute to an increase in thermal noise (KT/C) to degrade the resolution of the DAC. In this paper, a metal-insulator-metal (MIM) capacitor of 24 fF is implemented in TSMC 0.18μm 1P6M CMOS process to trade off the design between power consumption and noise contribution.

Moreover, the matching and noise in the capacitor array will dominate the accuracy of the DAC. However, the process variation resulting in matching error commonly plays a more important role compared with the thermal noise. Hence, the layout of the capacitor array based on the common-centroid structure is adopted to protect against the matching error.

D. SAR controller

For an N-bit SAR, two sets of registers are required in the binary search algorithm. One is used for storing the conversion results and the other is used for estimating the results. A non-redundant structure, as illustrated in Fig. 5, is adopted to reduce the usage of the registers; this has proved to be beneficial to power consumption [7]. In this structure, a finite state machine (FSM) is used to generate the control signal. At the beginning of conversion, the most significant bit (MSB) is set to one while the remaining bits are set to zero. The initial value of the DAC output is then set to 0.5V (1/2 full scale). If the comparator output is low, the MSB will be set to 0 and saved in the SAR's output. If the output is high, the MSB will be kept as 1. The residue bits will be processed in the same operations until the least significant bit (LSB) is determined.

The detailed control unit is shown in Fig. 6. Each control unit includes one D-FF and a combination logic block performing the following operations: shift register, load data, or hold data. All these can be expressed as a Boolean algebra and expressed as follows:

$$Bit(j)_{next} = \overline{Mem} \times \overline{Bit(j)} \times Shift + Bit(j) \times Load + Mem \times Bit(j) \quad (4)$$

III. MEASUREMENT RESULTS

The SA ADC is fabricated in a standard 0.18μm 1P6M CMOS process. Fig. 7 shows the chip photograph of the SA ADC. The core area is 0.248 x 0.420 mm^2.

A. Static measurement

Fig. 8 illustrates the measured integral nonlinearity (INL) and differential nonlinearity (DNL). The input signal with 1 kHz and 500mV_{pp} full-swing magnitude of sinusoidal wave is fed into the SA ADC's input. Moreover, the sampling rate is 10 kHz. The maximum DNL is +0.38/-0.41 LSB, while the maximum INL is +0.6/-0.89 LSB.

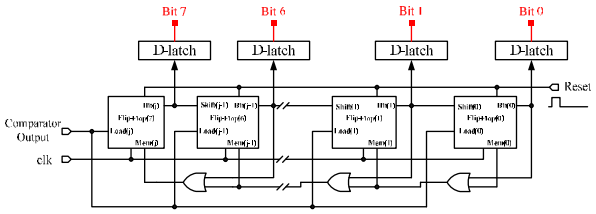

Fig. 5. N-bit SAR controller based on the non-redundant structure.

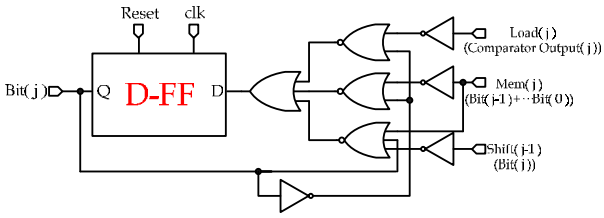

Fig. 6. Block diagram of the N_{th} control unit.

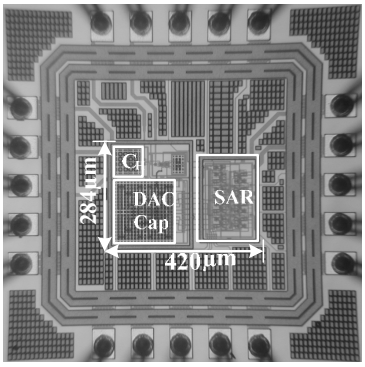

Fig. 7. Chip photograph of the SA ADC.

B. Dynamic measurement

A full-scale 1 kHz sine-wave spectrum measured at 10 kHz sampling rate is illustrated in Fig. 9. The signal-to-noise distortion ratio (SNDR) is 45.2dB and the spurious free dynamic range (SFDR) is 54 dB. Meanwhile, the effective number of bits (ENOB) defined as follows is 7.2 bits:

$$ENOB = \frac{SNDR - 1.76}{6.02} \quad (5)$$

C. Real ECG signal testing

An emulated arrhythmic ECG signal generated by the arbitrary waveform generator (AWG) is fed into the ADC. The 8-bit output waveform view displayed in the logic analyzer is adopted to demonstrate the operation of the SA ADC. Fig. 10 shows the ECG waveform reconstructed by the SA ADC's decimal codes. The waveform is consistent with the input ECG signal. Hence, the 8-bit digital codes of the SA ADC can be post-processed by the digital processor to diagnose the heart activities precisely.

Compared with other published literatures for biomedical applications [8], [9] as shown in Table II, the proposed SA ADC consumes less than 1 μW and is therefore suitable for ultra low-power biomedical systems.

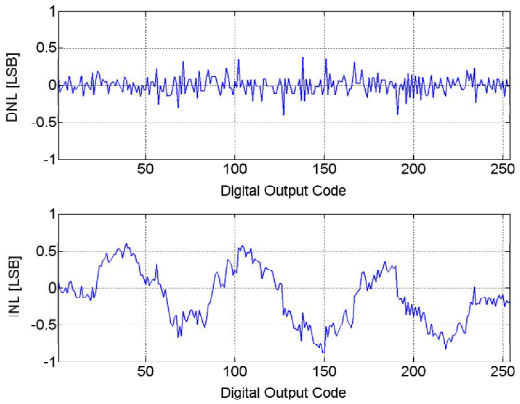

Fig. 8. Measured DNL and INL of the SA ADC.

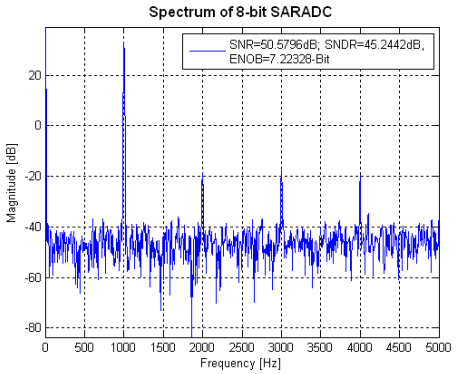

Fig. 9. Measured spectrum at 1 kHz input frequency, 500mV$_{pp}$ input swing, and 10 kHz sampling rate.

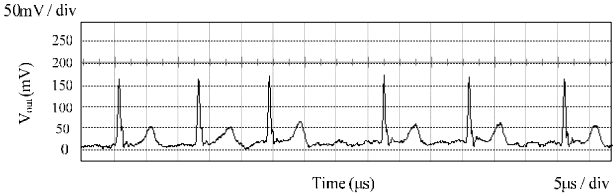

Fig. 10. Reconstructed arrhythmic ECG waveform from the SA ADC's output.

TABLE I. SUMMARY AND COMPARISONS OF THE SA ADC

	[8]*	[9]*	This work
Technology	0.18μm CMOS	0.18μm CMOS	0.18μm CMOS
Supply voltage	1	1.8	1
Power dissipation (μW)	32.6	300	0.95
ENOB (bit)	9.4	<10	7.2
Sampling rate (samples/s)	40k	70	10k
INL (LSB)	0.45	0.24	-0.89/+0.6
DNL (LSB)	0.25	0.33	-0.41/+0.38
ERBW (Hz)	300	<2k	1000
FOM (pJ/conversion-step)	80.4	>73.2	3.23

*simulation result;

$$FOM = \frac{Power}{2^{ENOB} \cdot 2 \cdot ERBW}$$

IV. CONCLUSION

A 1V, 8-bit, 10 kS/s successive approximation ADC has been implemented in the TSMC 0.18μm 1P6M CMOS process. The sub-threshold technique is adopted in the comparator design to decrease the SA ADC's power consumption. Meanwhile, a passive S/H circuit and an opamp-free, capacitor-based DAC are likewise used to meet the low-power requirement. The measurement results demonstrate that the SA ADC with 1-kHz 500 mV$_{pp}$ input sine wave can achieve ENOB of 7.2 bits under a 950 nW power consumption. Additionally, eight chips had been measured and compared in term of SNDR to represent the yield of the ADC as shown in Fig. 11. It manifests that the proposed SA ADC is suitable for low-power biomedical systems such as electrocardiogram (ECG) and electroencephalogram (EEG) acquisition systems.

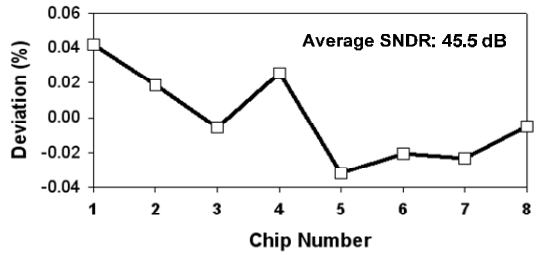

Fig. 11. SNDR spread of eight different chips.

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