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# Interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell

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**Abstract:** This study presents an interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell (VMC) techniques. The primary and secondary windings of each coupled inductor are inserted in the same phase and the third winding is inserted in the other phase. The VMC in each phase consists of two diodes, two capacitors, the secondary winding of the same phase coupled inductor and the third winding of the other phase coupled inductor. The voltage gain is increased and the output voltage is clamped across the capacitors of the VMCs. Then, the voltage across the power metal oxide semiconductor field effect transistors (MOSFETs) is decreased. The leakage inductance of the coupled inductors controls the output diode falling rate, which alleviates reverse recovery problems. The power MOSFETs are turned-on under zero current switching that helps to conversion efficiency improvement. Three modes of operation named as continuous conduction mode, discontinuous conduction mode and boundary conduction mode are investigated for the proposed converter. The carried mathematical analysis and satisfying operation of the proposed converter are verified via experimental results of an 870 W 60 V-input to 590 V-output laboratory prototype with 95.2% conversion efficiency.

## 1 Introduction

Renewable energies such as photovoltaic and fuel cells, are becoming increasingly important and widely used in distribution systems. These kinds of energies address the solutions to environmental pollution and the problem of exhaust of fossil energy reserves. However, the main characteristic of these energies is the low-output voltage, then a DC–DC converter with large voltage conversion ratio is used to increase the output voltage of the clean energy for the DC interface to the main electricity source through the DC–AC inverter [1–3]. Theoretically, the conventional transformerless DC–DC converters such as cascade boost and buck–boost converters can achieve a high-voltage conversion ratio with high-duty cycles [4, 5]. However, some effects such as the on-state resistance of the power metal oxide semiconductor field effect transistors (MOSFETs) ($r_{DS}$), the forward voltage drop ($V_{FD}$), the on-state resistance of rectifier diodes ($r_D$) and the equivalent series resistor (ESR) of capacitors and inductors will degrade the voltage gain of the converter, which limit their practical applications. Moreover, working with extreme duty cycles will cause in serious current reverse recovery and stability problems. Another important drawback of such converters is high-voltage stress across the main switch, which decreases the efficiency. The voltage conversion ratio can be extended by voltage lift and voltage multiplier cell (VMC) techniques [6–10]. However, the main switch suffers high transient current and the conduction loss is increased. Another solution for voltage gain extension is using of magnetic means such as coupled inductors with (or without) VMCs [11–18]. The voltage conversion ratio and the voltage stress across power MOSFETs can be controlled by the turns ratio of the coupled inductor. Also the reverse recovery problem of the diodes is alleviated by the leakage inductance and the leakage energy is recycled by active or passive clamp circuits. Although the extreme duty cycle is avoided in the aforementioned converters, however, the input current ripple is large because of single-phase operation, which decreases the renewable power source life time and limits their application for high-current and high-power applications. Interleaving technique can be used to minimise input power source current ripple [19–27]. The power is shared between the phases and consequently because of the reduction of losses, the conversion efficiency is maintained at high levels even for high-power applications. The proposed converter in [19] uses an resistor–capacitor-diode network to reduce the switching loss during turn-off transition. However, the duty cycle of power switches should be less than 0.5, which is a great limitation for increasing of voltage gain. The proposed converters in [20, 22, 23] employ only coupled inductor technique to increase voltage gain. However, without integrating the VMC in the converter, the voltage step-up capability is ordinary. A step-up converter based on three-state switching cell is proposed in [21]. An additional

winding is added to the auto transformer to provide high-voltage gain and reduce the voltage stress across the power switches. However, an additional inductor is needed to be inserted at the input of the converter for reducing of power source current ripple and also the power switches operate under hard commutation conditions. The converter in [24] integrates a forward energy-delivering circuit with a voltage-doubler to extend voltage gain. However, the voltage gain is not high, enough. A high step-up converter with a three-winding high-frequency coupled inductor and VMC is proposed in [25], which its power circuit is shown in Fig. 1. The third winding of each coupled inductor is inserted at the other phase. The passive clamp circuit is combined with the VMC. The VMC in each phase consists of the second winding of the coupled inductor in the same phase and the third winding of the coupled inductor at the other phase, a clamp capacitor, a clamp diode, a regenerative capacitor and a regenerative diode. The voltage gain is extended and the voltage stress across the power switches is reduced thank to coupled inductor turns ratio and VMC. The converter is suitable for high-current and high-power applications. An interleaved step-up converter is derived in [26] by inserting a VMC into the conventional interleaved boost converter. The VMC consists of a regenerative capacitor, a regenerative diode and the secondary windings of the coupled inductors. An asymmetric interleaved high step-up converter is proposed in [27] that combines the advantages of integrated fly-back boost converter and conventional interleaved boost converter with a voltage lift capacitor structure. The voltage is relatively high and the voltage stress across the power switches is low.

Based on the aforementioned discussions the integration of coupled inductor and VMC technique in interleaved structures is a better concept for obtaining higher voltage gain and less-voltage stress across the semiconductors even at high-power levels. This paper proposes an interleaved high step-up DC–DC converter suitable for high-current and high-power application. Using coupled inductor and VMC techniques, the proposed converter can achieve high-voltage gain and the voltage across the power MOSFETs is decreased. The coupled inductor has three windings. The second winding is inserted in the VMC of the same phase and the third winding is inserted in the VMC of the other phase. The VMC consists of two regenerative diodes and two regenerative capacitors instead of one regenerative diode and one regenerative capacitor and the windings of coupled inductors. The voltage gain is extended and the voltage stress across the semiconductors is reduced compared to the proposed converters in the literatures. The overall features of the proposed converter are as follows:

- High-voltage conversion ratio
- Low-voltage stress across semiconductors
- Zero current switching (ZCS) of the power MOSFETs
- Recycle of leakage energy
- Low-input current ripple
- High conversion efficiency

This paper is organised as follows:

- In Section 2, the proposed converter is presented and its modes of operation under continuous conduction mode (CCM), discontinuous conduction mode (DCM) and boundary conduction mode (BCM) are described.
- In Section 3, the performance analysis of the converter in CCM, DCM and BCM are demonstrated.
- In Section 4, the theoretical conversion efficiency, design guidelines of the proposed converter semiconductors and performance comparison are given.
- In Section 5, the discussion about unbalances effects on the operation of the proposed converter are given.
- In Section 6, the experimental results of an 870 W 60 V-input 590 V-output laboratory prototype are given to prove the satisfying operation of the proposed converter.

## 2 Proposed converter and operational stages

Fig. 2 shows the circuit configuration of proposed converter. The converter consists of a DC input voltage $V_{in}$, two power switches $S_1$ and $S_2$, two coupled inductors, seven capacitors and eight diodes. Each coupled inductor has three windings and the third winding is inserted at another phase. $L_{m1}$, $L_{m2}$ and $L_{Lk1}$, $L_{Lk2}$ are the magnetising and equivalent leakage inductors of the coupled inductors. '•' and '••' notate for the windings of coupled inductors in the first and second phase, respectively. The primary of each coupled inductor has $N_1$ turns and their secondary (second and third windings) have $N_2$ turns, respectively. Turns ratio ($N$) of the coupled inductors are equal to $N = N_2/N_1$. The VMCs are composed of two blocking capacitors ($C_{r11}$, $C_{r12}$ and $C_{r21}$, $C_{r22}$), two regenerative diodes ($D_{r11}$, $D_{r12}$ and $D_{r21}$, $D_{r22}$). $D_{C1}$ and $D_{C2}$ are the clamp diodes, $C_{C1}$and $C_{C2}$ are the clamp capacitors, $D_{o1}$ and $D_{o2}$ are the output diodes, $C_o$ is the output capacitor. The duty cycle in the proposed converter is higher than 0.5. As the main objective of the proposed converter is to obtain high-voltage gain and such characteristic is achieved when the duty cycle is higher than 0.5, hence, the steady-state analysis has been made only for this case. It is important to point out that the proposed high step-up converter can also function for duty cycle lower

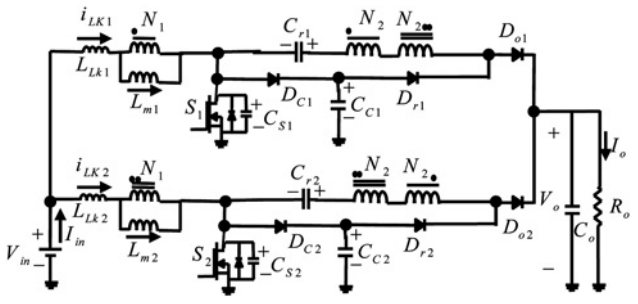

**Fig. 1** *Power circuit of the proposed converter in [25]*

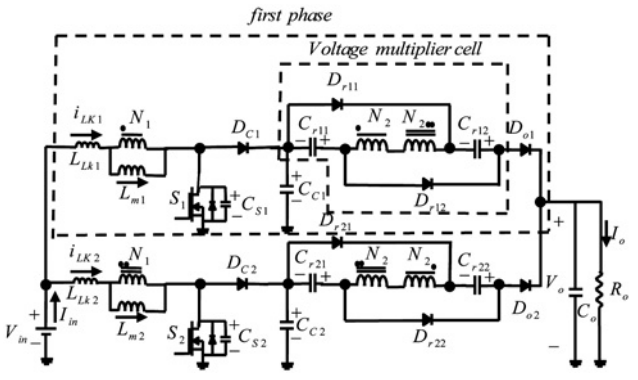


**Fig. 2** *Circuit configuration of the proposed converter*




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than 0.5. However, with duty cycle lower than 0.5, the secondary induction voltage of the transformer is lower, and consequently, it is not possible to obtain the high-voltage gain as that for duty ratio greater than 0.5. To simplify the circuit analyses following assumptions are made:

(1) All capacitors are large enough. Thus, their respective voltages are considered constant in one switching period.
(2) The power devices are ideal, but the parasitic capacitors of the power switches ($C_{S_1}$, $C_{S_2}$) are considered.

### 2.1 CCM operation

Key waveforms of the proposed converter under CCM are shown in Fig. 3. There are 14 modes of operation in one switching period. Owing to symmetry of the operation only first seven modes are analysed. Equivalent circuits of the proposed converter under CCM are shown in Figs. 4 and 5.

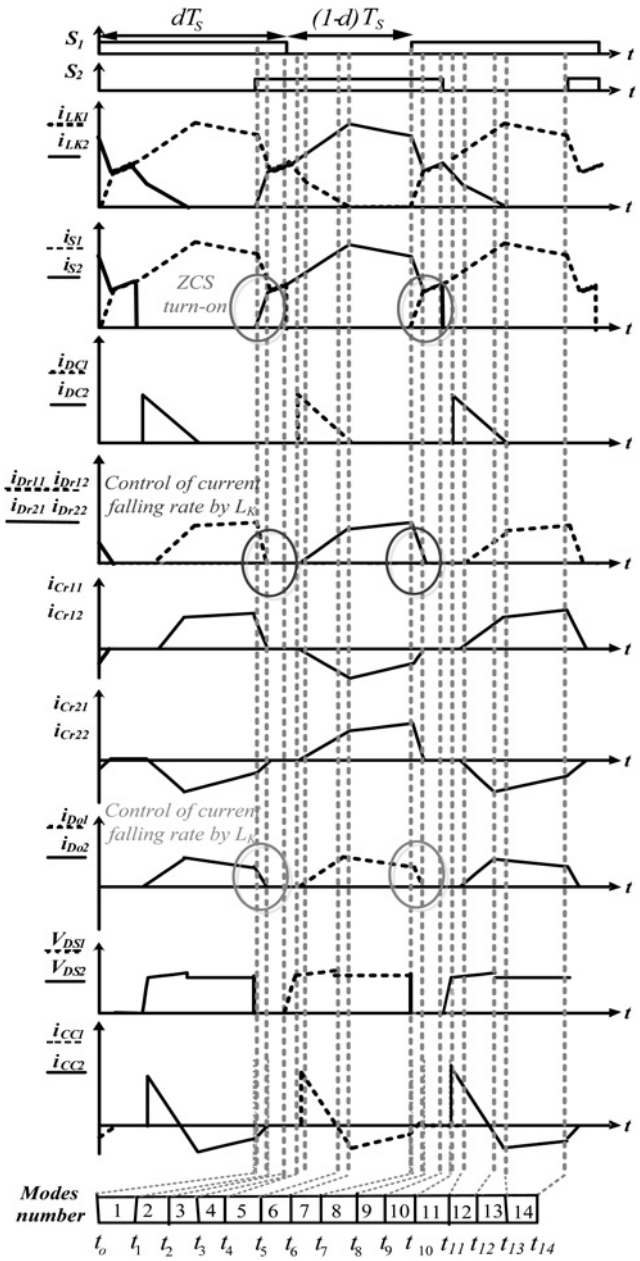


**Fig. 3** *Key waveforms of the proposed converter under CCM*

*Mode 1 [$t_0 < t < t_1$]:* At $t = t_0$, the switch $S_2$ is turned on with ZCS soft switching condition (Fig. 4*a*). The diodes $D_{C1}$, $D_{C2}$, $D_{r21}$, $D_{r22}$ and $D_{o1}$ are in turn-off state and the switch $S_1$, diodes $D_{r11}$, $D_{r12}$ and $D_{o2}$ are in turn-on state. In this time interval, the energy of $C_{S_2}$ is discharged, rapidly. The energy stored in the coupled inductors is released into the capacitors $C_{r11}$ and $C_{r12}$, at the first phase and the energy stored in the coupled inductors is released to the $C_o$, at the second phase. The current through the leakage inductor $L_{Lk2}$ is increased linearly, which leads to decrease of the secondary current through interleaved phases. This operating mode ends when the $i_{Lk2}$ reaches $i_{Lm2}$. Thus $D_{o2}$ is turned off with ZCS condition and the reverse recovery current problem is alleviated. The following equations can be written in this mode

$$L_{Lk1}\frac{\mathrm{d}i_{Lk1}}{\mathrm{d}t} = V_{in} - V_{p1} \tag{1}$$

$$i_{Lk1} = i_{p1} + i_{L_{m1}} \tag{2}$$

$$L_{Lk2}\frac{\mathrm{d}i_{Lk2}}{\mathrm{d}t} = V_{in} - V_{p2} \tag{3}$$

$$i_{Lk2} = i_{p2} + i_{L_{m2}} \tag{4}$$

$$\begin{aligned} i_{p1} &= -i_{p2} = N(2i_{D_{r11}} + i_{D_{o2}}) \\ &= -\frac{V_{C_{r11}}}{N(L_{Lk1} + L_{Lk2})}t + i_{p1}(t_0) \end{aligned} \tag{5}$$

where $i_p$ and $V_p$ notate for the current and voltage of primary side of coupled inductors.

*Mode 2 [$t_1 < t < t_2$]:* In this time interval, switches $S_1$ and $S_2$ are in turn-on state (Fig. 4*b*). Diodes $D_{C1}$, $D_{C2}$, $D_{r11}$, $D_{r12}$, $D_{r21}$, $D_{r22}$, $D_{o1}$ and $D_{o2}$ are all in turn-off state. In this mode, the inductors $L_{Lk1}$, $L_{m1}$, $L_{Lk2}$ and $L_{m2}$ are charged linearly from the DC input voltage. This mode ends when switch $S_1$ is turned off at $t = t_2$. The following equations are held in this mode of operation

$$i_{L_{m1}} = I_{L_{m1}}(t_1) + \frac{V_{in}}{L_{Lk1} + L_{m1}}(t - t_1) \tag{6}$$

$$i_{L_{m2}} = I_{L_{m2}}(t_1) + \frac{V_{in}}{L_{Lk2} + L_{m2}}(t - t_1) \tag{7}$$

$$V_{D_{C1}} = V_{C_{C1}} \tag{8}$$

$$V_{D_{C2}} = V_{C_{C2}} \tag{9}$$

*Mode 3 [$t_2 < t < t_3$]:* At time $t = t_2$, switch $S_1$ is turned off (Fig. 4*c*). The switch $S_2$ is in turn-on state. Diodes $D_{C1}$, $D_{C2}$, $D_{r11}$, $D_{r12}$, $D_{r21}$, $D_{r22}$, $D_{o1}$ and $D_{o2}$ are all in turn-off state. The parasitic capacitor $C_{S_1}$ is charged by inductors $L_{Lk1}$ and $L_{m1}$ currents. This increases the voltage across diode $D_{C1}$. This mode ends when the voltage across $D_{C1}$ reaches to zero at $t = t_3$

$$V_{D_{S_1}} = V_{C_{S_1}}(t_2) + \frac{1}{C_{S_1}}\int_{t_2}^{t} i_{C_{S_1}}\,\mathrm{d}t = \frac{I_{L_{m1}(t_2)}}{C_{S_1}}(t - t_2) \tag{10}$$

*Mode 4 [$t_3 < t < t_4$]:* At time $t = t_3$, $D_{C1}$ is turned on (Fig. 4*d*). $S_1$ is kept switched off and $S_2$ is kept switched on. Diodes $D_{C2}$, $D_{r11}$, $D_{r12}$, $D_{r21}$, $D_{r22}$, $D_{o1}$ and $D_{o2}$ are all in turn-off

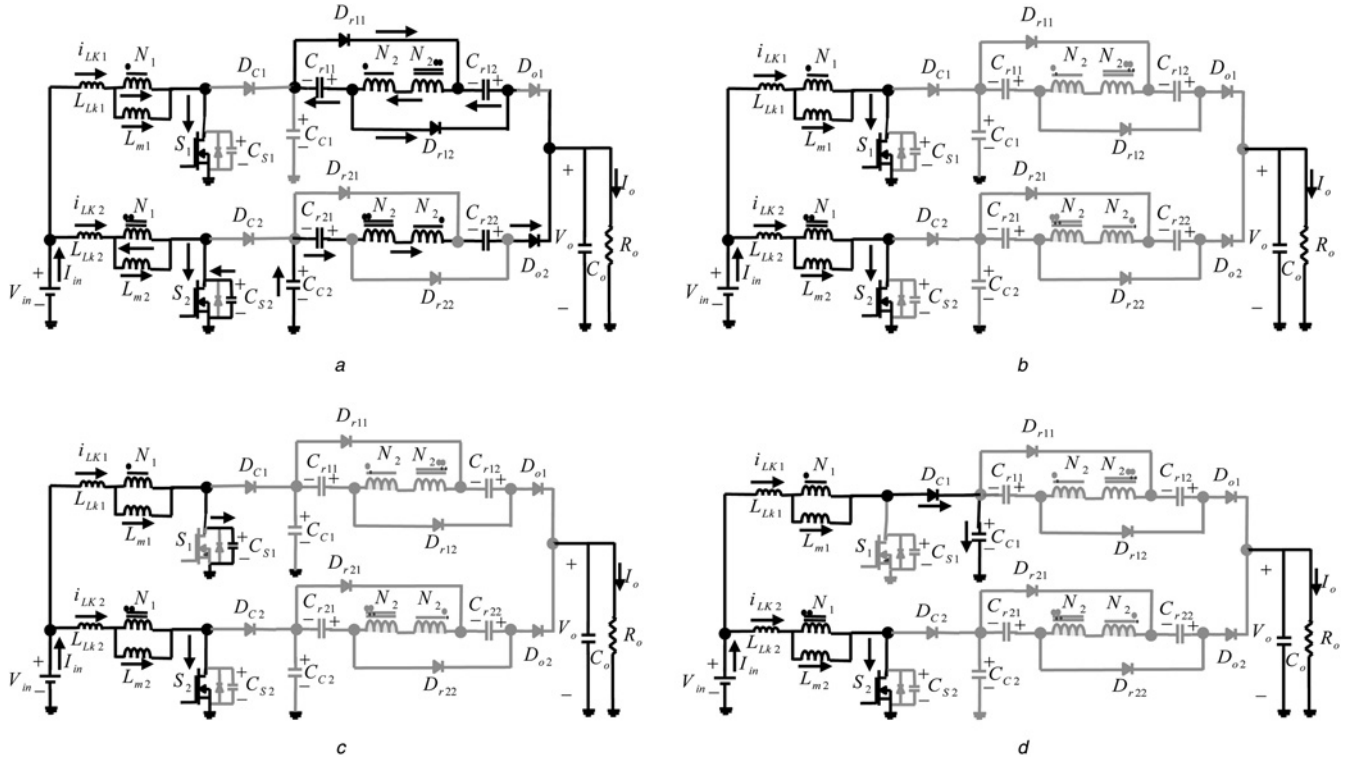


**Fig. 4** *Equivalent circuits of the proposed converter under CCM*

*a* Mode 1
*b* Mode 2
*c* Mode 3
*d* Mode 4

state. During this time interval, the stored energy in $L_{Lk1}$ and $L_{m1}$ is released to clamp capacitor $C_{C1}$ that increases the voltage across switch $S_1$ and the output diode $D_{o1}$. The inductors $L_{Lk2}$ and $L_{m2}$ are charged linearly from DC input voltage. This mode ends when the voltage across output diode $D_{o1}$ reaches to zero at $t = t_4$

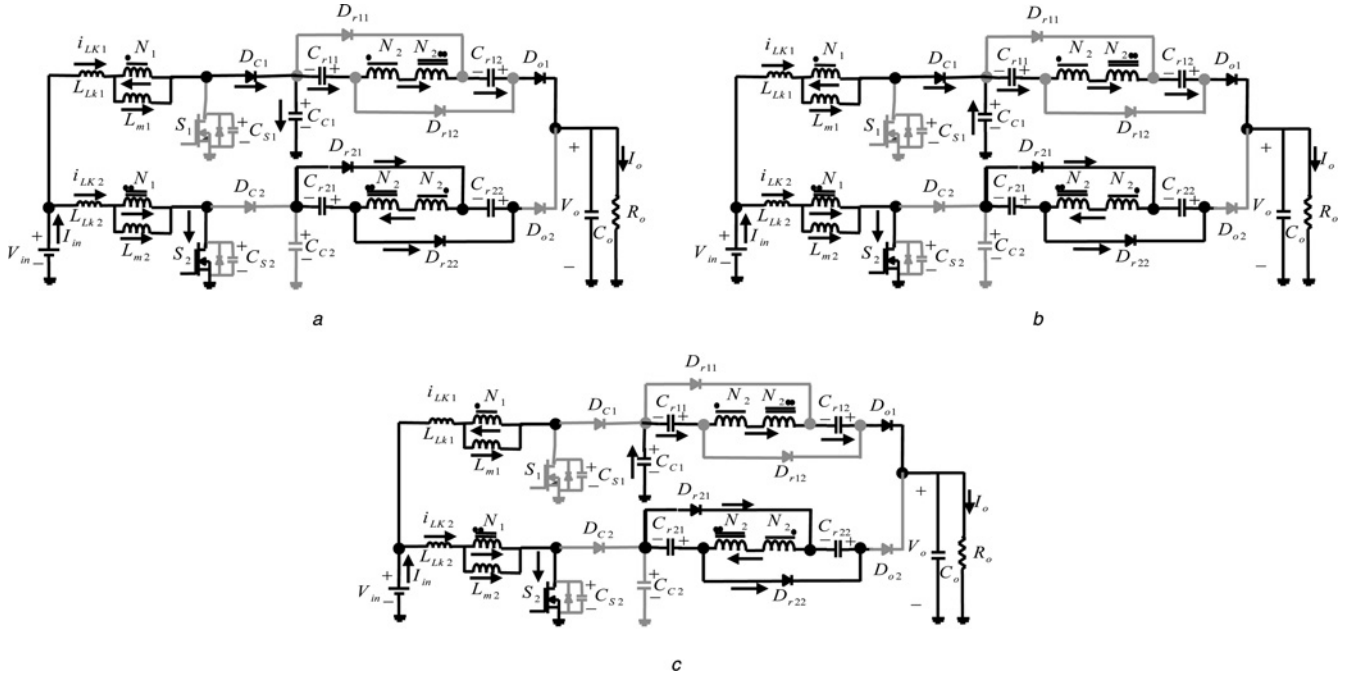


**Fig. 5** *Rest of equivalent circuits of the proposed converter under CCM*

*a* Mode 5
*b* Mode 6
*c* Mode 7




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$$V_{C_{C1}} = V_{C_{C1}}(t_3) + \frac{1}{C_{C1}}\int_{t_3}^{t} i_{C_{S_1}}\,dt$$
$$= V_{C_{C1}}(t_3) + \frac{I_{L_{m1}}(t_3)}{C_{C1}}(t - t_3) \quad (11)$$

*Mode 5 [$t_4 < t < t_5$]:* At time $t = t_4$, diode $D_{o1}$ is turned on (Fig. 5*a*). The switch $S_1$ is kept turned off and $S_2$ is kept turned on. The diodes $D_{C2}$, $D_{r11}$, $D_{r12}$ and $D_{o2}$ are in turn-off state and the diodes $D_{C1}$, $D_{o1}$, $D_{r21}$ and $D_{r22}$ are in turn-on state. The energies of $L_{Lk1}$ and $L_{m1}$ are released to clamp capacitor $C_{C1}$. The coupled inductors in first phase, DC input power source, capacitors $C_{r11}$ and $C_{r12}$ are in series to transfer the energy to the output load. Thus the capacitors $C_{r11}$ and $C_{r12}$ are discharged. Capacitors $C_{r21}$ and $C_{r22}$ are connected in parallel to each other and the secondary windings of coupled inductors in second phase and are charged, equally. This mode ends when the current through capacitor $C_{C1}$ reverses its direction at $t = t_5$

$$i_{p2} = -i_{p1} = N(2i_{D_{r21}} + i_{D_{o1}})$$
$$= \frac{(N+1)V_{C_{C1}} + 2V_{C_{r11}} - V_o}{N(L_{Lk1} + L_{Lk2})}(t - t_4) + i_{p2}(t_4) \quad (12)$$

$$i_{D_{C1}} = i_{Lk1} = i_{L_{m1}}(t_4)$$
$$- \frac{(N+1)V_{C_{C1}} + 2V_{C_{r11}} - V_o}{N(L_{Lk1} + L_{Lk2})}(t - t_4) \quad (13)$$

$$i_{C_{C1}} = i_{L_{m1}}(t) - (N+1)i_{D_{o1}} - 2Ni_{D_{r21}} \quad (14)$$

$$i_{S_2} = i_{Lk2} = i_{L_{m2}} + N(i_{D_{o1}} + 2i_{D_{r21}}) \quad (15)$$

*Mode 6 [$t_5 < t < t_6$]:* At time $t = t_5$, the current through clamp capacitor $C_{C1}$ reverses its direction (Fig. 5*b*). The equivalent circuit of the proposed converter in this time interval is similar to mode 5. This mode ends when diode $D_{C1}$ is turned off at $t = t_6$.

*Mode 7 [$t_6 < t < t_7$]:* At time $t = t_6$, the current through $D_{C1}$ reaches to zero (Fig. 5*c*). Switch $S_1$, diodes $D_{C1}$, $D_{C2}$, $D_{r11}$, $D_{r12}$ and $D_{o2}$ are in turn-off state. Switch $S_2$, diodes $D_{o1}$, $D_{r21}$ and $D_{r22}$ are in turn-on state. Inductor $L_{m1}$ releases its energy to the output load via the secondary side of the coupled inductors. Inductors $L_{m2}$ and $L_{Lk2}$ are charge linearly. This mode ends when switch $S_2$ is turned on at $t = t_7$ and the second half cycles start.

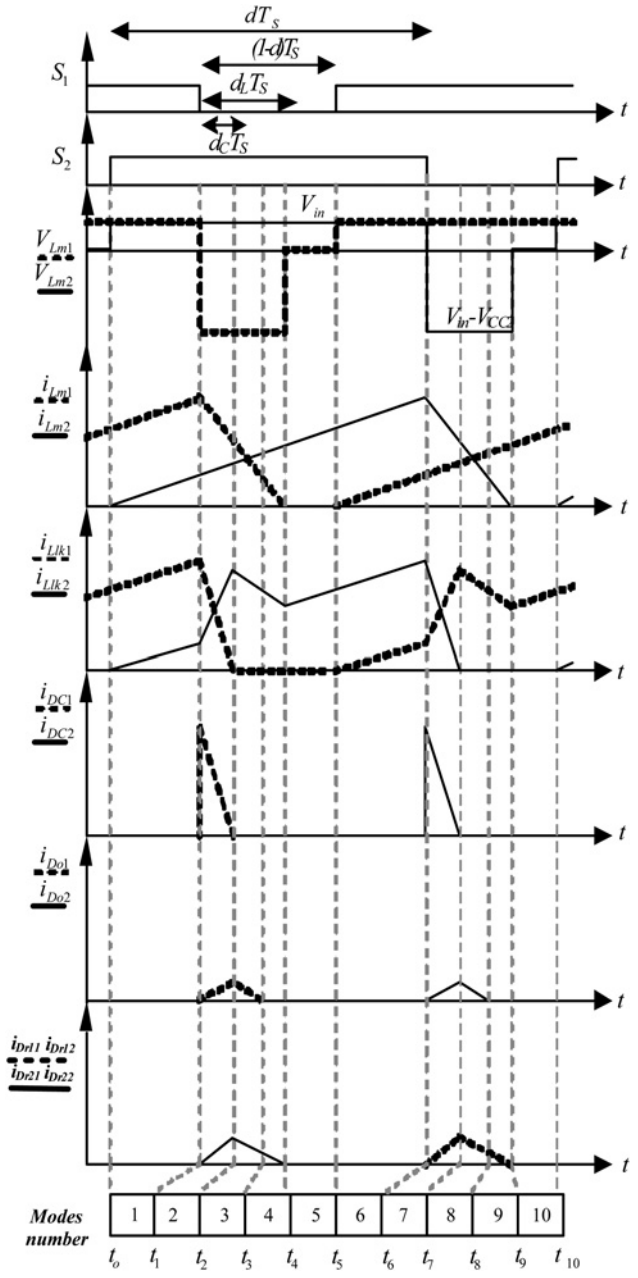


**Fig. 6** *Key waveforms of the proposed converter under DCM*

## 2.2 DCM operation

Key waveforms of the proposed converter under DCM are shown in Fig. 6. There are ten modes of operation in one switching period. Owing to symmetry of the operation only first five modes are analysed. Equivalent circuits of the proposed converter under DCM are shown in Fig. 7.

*Mode 1 [$t_0 < t < t_1$]:* In this time interval, switches $S_1$ and $S_2$ are in turn-on state (Fig. 7*a*). Diodes $D_{C1}$, $D_{C2}$, $D_{r11}$, $D_{r12}$, $D_{r21}$, $D_{r22}$, $D_{o1}$ and $D_{o2}$ are all in turn-off state. In this mode, the inductors $L_{Lk1}$, $L_{m1}$, $L_{Lk2}$ and $L_{m2}$ are charged linearly from the DC input voltage. This mode ends when switch $S_1$ is turned off at $t = t_1$.

*Mode 2 [$t_1 < t < t_2$]:* At time $t = t_1$, switch $S_1$ is turned off (Fig. 7*b*). Diodes $D_{C2}$, $D_{r11}$, $D_{r12}$ and $D_{o2}$ are in turn-off state. Switch $S_2$ and the diodes $D_{C1}$, $D_{o1}$, $D_{r21}$ and $D_{r22}$ are in turn-on state. The coupled inductors in first phase, DC input power source, capacitors $C_{r11}$ and $C_{r12}$ are in series to transfer the energy to the output load. Thus the capacitors $C_{r11}$ and $C_{r12}$ are discharged. Capacitors $C_{r21}$ and $C_{r22}$ are connected in parallel to each other and the secondary windings of coupled inductors in second phase and are charged, equally. This mode ends when diode $D_{C1}$ is turned off at $t = t_2$.

*Mode 3 [$t_2 < t < t_3$]:* At time $t = t_2$, diode $D_{C1}$ is turned off (Fig. 7*c*). Switch $S_1$, diodes $D_{C1}$, $D_{C2}$, $D_{r11}$, $D_{r12}$ and $D_{o2}$ are in turn-off state. Switch $S_2$, diodes $D_{o1}$, $D_{r21}$ and $D_{r22}$ are in turn-on state. Inductor $L_{m1}$ releases its energy to the output load via the secondary side of the coupled inductors. Inductors $L_{m2}$ and $L_{Lk2}$ are charge linearly. This mode ends when the energy of the clamp capacitor $C_{C1}$ is fully released to the output and $D_{o2}$ is turned off at $t = t_3$.

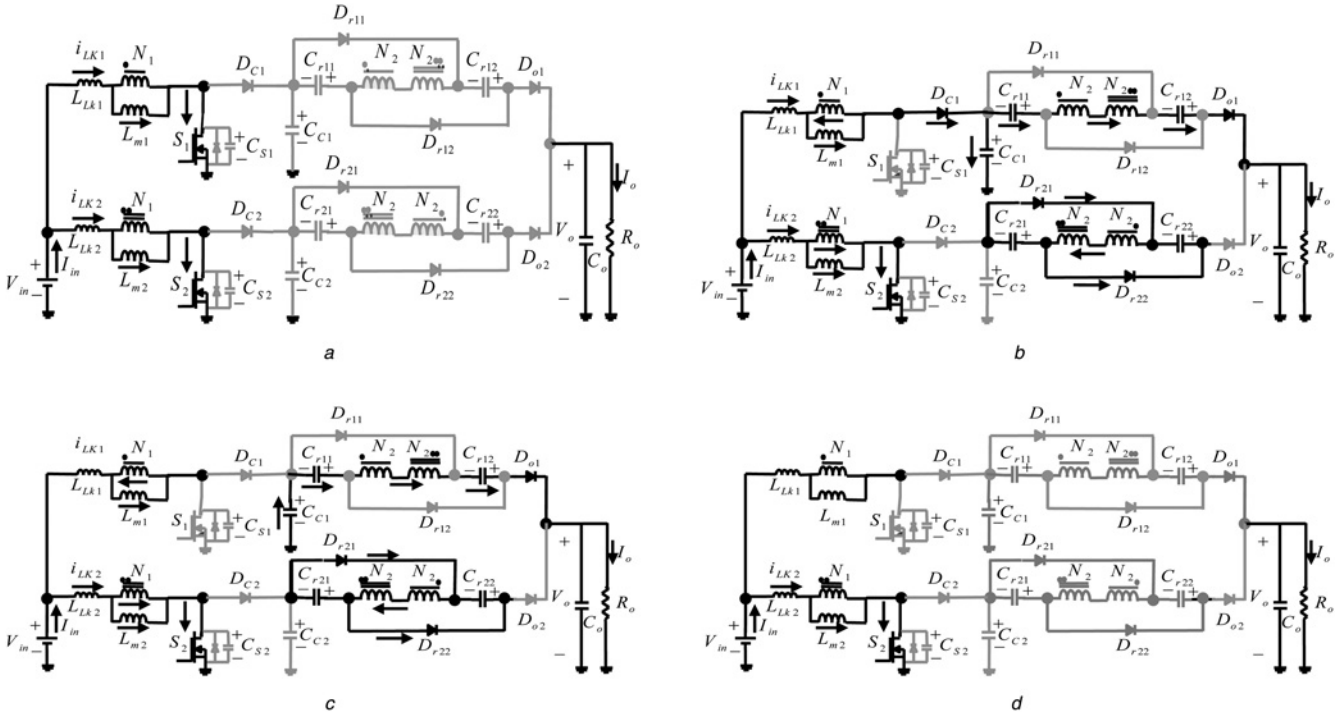


**Fig. 7** *Equivalent circuits of the proposed converter under DCM*

*a* Mode 1
*b* Mode 2
*c* Mode 3
*d* Mode 5

*Mode 4 [$t_3 < t < t_4$]:* At time $t = t_3$, diode $D_{o1}$ is turned off. Switch $S_1$, diodes $D_{C1}$, $D_{C2}$, $D_{r11}$, $D_{r12}$, $D_{o1}$ and $D_{o2}$ are all in turn-off state. Switch $S_2$, diodes $D_{r21}$ and $D_{r22}$ are in turn-on state. The remained stored energy in the magnetising inductor $L_{m1}$ is released to the capacitors $C_{r21}$ and $C_{r22}$. Owing to maximum subfigure limitation of the paper, the equivalent circuit of this time interval cannot be shown. This mode ends when $i_{L_{m1}}$ reaches to zero at $t = t_4$.

*Mode 5 [$t_4 < t < t_5$]:* At time $t = t_4$, $i_{L_{m1}}$ reaches to zero that makes the diodes $D_{r21}$ and $D_{r22}$ turned off (Fig. 7*d*). All the semiconductors except switch $S_2$ are in turn-off state. This mode ends when $S_1$ is turned on at $t = t_5$ and the second half cycles start.

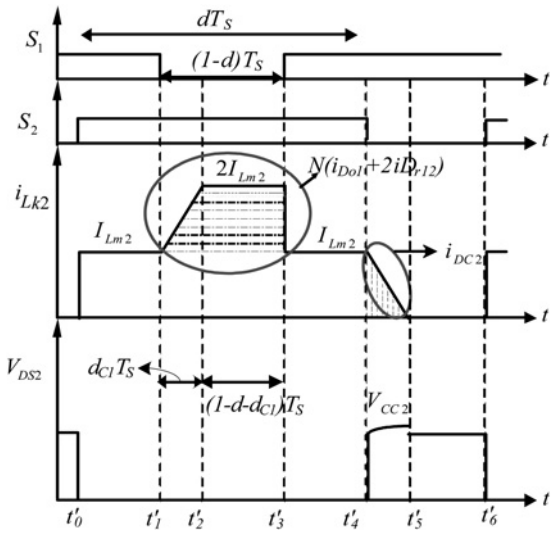


**Fig. 8** *Simplified waveforms of the proposed converter under CCM*

## 3 Steady-state analysis of the proposed converter

In this section, the steady-state analysis of the proposed converter under CCM, DCM and BCM is presented. It is assumed that $L_{Lk1} = L_{Lk2} = L_{Lk}$ and $L_{m1} = L_{m2} = L_m$. The following assumptions are made because of the symmetry of the proposed converter

$$I_{L_{m1}} = I_{L_{m2}} = I_{L_m} \tag{16}$$

$$V_{C_{C1}} = V_{C_{C2}} = V_{C_C} \tag{17}$$

$$V_{C_{r11}} = V_{C_{r12}} = V_{C_{r21}} = V_{C_{r22}} = V_{C_r} \tag{18}$$

### 3.1 CCM operation analysis

Fig. 8 shows the simplified waveforms of the proposed converter under CCM. The vertical dashed line area in Fig. 8 shows $i_{D_{C2}}$. The average value of this current is equal to $I_o/2$. Then the following equation can be written

$$I_{L_m} = \frac{I_o}{d_{C1}} \tag{19}$$

Knowing that the horizontal dashed line surface equal to $N(i_{D_{o1}} + 2i_{D_{r21}})$, then

$$\frac{(1-d)T_S + [(1-d-d_{C1})]T_S}{2T_S} I_{L_m} = \text{Ave}\left[N(i_{D_{o1}} + 2i_{D_{r21}})\right] \tag{20}$$




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DCM, (c) characteristic curves of CCM, DCM and BCM regions under $N = 1$

$$I_{L_m} = \frac{3NI_o}{2(1-d) - d_{C1}} \tag{21}$$

By equating (19) and (21), the following equations are obtained

$$d_{C1} = \frac{2(1-d)}{3N+1} \tag{22}$$

$$I_{L_m} = \frac{3N+1}{2(1-d)} I_o \tag{23}$$

The following equations can be written in the time intervals $t_1' - t_2'$ and $t_4' - t_5'$ (modes 5 and 12)

$$V_{Lk1(t'4-t'5)} = V_{Lk2(t'1-t'2)} = -V_{Lk2(t'4-t'5)} = L_{Lk}\frac{(3N+1)^2 f_S I_o}{4(1-d)^2} \tag{24}$$

$$V_{D_{S_2}(t'4-t'5)} = V_{C_C} \tag{25}$$

$$V_{C_C} = V_o - 3V_{C_r} \tag{26}$$

$$V_o = V_{C_C} + 2V_{C_r} + N[(V_{in} - V_{Lk1(t'4-t'5)}) - (V_{in} - V_{Lk2(t'4-t'5)} - V_{C_C})] \tag{27}$$

Substituting (24) into (27), yields the following equation

$$V_o = (N+1)V_{C_C} + 2V_{C_r} + 2NV_{Lk2(t'4-t'5)} \tag{28}$$

Using (26) and (28), $V_{C_C}$ and $V_{C_r}$ are derived as below

$$V_{C_C} = \frac{V_o - 6NV_{Lk2(t'4-t'5)}}{3N+1} \tag{29}$$

$$V_{C_r} = \frac{N(V_o + 2V_{Lk2(t'4-t'5)})}{3N+1} \tag{30}$$

The voltage stress across switch $S_2(S_1)$ in mode 7 (mode 14) is found to be

$$V_{D_{S_2}(t'5-t'6)} = V_{in} - \left(\frac{NV_{in} - V_{C_{r12}}}{N}\right) = \frac{V_{C_{r12}}}{N} = \frac{V_{C_r}}{N} \tag{31}$$

The voltage-second balance is applied to the primary winding of the coupled inductor, which is given by

$$V_{d_{S_2}-45} d_{C1} T_S + V_{d_{S_2}-56}(1-d-d_{C1})T_S = V_{in} T_S \tag{32}$$

From (22)–(32), the accurate voltage gain of the proposed converter in CCM operation is obtained as below

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{3N+1}{(1-d)\left[1 + \left((L_{Lk2} f_S (3N+1)^2)/(2R_o(1-d)^2)\right)\right]} \tag{33}$$

By neglecting the leakage inductor, the following equations

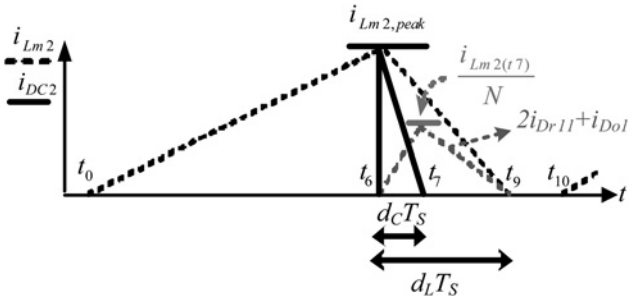


**Fig. 9** *Simplified waveforms of the proposed converter under DCM*

can be derived

$$V_{C_C} = \frac{V_{in}}{1-d} = \frac{V_o}{3N+1} \tag{34}$$

$$V_{C_r} = NV_{C_C} = \frac{NV_o}{3N+1} \tag{35}$$

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{3N+1}{(1-d)} \tag{36}$$

### 3.2 DCM operation analysis

The simplified waveforms of the proposed converter under DCM are shown in Fig. 9.

Following equations can be written in the $t_0 < t < t_6$ and $t_6 < t < t_9$ time intervals

$$V_{L_{m2}\text{-charge}} = V_{in} \tag{37}$$

$$V_{L_{m2}\text{-discharge}} = V_{in} - V_{C_{C2}} \tag{38}$$

$$V_o = 3V_{C_{r11}} + V_{C_{C2}} \tag{39}$$

$$V_{L_{m2}\text{-discharge}} = V_{in} - \frac{V_{C_{r11}}}{N} \tag{40}$$

Using (38)–(40), the following equations are obtained

$$V_{C_{r11}} = NV_{C_{C2}} \tag{41}$$

$$V_{C_{C2}} = \frac{V_o}{3N+1} \tag{42}$$

Using the volt-second balance principle on $L_{m2}$, the following equation is derived

$$V_{C_{C2}} = \left(1 + \frac{d}{d_L}\right) V_{in} \tag{43}$$

The values of $i_{L_{m2},peak}$ and $i_{L_{m2}}(t_7)$ are calculated as

$$i_{L_{m2},peak} = \frac{V_{in}}{L_{m2}} dT_S \tag{44}$$

$$i_{L_{m2}}(t_7) = i_{L_{m2},peak} + \frac{V_{in} - V_{C_{C2}}}{L_m} d_C T_S \tag{45}$$

The average values of $i_{D_{C1}}$ and $2i_{D_{r11}} + i_{D_{o2}}$ are $I_o/2$ and $3I_o/2$, respectively. Then $d_C$ and $d_L$ are found to be

$$d_C = \frac{I_o L_m}{dV_{in} T_S} \tag{46}$$

$$d_L = \frac{3NI_o}{i_{L_{m2},peak} + \left(\left(V_{in} - V_{C_{C2}}\right)/L_m\right) d_C T_S} = \frac{3NI_o L_m f_S}{(d + d_C)V_{in} - d_C V_{C_{C2}}} \tag{47}$$

Substituting (42) and (47) into (43), the voltage gain of the proposed converter under DCM operation is obtained as

$$M_{DCM} = \frac{3N+1}{2} + \sqrt{\frac{(3N+1)^2}{4} + \frac{d^2}{\tau_L}} \tag{48}$$

where $\tau_L = L_m f_S / R_o$ is the normalised magnetising inductor time constant.

### 3.3 BCM operation analysis

When the proposed converter is operating in BCM condition, the voltage gain of CCM and DCM operations are equal. Using (36) and (48), the following equation is obtained as boundary normalised magnetising inductor time constant $\tau_{L_B}$

$$\tau_{L_B} = \frac{d(1-d)^2}{(3N+1)^2} = \frac{d}{M_{CCM}^2} \tag{49}$$

Fig. 10 shows the characteristic curves of the proposed converter under CCM, DCM and BCM regions under $N = 1$. If the $\tau_L$ is higher than $\tau_{L_B}$, the proposed converter operates in CCM, else it operates in DCM.

## 4 Analysis of the conduction losses, design guidelines and performance comparison

In this section, the conduction losses of the proposed converter are analysed. Then the design guidelines of semiconductors and performance comparison between the proposed converter and some other solutions in the literatures are presented.

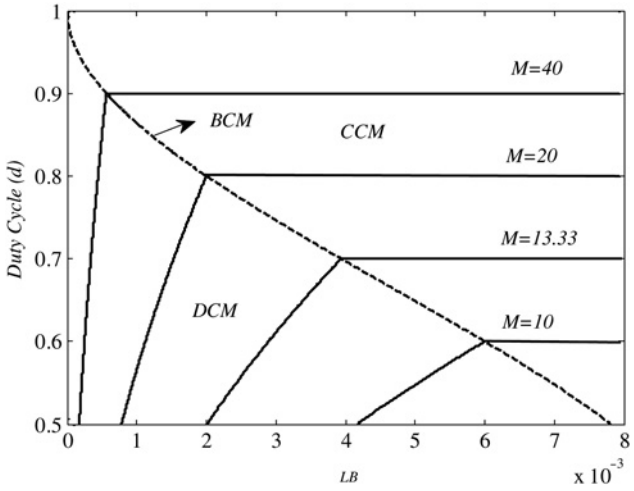


**Fig. 10** *Characteristic curves of the proposed converter under CCM, DCM and BCM*

### 4.1 Analysis of the conduction losses

Some conduction losses are caused by ESRs of the semiconductor components and the coupled inductor. Thus they can affect the efficiency of the proposed converter. To simplify the conduction losses analysis of the proposed converter, the leakage inductors of the coupled inductors are neglected. The operating principle of the proposed converter is divided into six modes, for which because of the symmetry of the operation only the first three modes are shown in Fig. 11.

*Mode 1 [$0 < t < (d - 0.5)T_S$]:* In this mode, power switches $S_1$ and $S_2$ are turned on and all the diodes are in turn-off state. The equivalent circuit is shown in Fig. 11*a* and the following equations can be derived

$$V_{in} = I_{L_{m1}}(r_{L_{11}} + r_{D_{S_1}}) + V^{I}_{L_{m1}} \tag{50}$$

$$V_{in} = I_{L_{m2}}(r_{L_{21}} + r_{D_{S_2}}) + V^{II}_{L_{m2}} \tag{51}$$

*Mode 2 [$(d - 0.5)T_S < t < (d + d_{C1} - 0.5)T_S$]:* In this mode, power switch $S_1$ is turned off and diodes $D_{C1}$, $D_{o1}$, $D_{r21}$ and $D_{r22}$ are turned on. The equivalent circuit is shown in Fig. 11*b* and the following equations can be derived

$$V_{in} = V^{I}_{L_{m1}} + [I_{L_{m1}} - N(I_{D_{o1}} + 2I_{D_{r21}})] \times (r_{L_{11}} + r_{D_{C1}}) + V_{F_{D_{C1}}} + V_{C_{C1}} \tag{52}$$

$$V_{in} = V^{II}_{L_{m2}} + [I_{L_{m2}} + N(I_{D_{o1}} + 2I_{D_{r21}})](r_{L_{21}} + r_{S_2}) \tag{53}$$

$$V_o = V_{C_{r11}} + V_{C_{r12}} + V_{C_{C1}} + N(V^{II}_{L_{m2}} - V^{II}_{L_{m1}}) - (r_{L_{12}} + r_{L_{23}})I_{D_{o1}} - V_{F_{D_{o1}}} \tag{54}$$

$$N(V^{II}_{L_{m1}} - V^{II}_{L_{m2}}) + V_{C_{r11}} + 2I_{D_{r21}}(r_{L_{22}} + r_{L_{13}}) + V_{F_{D_{r21}}} + r_{D_{r21}}I_{D_{r21}} = 0 \tag{55}$$

$$N(V^{II}_{L_{m1}} - V^{II}_{L_{m2}}) + V_{C_{r22}} + 2I_{D_{r21}}(r_{L_{22}} + r_{L_{13}}) + V_{F_{D_{r22}}} + r_{D_{r22}}I_{D_{r22}} = 0 \tag{56}$$

*Mode 3 [$(d + d_{C1} - 0.5)T_S < t < 0.5T_S$]:* In this mode, diode $D_{C1}$ is turned off. The equivalent circuit is shown in Fig. 11*c* and the following equations can be obtained that are equal to (52)–(56)

$$V_{in} = V^{III}_{L_{m2}} + [I_{L_{m2}} + N(I_{D_{o1}} + 2I_{D_{r21}})](r_{L_{21}} + r_{S_2}) \tag{57}$$

$$V_o = V_{C_{r11}} + V_{C_{r12}} + V_{C_{C1}} + N(V^{III}_{L_{m2}} - V^{III}_{L_{m1}}) - (r_{L_{12}} + r_{L_{23}})I_{D_{o1}} - V_{F_{D_{o1}}} \tag{58}$$

$$N(V^{III}_{L_{m1}} - V^{III}_{L_{m2}}) + V_{C_{r11}} + 2I_{D_{r21}}(r_{L_{22}} + r_{L_{13}}) + V_{F_{D_{r21}}} + r_{D_{r21}}I_{D_{r21}} = 0 \tag{59}$$

$$N(V^{III}_{L_{m1}} - V^{III}_{L_{m2}}) + V_{C_{r22}} + 2I_{D_{r21}}(r_{L_{22}} + r_{L_{13}}) + V_{F_{D_{r22}}} + r_{D_{r22}}I_{D_{r22}} = 0 \tag{60}$$

In general, to predict the power loss in resistor $R$, we should calculate RMS current ($I_{RMS}$) through the resistor rather than the average current. Then the power loss will be equal to $RI^2_{RMS}$. However, the small ripple approximation technique




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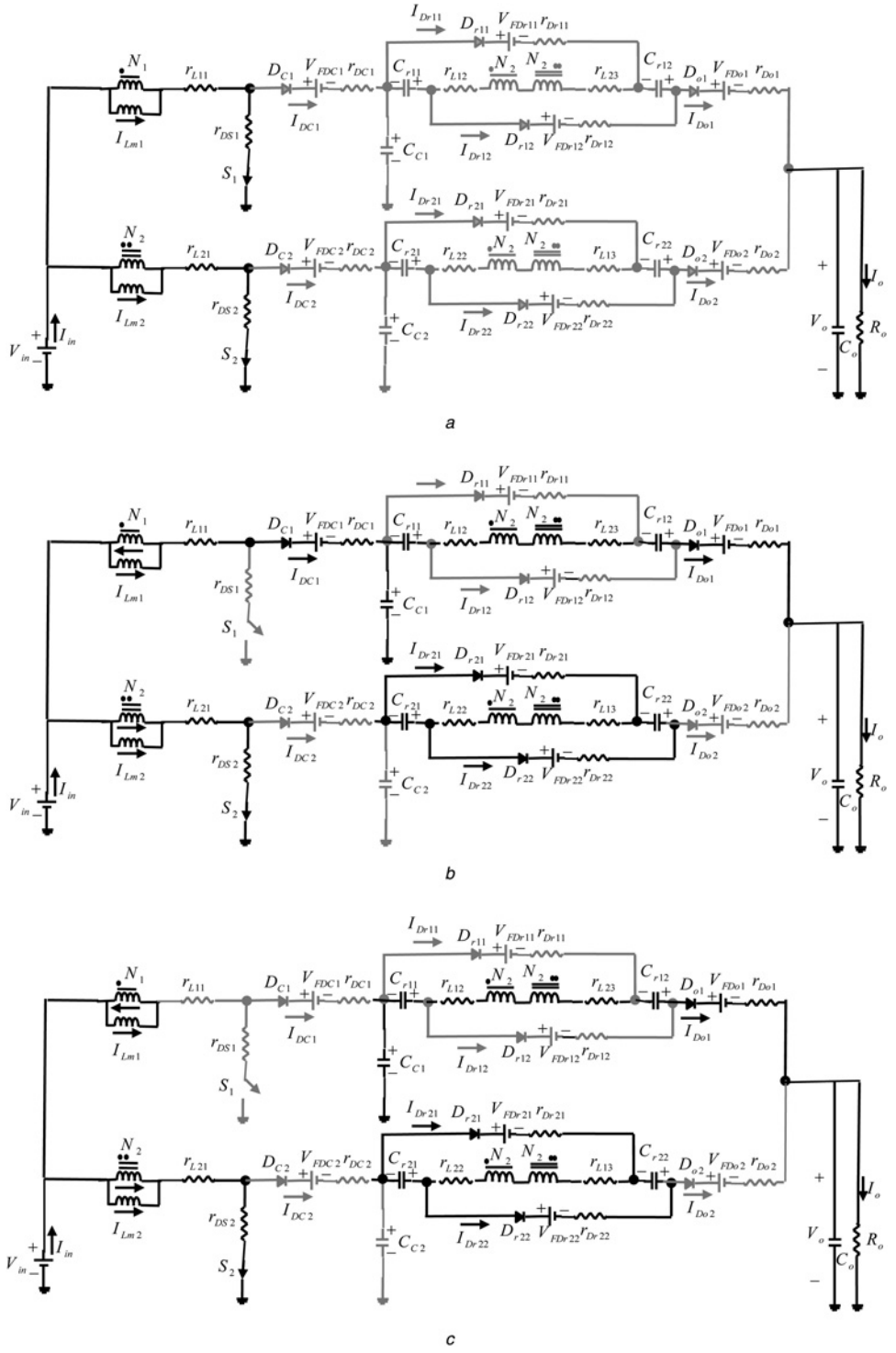


**Fig. 11** *Equivalent circuits of the proposed converter, including the ESRs of the coupled inductors, the on-state forward voltage drop of the diodes and resistance of power MOSFETs and diodes*

*a* Mode 1 $[0 < t < (d - 0.5)T_S]$
*b* Mode 2 $[(d - 0.5)T_S < t < (d + d_{C1} - 0.5)T_S]$
*c* Mode 3 $[(d + d_{C1} - 0.5)T_S < t < 0.5T_S]$

can correctly predict the losses, provided that the current ripple is small. However, in real condition the current ripple is not zero. Suppose that the average current that follows through the MOSFET during $dT_S$ is $I$. Consider three case for the MOSFET resistor current (during $dT_S$) [28].

*Case (a):* the current ripple is 0 ($\Delta i = 0$): $I_{RMS} = I\sqrt{d}$, $P_{Loss} = RI_{RMS}^2 = dRI^2$ and $P_{average} = dRI^2$.

*Case (b):* the current ripple is $0.1I$ ($\Delta i = 0.1I$): $I_{RMS} = (1.0067)I\sqrt{d}$, $P_{Loss} = RI_{RMS}^2 = (1.0033)dRI^2$ and $P_{average} = dRI^2$.

*Case (c):* the current ripple is $I$ ($\Delta i = I$): $I_{RMS} = (1.155)I\sqrt{d}$, $P_{Loss} = RI_{RMS}^2 = (1.3333)dRI^2$ and $P_{average} = dRI^2$.

As can be seen in the worse condition [case (c)], the difference between the actual power loss and average power

loss is 0.3333. Then the average model can nearly correctly predict the power loss [12, 27, 28].

Then, small ripple approximation is used to calculate the conduction losses. Thus all currents that pass through the components are approximated by the DC components. The average currents that pass through the diodes can be obtained as below

$$I_{D_{C1}} = I_{D_{o1}} = I_{D_{r21}} = I_{D_{r22}} = \frac{I_o}{2(1-d)} \tag{61}$$

From mode 2, the magnetising current $I_{L_{m1}}$ can be obtained

$$I_{L_{m1}} = N(I_{D_{o1}} + 2I_{D_{r21}}) = \frac{(3N+1)I_o}{2(1-d)} \tag{62}$$

Owing to symmetry of the phases, ESRs of the coupled inductors and the characteristics of semiconductors are taken equal. Then

$$r_{D_{S_1}} = r_{D_{S_2}} = r_{D_S} \tag{63}$$

$$r_{L_{11}} = r_{L_{21}} = r_{L_1} \tag{64}$$

$$r_{L_{12}} = r_{L_{13}} = r_{L_{22}} = r_{L_{23}} = r_{L_2} \tag{65}$$

$$V_{F_{D_{C1}}} = V_{F_{D_{C2}}} = V_{F_{D_C}} \tag{66}$$

$$r_{D_{C1}} = r_{D_{C2}} = r_{D_C} \tag{67}$$

$$V_{F_{D_{r11}}} = V_{F_{D_{r12}}} = V_{F_{D_{r21}}} = V_{F_{D_{r22}}} = V_{F_{D_r}} \tag{68}$$

$$r_{D_{r11}} = r_{D_{r12}} = r_{D_{r21}} = r_{D_{r22}} = r_{D_r} \tag{69}$$

$$V_{F_{D_{o1}}} = V_{F_{D_{o2}}} = V_{F_{D_o}} \tag{70}$$

$$r_{D_{o1}} = r_{D_{o2}} = r_{D_o} \tag{71}$$

Applying the volt-second principle for $L_{m1}$ and using (50)–(71), the following equations are derived

$$V_{C_C} = \frac{V_{in}}{1-d} - \frac{(3N+1)I_o}{2(1-d)}\left\{\frac{(2d-1)(r_{L_1}+r_{D_S})}{1-d} + \frac{r_{L_1}+r_{D_C}+(6N+1)(1-d)(r_{L_1}+r_{D_S})}{3N+1}\right\} - V_{F_{D_C}} \tag{72}$$

$$V_{C_r} = \frac{NI_o}{2(1-d)} \times \left[(r_{L_1}+r_{D_C}) - (6N+1)(r_{L_1}+r_{D_S}) - \frac{(4r_{L_2}+r_{D11})}{N}\right] + NV_{C_C} + NV_{F_{D_C}} - V_{F_{D_r}} \tag{73}$$

$$M = \frac{V_o}{V_{in}} = \frac{((3N+1)/(1-d)) - (1/V_{in})(V_{F_{D_C}} + V_{F_{D_o}} + 2V_{F_{D_r}})}{1 + (A/(2(1-d)R_o))} \tag{74}$$

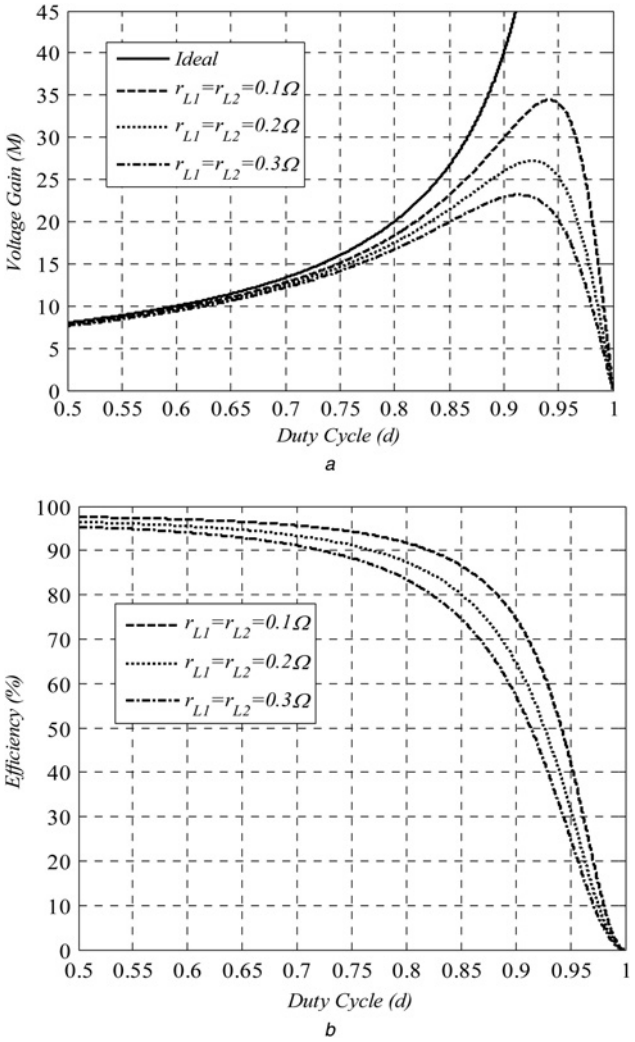


**Fig. 12** *Steady-state curves of the proposed converter*

*a* Voltage gain of the proposed converter, including parasitic components
*b* Efficiency of the proposed converter, including parasitic components

where

$$A = 3N(6N+1)(r_{L_1}+r_{D_S}) + r_{L_1} + 10r_{L_2} + r_{D_C} + r_{D_o} + 2r_{D11} + (r_{L_1}+r_{D_S})(6N+1)(1+3N)(1-d) + \frac{(2d-1)(3N+1)^2(r_{L_1}+r_{D_S})}{(1-d)}$$

Efficiency is expressed as below

$$\eta = \frac{P_o}{P_{in}} = M\frac{I_o}{I_{in}} = M\frac{I_o}{2I_{LM}} = \frac{M}{((3N+1)/(1-D))} \times \frac{1-((1-d)/(V_{in}(3N+1)))(V_{F_{D_C}} + V_{F_{D_o}} + 2V_{F_{D_r}})}{1+(A/(2(1-d)R_o))} \tag{75}$$

Figs. 12*a* and *b* show the curves of $M$ and $\eta$ against $d$ under the following conditions




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**Table 1** Components stress analysis of the proposed converter

| Parameters | Values |
|---|---|
| voltage stress across switches and clamp diodes | $V_{C_C} = \frac{V_o}{3N+1}$ |
| voltage stress across diodes when one of switches is on (except clamp diodes) | $2V_{C_r} = \frac{2NV_o}{3N+1}$ |
| voltage stress across diodes when both of switches are on (except clamp diodes) | $V_{C_r} = \frac{NV_o}{3N+1}$ |
| average current of switches | $dI_{in}/2$ |
| RMS current of switches | $\sqrt{d}I_{in}/2$ |
| average current of all diodes | $I_o/2$ |
| RMS current of clamp diodes | $\sqrt{d_{C1}}I_o/2$ |
| RMS currents of diodes (except clamp diodes) | $\frac{I_o}{2\sqrt{1-D}}$ |

$$V_{in} = 60\,\text{V}; \quad V_o = 590; \quad N = 1; \quad R_o = 400\,\Omega$$
$$r_{D_S} = 0.07\,\Omega$$
$$r_{D_C} = r_{D_r} = r_{D_o} = 0.01\,\Omega$$
$$V_{F_{D_C}} = V_{F_{D_r}} = V_{F_{D_o}} = 1\,\text{V}$$

As can be seen both voltage gain and efficiency are affected by various coupled inductor winding ESRs and duty cycles. Working at extreme duty cycles reduces the conversion efficiency.

### 4.2 Design guidelines and performance comparison

The voltage and current stresses of the semiconductors of the proposed converter are summarised in Table 1 that can be helpful for specific designers. To understand the merits of the proposed converter some comparisons with other high step-up solutions in the literature in the terms of voltage gain, the maximum voltage across power MOSFETs, the highest voltage on diodes and also components number are presented in Table 2. Also the proposed converter utilises more diodes compared to the conventional converters, however, the voltage gain and highest voltage stress across semiconductors have been improved. The curves of normalised voltage stress of semiconductors are shown in Fig. 13. As can be seen, the proposed converter achieves higher voltage gains and the voltage stress across the semiconductors is lower when compared to the conventional ones. Then switches with lower $r_{D_S}$ and diodes with lower forward voltage drop can be adapted, that reduces the on-state losses of the proposed converter at higher voltages and currents.

The value of magnetising inductors $L_{m1}$ and $L_{m2}$ can be designed based on the equation of BCM condition, which is

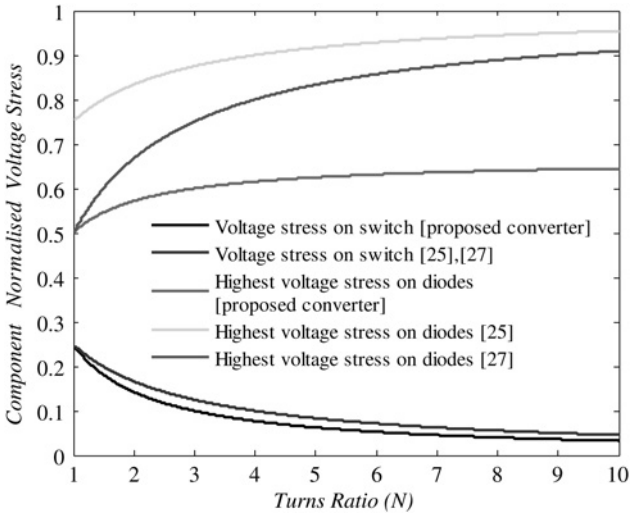


**Fig. 13** *Comparison of components normalised voltage stress between proposed converter and other converters in the literatures*

derived from

$$L_{mB} = \frac{d(1-d)^2 R_o}{f_S(3N+1)^2} \tag{76}$$

The turns ratio design is the key parameter for the proposed converter, because it determined the voltage stress across semiconductors, which is given by

$$N = \frac{1}{3}\left[\frac{V_o}{V_{in}}(1-D) - 1\right] \tag{77}$$

Once the duty cycle of the switches is selected, the turns ratio of the coupled inductors can be designed.

Assuming all the stored energy in the leakage inductor is released to the clamp capacitor, the value of the clamp capacitor can be designed as below

$$C_C \simeq \frac{L_{Lk} I_{in,max}^2}{8V_{C_C}\Delta V_{C_C}} \tag{78}$$

where $I_{in,max}$ is the maximum value of the input current and $\Delta V_{C_C}$ is the voltage ripple on the clamp capacitor. As can be seen from (78), a large value of the clamp capacitor may reduce the voltage ripple, greatly. However, a too large value has no improvement in clamping performance and it is bulky and costly. The value of the regenerative capacitor can be designed as below

$$C_r \simeq \frac{P_o}{2V_o f_S \Delta V_{C_r}} = \frac{I_o}{2f_S \Delta V_{C_r}} \tag{79}$$

**Table 2** Performance comparison of the proposed converter and other interleaved structures in the literature

| High step-up converter | Converter in [25] | Converter in [27] | Proposed converter |
|---|---|---|---|
| voltage gain | $((2(N+1))/(1-d))$ | $((2(N+1))/(1-d))$ | $((3N+1)/(1-d))$ |
| voltage stress of switches | $(V_o/(2(N+1)))$ | $(V_o/(2(N+1)))$ | $(V_o/(3N+1))$ |
| highest voltage stress on diodes | $((NV_o)/(N+1))$ | $(((2N+1)V_o)/(2(N+1)))$ | $((2NV_o)/(3N+1))$ |
| quantities of diodes | 6 | 4 | 8 |
| quantities of cores | 2 | 2 | 2 |
| quantities of secondary side windings | 2 | 1 | 2 |

**Table 3** Simulation of current differences $\Delta = (I_{in1} - I_{in2})/I_{in1}$ between the phases because of the asymmetrical duty cycle

| $D_1 = 61.5\%$ | $\Delta = (I_{in1} - I_{in2})/I_{in1}$ | |
|---|---|---|
| | Case (1): $N = 1$, $V_{in} = 60$ V | Case (2): $N = 2$, $V_{in} = 63$ V |
| $D_2 = 56.5$ | 0.16 | 0.1 |
| $D_2 = 57.5$ | 0.1023 | 0.076 |
| $D_2 = 58.5$ | 0.092 | 0.064 |
| $D_2 = 59.5$ | 0.05 | 0.042 |
| $D_2 = 60.5$ | 0.032 | 0.02 |
| $D_2 = 61.5$ | 0 | 0 |
| $D_2 = 62.5$ | −0.031 | −0.03 |
| $D_2 = 63.5$ | −0.051 | −0.044 |
| $D_2 = 64.5$ | −0.1 | −0.09 |
| $D_2 = 65.5$ | −0.16 | −0.12 |
| $D_2 = 66.5$ | −0.21 | −0.15 |

**Table 4** Simulation of current differences $\Delta = (I_{in1} - I_{in2})/I_{in1}$ between the phases because of the asymmetrical leakage inductors

| $L_{k1}$, μH | 6 | 6 | 6 | 6 |
|---|---|---|---|---|
| $L_{k2}$, μH | 1.5 | 3 | 6 | 15 |
| $\Delta = (I_{in1} - I_{in2})/I_{in1}$, % | −2 | −1.8 | 0 | 2.4 |

One key point on selecting the power MOSFETs and power diodes is that the maximum imposed voltage across them during turn-off state, should be less than the maximum allowed values from the data sheet. Then from Table 1, following constraint should be held

$$\left(V_{\text{Mosfet}} = V_{D_C} = \frac{V_{\text{in,max}}}{1 - d_{\max}}\right) < V_{\text{Data sheet}} \tag{80}$$

$$\left(V_{D_r} = \frac{2NV_{\text{in,max}}}{1 - d_{\max}}\right) < V_{\text{Data sheet}} \tag{81}$$

## 5 Discussion of unbalances in the proposed converter

Two main parameters than can affect the balance operation of the two phases and consequently the equal current sharing performance, are the duty cycle and leakage inductors. Table 3 shows the simulation of current differences $\Delta = (I_{in1} - I_{in2})/I_{in1}$ between the phases because of the asymmetrical duty cycle. The simulations have been done in PSCAD-EMTDC software. The duty cycle of phase 1 is kept at 61.5% and the duty cycle of the second phase varies from 56.5 to 66.5%. The simulations have been done for two cases:

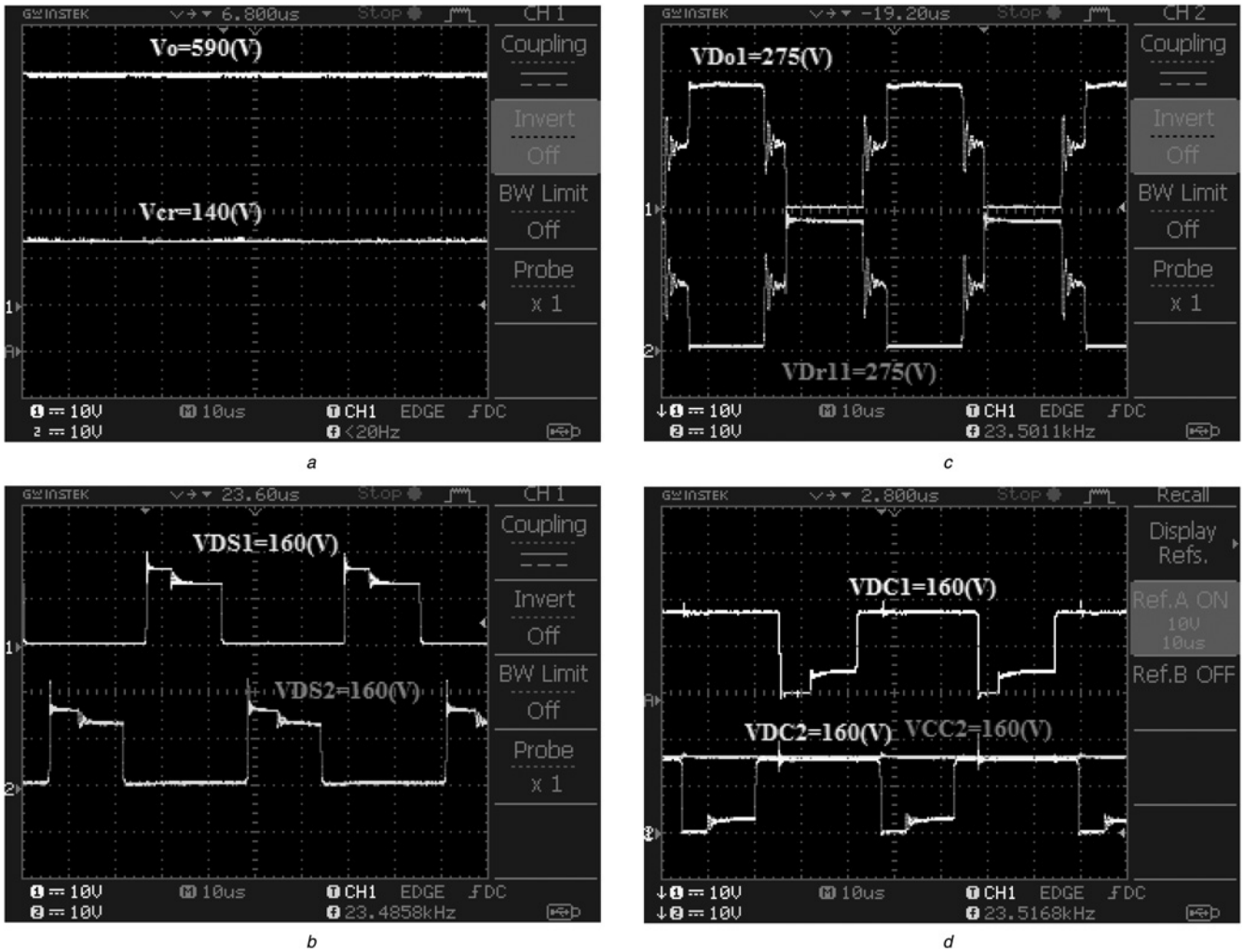


**Fig. 14** *Voltage measurements of the proposed converter under CCM [vertical axis: 100 V/Div. (probe*10), horizontal axis: 10 μS/Div.]*

(a) $V_o$ and $V_{Cr}$
(b) $V_{DS1}$ and $V_{DS2}$
(c) $V_{Do1}$ and $V_{Dr11}$
(d) $V_{DC1}$, $V_{DC2}$ and $V_{CC2}$




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case (1): $N = 1$, $V_{in} = 60$ V, and case (2): $N = 2$, $V_{in} = 33$ V. It can be seen in both cases at $d_1 = d_2 = 61.5\%$ the current difference is zero. In cases (1) and (2), when $d_2 = 66.5\%$, the current difference is −0.21 and −0.15, respectively. From the simulation results, it can be concluded that increasing of turns ratio can improve the current sharing performance. The simulation results of the current sharing performance under different leakage inductances are shown in Table 4. It can be seen that the leakage inductors have a negligible effect on current sharing performance even when the difference between them is considerable Table 4.

## 6 Experimental verification

To verify the effectiveness of the proposed converter a 870 W prototype is built. The specification of the tested converter is as below

$V_{in} = 60$ V; $V_o = 590$ V; $P_o = 870$ W; $f_S = 23.5$ kH
$N = 1$, $L_{Lk1} = L_{Lk2} = 6$ μH; $L_{m1} = L_{m2} = 320$ μH
$C_o = 330$ μF;

$C_{C1} = C_{C2} = C_{r11} = C_{r12} = C_{r21} = C_{r22} = 68$ μF
$D_{C1}, D_{C1}, D_{r11}, D_{r12}, D_{21}, D_{22}, D_{o1}, D_{o2}$: MUR1560
$S_1, S_2$: $N$-channel MOSFET STW45NM50F
$r_{D_S} = 0.07\,\Omega$

E-55 Ferrit cores have been selected for coupled inductors. The primary winding, the second winding and the third winding are all 35 turns. According to (24), (29), (30) and (33), $V_{C_C} = 158$ V, $V_{C_r} = 144$ V and $V_o = 611$ V. According to Table 1, the components voltage stresses are obtained as: $V_{D_S} = V_{D_C} = V_{C_C} = 157$ V, $V_{D_r} = V_{D_o} = 2V_{C_r} = 288$ V. It should be noticed that the values of voltage stresses in Table 1 is based on ideal conditions (34) and (35). Fig. 14 shows the voltage measurements of the proposed converter under CCM. As can be seen the mathematical analysis and the experimental results match each other, fairly. However, the difference between the mathematical analysis and experimental results is because of the parasitic components of the proposed converter such as ESRs and forward voltage drop of the diodes.

Fig. 15 shows the current measurements of the proposed converter under CCM. Relatively good current sharing

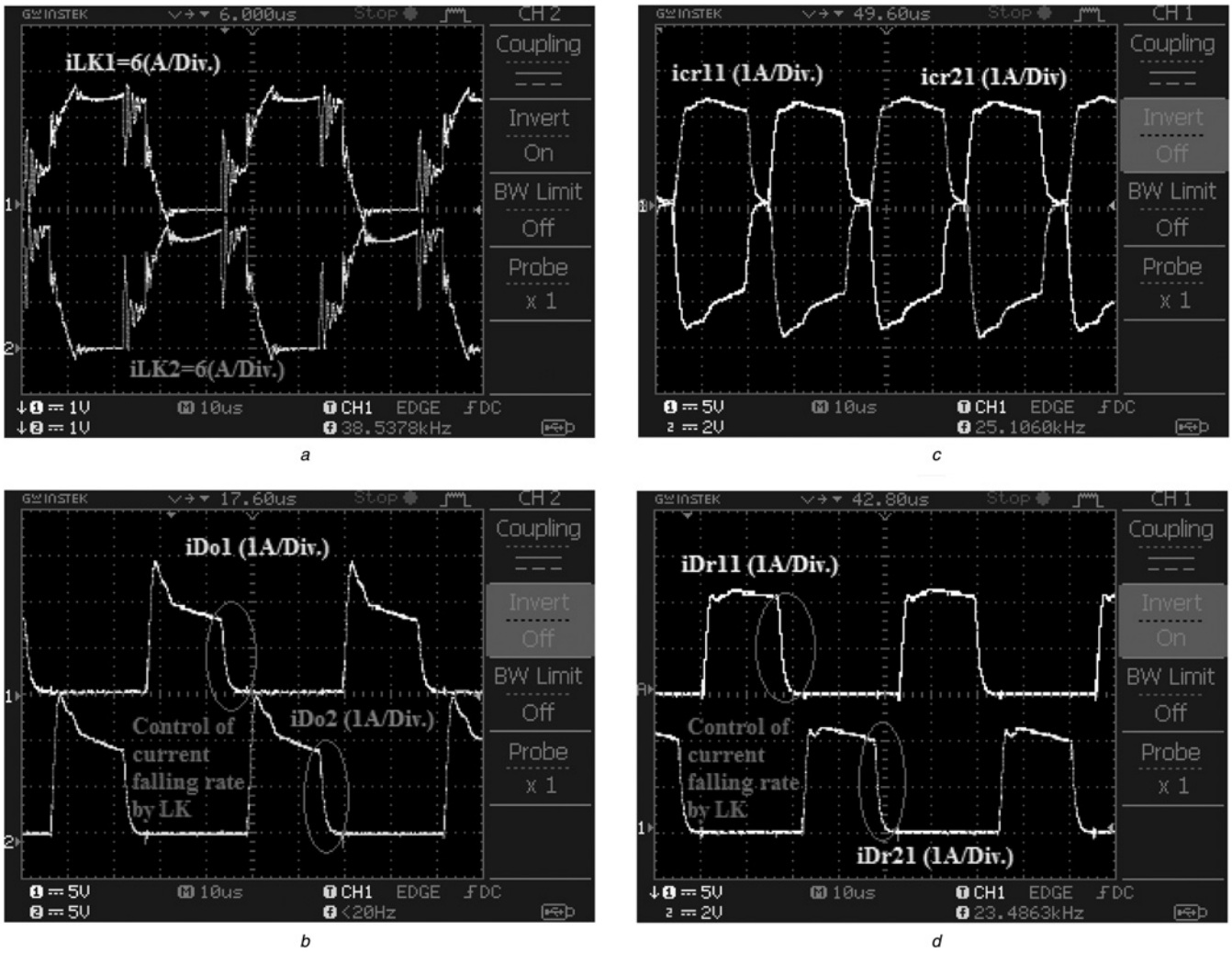


**Fig. 15** *Current measurements of the proposed converter under CCM (horizontal axis: 10 μS/Div.)*

(a) $i_{Lk1}$ and $i_{Lk2}$
(b) $i_{D_{o1}}$ and $i_{D_{o2}}$
(c) $i_{C_{r11}}$ and $i_{C_{r21}}$
(d) $i_{D_{r11}}$ and $i_{D_{r21}}$

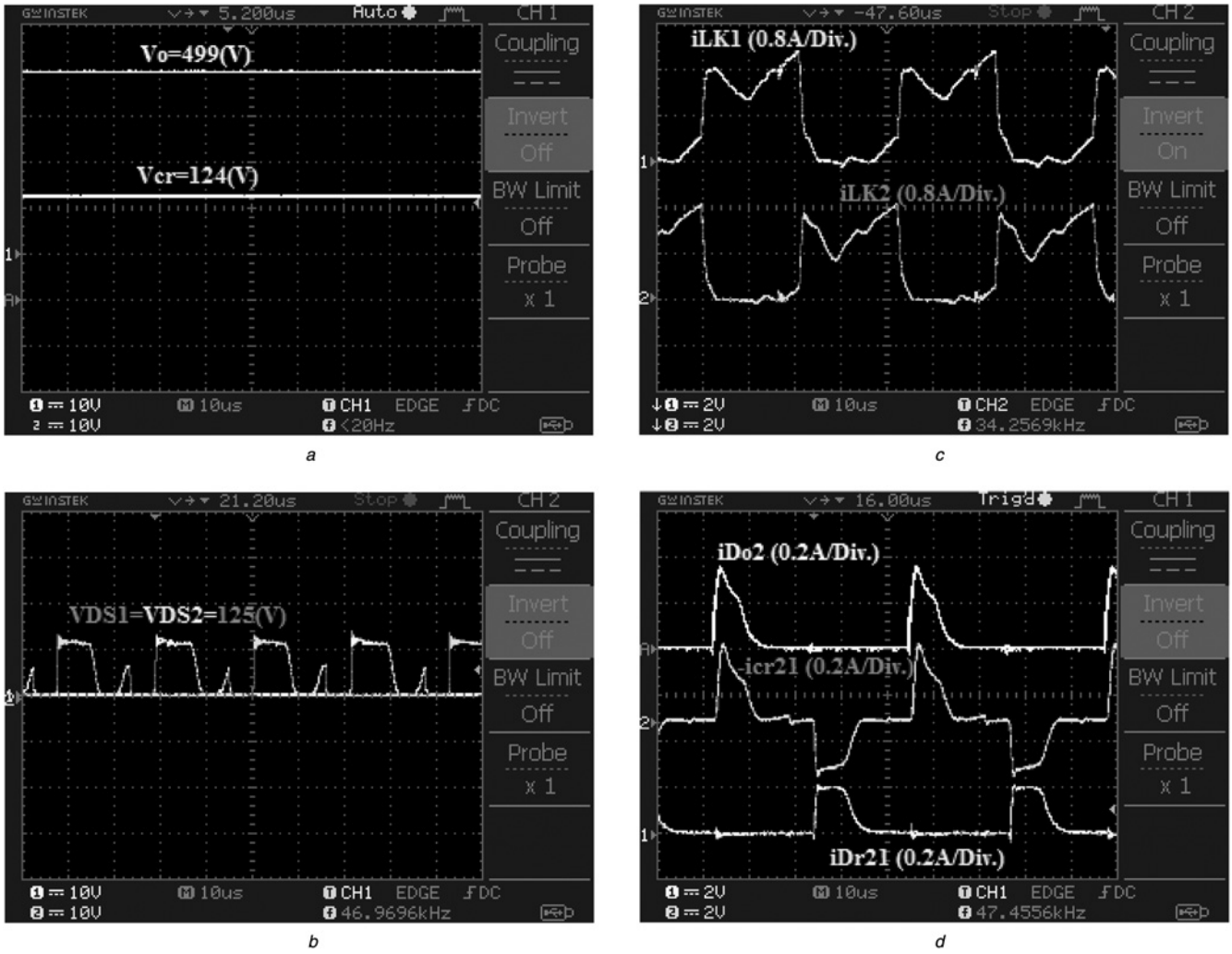


**Fig. 16** *Experimental results of the proposed converter under DCM condition [vertical axis for (a) and (b) 100 V/Div. (probe*10), horizontal axis: 10 μS/Div.]*

(a) $V_o$ and $V_{Cr}$
(b) $V_{DS1}$ and $V_{DS2}$
(c) $i_{Lk1}$ and $i_{Lk2}$
(d) $i_{Do2}$, $-i_{C_{r21}}$ and $i_{D_{r21}}$

performance can be seen from Fig. 15*a*. The ringing phenomenon in the results is because of resonance between the leakage inductors and parasitic capacitors of the power MOSFETs. It is clear from Figs. 15*b* and *d* that the current falling rate of output and regenerative diodes are controlled by leakage inductors that alleviate the reverse current recovery problem.

To achieve the DCM operating condition, the output load is increased to 13 kΩ. $\tau_L$ is obtained $= 0.59 \times 10^{-3}$ that is lower than the boundary value in Fig. 10 at $d = 0.615$. Then the converter operates under DCM. The input voltage is set at 20 V. According to (48), the voltage gain is obtained 26.86 that yields $V_o = 548$ V. According to (41) and (42), $V_{C_r} \cong 135$ V. Fig. 16 shows the experimental results of the proposed converter under DCM. As can be seen the mathematical analysis and experimental results match each other, fairly. It should be mentioned again here that the difference between the mathematical analysis and experimental results is because of the parasitic components that affect the voltage gain and were not taken into account in DCM voltage gain analysis.

**Table 5** Conversion efficiency and measured output voltage of the proposed converter under various load conditions

| Output power $P_o$, W | Output voltage $V_o$, V | Efficiency, % |
|---|---|---|
| 273 | 619 | 95.5 |
| 317 | 615.8 | 96.4 |
| 415 | 611 | 96.5 |
| 524 | 606 | 97 |
| 600 | 602.5 | 96.7 |
| 711 | 596.3 | 96.1 |
| 870 | 590 | 95.2 |

The measured efficiencies and output voltages of the proposed converter under various load conditions are given in Table 5. HIOKI 3256 DIGITAL HiTESTER (made in Japan), KYORITSU KEW MATE MODEL 2000 (made in Japan) and FUKE FK9205X DIGITAL MULTIMETER have been used for measurement of input and output powers, then the efficiency obtained as $\eta = P_o/P_{in} = (V_o I_o)/(V_{in} I_{in})$. As can be seen the proposed converter reaches the maximum efficiency of 97% at 524 W and the test condition efficiency at 870 W is 95.2%.




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## 7 Conclusion

An interleaved high step-up DC–DC converter based on three-winding high-frequency coupled inductor and VMCs has been presented in this paper. The voltage gain is extended and the extreme duty cycle can be avoided. The voltage across the MOSFET is low and then switches with lower on-state resistance can be adapted. Owing to presence of the leakage inductor of the coupled inductors, the ZCS is provided for semiconductor that alleviated the switching losses and diodes reverse recovery problems. The proposed converter was investigated in CCM, DCM and BCM regions. Also the theoretical efficiency of the proposed converter has been analysed and some comparisons in the terms of voltage gain, MOSFETs and diodes voltage stresses and components number has been provided between the proposed converter and the converters in the literature. Finally, in order to show the satisfying operation of the proposed converter an 870 W 60 V-input to 590 V-output laboratory prototype with 95.2% conversion efficiency has been provided. It was shown that the mathematical analysis and experimental results match each other, fairly.

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