New Three-Phase Multilevel Inverter With Reduced Number of Power Electronic Components

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***Abstract*—In this paper, a new configuration of a three-phase five-level multilevel voltage-source inverter is introduced. The proposed topology constitutes the conventional three-phase two-level bridge with three bidirectional switches. A multilevel dc link using fixed dc voltage supply and cascaded half-bridge is connected in such a way that the proposed inverter outputs the required output voltage levels. The fundamental frequency staircase modulation technique is easily used to generate the appropriate switching gate signals. For the purpose of increasing the number of voltage levels with fewer number of power electronic components, the structure of the proposed inverter is extended and different methods to determine the magnitudes of utilized dc voltage supplies are suggested. Moreover, the prototype of the suggested configuration is manufactured as the obtained simulation and hardware results ensured the feasibility of the configuration and the compatibility of the modulation technique is accurately noted.**

***Index Terms*—Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter.**

I. Introduction

MULTILEVEL inverters consist of a group of switching devices and dc voltage supplies, the output of which produces voltages with stepped waveforms. Multilevel technology has started with the three-level converter followed by numerous multilevel converter topologies. Different topologies and wide variety of control methods have been developed in the recent literature [1]–[3]. The most common multilevel inverter configurations are neutral point clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge (CHB). The deviating voltage of neutral-point voltage in NPC, the unbalanced voltage in the dc link of FC, and the large number of separated dc supplies in CHB are considered the main drawbacks of these topologies [4], [5]. Apart from these three main topologies, other topologies are introduced [6]–[17]. Recently, asymmetrical and hybrid multistage topologies are becoming one of the most interested research area. In the asymmetrical configurations, the magnitudes of dc voltage supplies are unequal. These topologies reduce the cost and size of the inverter and improve the reliability since minimum number of power electronic components, capacitors, and dc supplies are used. The hybrid multistage converters consist of different multilevel configurations with unequal dc voltage supplies. With such converters, different modulation strategies and power electronic components technologies are needed [18]–[26]. On the other hand, for the purpose of improving the performance of the conventional single- and three-phase inverters, different topologies employing different types of bidirectional switches have been suggested in [27]–[29]. Comparing to the unidirectional one, bidirectional switch is able to conduct the current and withstanding the voltage in both directions. Bidirectional switches with an appropriate control technique can improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels [30]–[34]. Based on this technical background, this paper suggests a novel topology for a three-phase five-level multilevel inverter. The number of switching devices, insulated-gate driver circuits, and installation area and cost are significantly reduced. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the high number of voltage level with an effective application of a fundamental frequency staircase modulation technique. Extended structure for N-level is also presented and compared with the conventional well-known multilevel inverters. Simulation and hardware results are given and explained.

II. Proposed Topology

Fig. 1(a) and (b) shows the typical configuration of the proposed three-phase five-level multilevel inverter. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of $4V_{\rm dc}$ and CHB having two unequal dc voltage supplies of $V_{\rm dc}$ and $2V_{\rm dc}$ are connected to (+, –, o) bridge terminals. Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are

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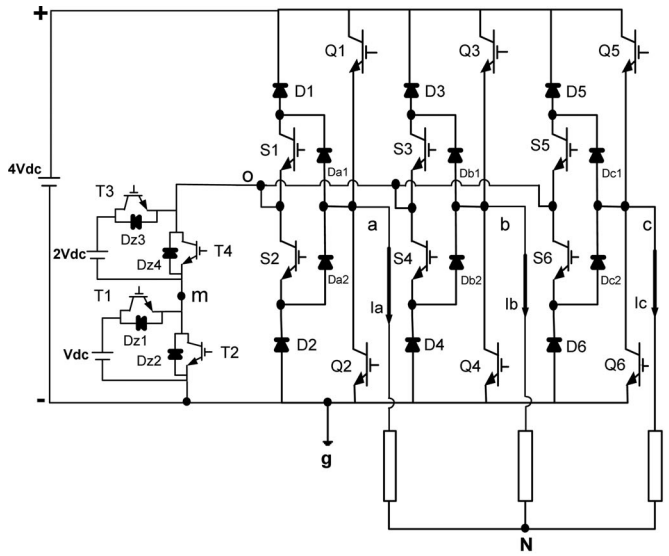
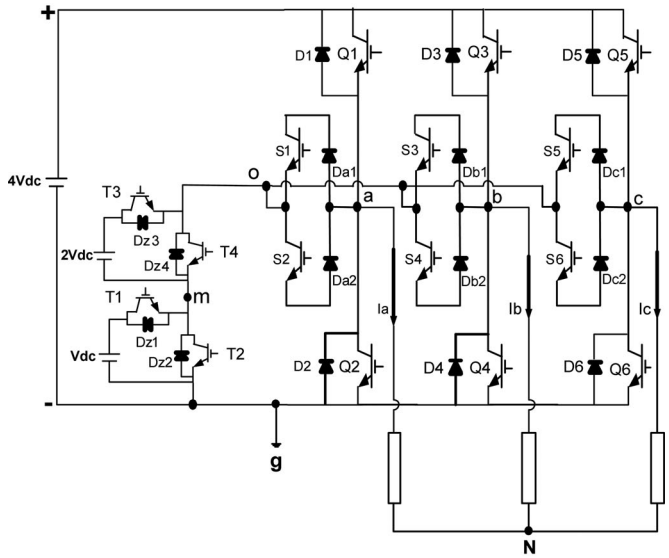


(a)



(b)

Fig. 1. Circuit diagram of the proposed three-phase five-level multilevel inverter.

turned ON and OFF under inverted conditions to output two different voltage levels. The first cell dc voltage supply $V_{\rm dc}$ is added if switch T1 is turned ON leading to $V_{\rm mg} = +V_{\rm dc}$ where $V_{\rm mg}$ is the voltage at node (m) with respect to inverter ground (g) or bypassed if switch T2 is turned ON leading to $V_{\rm mg} = 0$. Likewise, the second cell dc voltage supply $2V_{\rm dc}$ is added when switch T3 is turned ON resulting in $V_{\rm om} = +2V_{\rm dc}$ where $V_{\rm om}$ is the voltage at midpoint (o) with respect to node (m) or bypassed when switch T4 is turned ON resulting in $V_{\rm om} = 0$. The peak voltage rating of the switches of the conventional two-level bridge (Q1–Q6) is $4V_{\rm dc}$ whereas the bidirectional switches (S1–S6) have a peak voltage rating of $3V_{\rm dc}$. In CHB cells, the peak voltage rating of second cell switches (T3 and T4) is $2V_{\rm dc}$ while the peak voltage rating of T1 and T2 in the first cell is $V_{\rm dc}$. By considering phase a, the operating status of the switches and the inverter line-to-ground voltage $V_{\rm ag}$ are given in Table I.

TABLE I
Switching State *Sa* and Inverter Line-to-Ground Voltage $V_{\rm ag}$

Sa	Q1	S1	S2	Q2	T1	T2	T3	T4	*Vag*
4	on	off	off	off	on	off	on	off	*+4Vdc*
3	off	on	on	off	on	off	on	off	*+3Vdc*
2	off	on	on	off	off	on	on	off	*+2Vdc*
1	off	on	on	off	on	off	off	on	*+Vdc*
0	off	off	off	on	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages $V_{\rm ag}, V_{\rm bg}$, and $V_{\rm cg}$ in terms of switching states *Sa*, *Sb*, and *Sc* as

$$\begin{bmatrix} V_{\rm ag} \\ V_{\rm bg} \\ V_{\rm cg} \end{bmatrix} = \frac{4V_{\rm dc}}{N-1} * \begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} \tag{1}$$

where $N = 5$ is the maximum number of voltage levels.

The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The inverter may have 24 different modes within a cycle of the output waveform. According to Table II, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on-state. As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current $I_{\rm b}$ can flow in S3 and Db1 or S4 and Db2). Since some insulated-gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms $V_{\rm ab}, V_{\rm bc}$, and $V_{\rm ca}$ with corresponding switching gate signals are depicted in Fig. 2 where $V_{\rm ab}, V_{\rm bc}$, and $V_{\rm ca}$ are related to $V_{\rm ag}, V_{\rm bg}$, and $V_{\rm cg}$ by

$$\begin{bmatrix} V_{\rm ab} \\ V_{\rm bc} \\ V_{\rm ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} V_{\rm ag} \\ V_{\rm bg} \\ V_{\rm cg} \end{bmatrix}. \tag{2}$$

The inverter line-to-neutral voltages $V_{\rm aN}, V_{\rm bN}$, and $V_{\rm cN}$ may be expressed as

$$\begin{bmatrix} V_{\rm aN} \\ V_{\rm bN} \\ V_{\rm cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{\rm ag} \\ V_{\rm bg} \\ V_{\rm cg} \end{bmatrix}. \tag{3}$$

It is useful to recognize that the inverter voltages at terminals a, b, and c with respect to the midpoint (o) are given by

$$\begin{bmatrix} V_{\rm ao} \\ V_{\rm bo} \\ V_{\rm co} \end{bmatrix} = \begin{bmatrix} V_{\rm ag} \\ V_{\rm bg} \\ V_{\rm cg} \end{bmatrix} - \begin{bmatrix} V_{\rm og} \\ V_{\rm og} \\ V_{\rm og} \end{bmatrix} \tag{4}$$

where $V_{\rm og}$ is the voltage at midpoint (o) with respect to ground (g). $V_{\rm og}$ routinely fluctuates among three different voltage values $V_{\rm dc}$, $2V_{\rm dc}$, and $3V_{\rm dc}$ as follows:

$$V_{\rm og} = \begin{cases} V_{\rm dc}, & \text{if } Sa + Sb + Sc \le 5 \\ 2V_{\rm dc}, & \text{if } Sa + Sb + Sc = 6 \\ 3V_{\rm dc}, & \text{if } Sa + Sb + Sc \ge 7. \end{cases} \tag{5}$$

The simulated voltage waveforms of $V_{\rm ag}, V_{\rm og}, V_{\rm ao}$, and $V_{\rm aN}$ based on (1)–(5) are shown in Fig. 3 where, for instance, 13

TABLE II
SWITCHING STATES SEQUENCE OF THE PROPOSED INVERTER WITHIN ONE CYCLE

Sa Sb Sc	Period T [s]	ON switches Leg *a*	ON switches Leg *b*	ON switches Leg *c*	ON switches cascaded half-bridge	*Vag* [V]	*Vbg* [V]	*Vcg* [V]
400	t1	Q1	Q4	Q6	T1,T4	*4Vdc*	0	0
410	t2	Q1	S3, S4	Q6	T1,T4	*4Vdc*	*Vdc*	0
420	t3	Q1	S3, S4	Q6	T2,T3	*4Vdc*	*2Vdc*	0
430	t4	Q1	S3, S4	Q6	T1,T3	*4Vdc*	*3Vdc*	0
440	t5	Q1	Q3	Q6	T1,T3	*4Vdc*	*4Vdc*	0
340	t6	S1, S2	Q3	Q6	T1,T3	*3Vdc*	*4Vdc*	0
240	t7	S1, S2	Q3	Q6	T2,T3	*2Vdc*	*4Vdc*	0
140	t8	S1, S2	Q3	Q6	T1,T4	*Vdc*	*4Vdc*	0
040	t9	Q2	Q3	Q6	T1,T4	0	*4Vdc*	0
041	t10	Q2	Q3	S5, S6	T1,T4	0	*4Vdc*	*Vdc*
042	t11	Q2	Q3	S5, S6	T2,T3	0	*4Vdc*	*2Vdc*
043	t12	Q2	Q3	S5, S6	T1,T3	0	*4Vdc*	*3Vdc*
044	t13	Q2	Q3	Q5	T1,T3	0	*4Vdc*	*4Vdc*
034	t14	Q2	S3, S4	Q5	T1,T3	0	*3Vdc*	*4Vdc*
024	t15	Q2	S3, S4	Q5	T2,T3	0	*2Vdc*	*4Vdc*
014	t16	Q2	S3, S4	Q5	T1,T4	0	*Vdc*	*4Vdc*
004	t17	Q2	Q4	Q5	T1,T4	0	0	*4Vdc*
104	t18	S1, S2	Q4	Q5	T1,T4	*Vdc*	0	*4Vdc*
204	t19	S1, S2	Q4	Q5	T2,T3	*2Vdc*	0	*4Vdc*
304	t20	S1, S2	Q4	Q5	T1,T3	*3Vdc*	0	*4Vdc*
404	t21	Q1	Q4	Q5	T1,T3	*4Vdc*	0	*4Vdc*
403	t22	Q1	Q4	S5, S6	T1,T3	*4Vdc*	0	*3Vdc*
402	t23	Q1	Q4	S5, S6	T2,T3	*4Vdc*	0	*2Vdc*
401	t24	Q1	Q4	S5, S6	T1,T4	*4Vdc*	0	*Vdc*

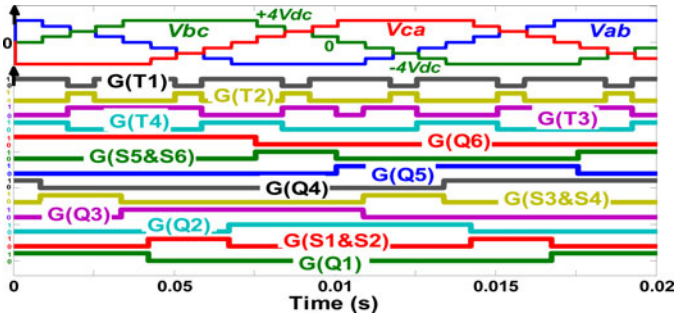


Fig. 2. Simulated waveforms of $V_{\rm ab}, V_{\rm bc}$, and $V_{\rm ca}$ with corresponding switching gate signals for the proposed inverter at fundamental frequency $f = 50$ Hz.

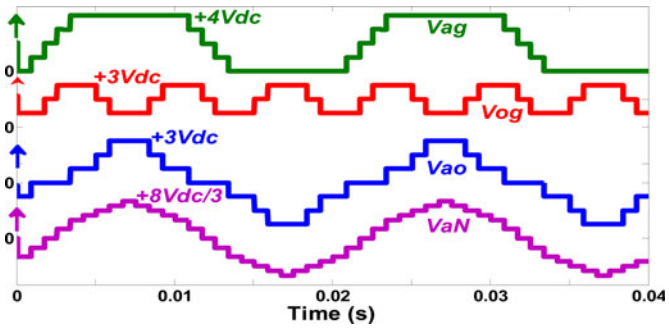


Fig. 3. Simulated waveforms of $V_{\rm ag}, V_{\rm og}, V_{\rm ao}$, and $V_{\rm aN}$ for the proposed inverter $f = 50$ Hz.

sequent voltage steps are seen in $V_{\rm aN}$ waveform as follows: $+8V_{\rm dc}/3$, $+7V_{\rm dc}/3$, $+6V_{\rm dc}/3$, $+5V_{\rm dc}/3$, $+4V_{\rm dc}/3$, $+2V_{\rm dc}/3$, 0, $-2V_{\rm dc}/3$, $-4V_{\rm dc}/3$, $-5V_{\rm dc}/3$, $-6V$dc/3, $-7V_{\rm dc}/3$, and $-8V_{\rm dc}/3$. It is worth noting that all simulated waveforms are obtained at $t_1 = t_2 = \cdots = t_{24} = 0.02/24$ s. In order to plot the space vector diagram of the proposed inverter in a stationary d–q reference frame, the following equations can be used to derive d and q voltage components for all inverter vectors:

$$V_q = \frac{4V_{\rm dc}}{3(N-1)}(2Sa - Sb - Sc) \tag{6}$$

$$V_d = \frac{4V_{\rm dc}}{\sqrt{3}(N-1)}(Sc - Sb) \tag{7}$$

$$V = V_q - jV_d. \tag{8}$$

For all switching states presented in Table II, Fig. 4 shows the space vector diagram for the proposed topology.

III. SWITCHING ALGORITHM

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms. An iterative method such as the Newton–Raphson method is normally used to find the solutions to $(N–1)$ nonlinear transcendental equations. The difficult calculations and the need of high-performance controller for the real application are the main disadvantages of such method. Therefore, an alternative method is proposed to generate the inverter's switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of *Sa*, *Sb*, and *Sc*. The basis of the proposed method can be explained as following: For a given value of modulation index M_a and within a full cycle of

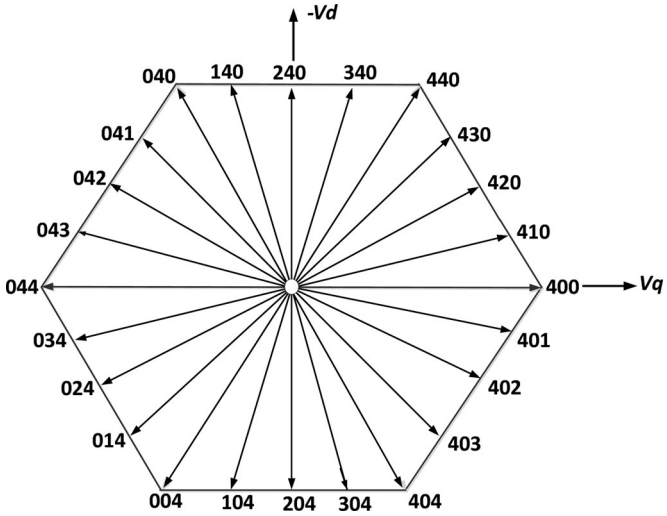


Fig. 4. Switching states vectors of the proposed inverter in *d–q* reference frame.

the operation of the proposed inverter, the switching states *Sa*, *Sb*, and *Sc* are determined instantaneously. The on-time calculations of *Sa*, *Sb*, and *Sc* directly depend on the instantaneous values of the inverter line-to-ground voltages. It is well known that the reference values of $V_{\rm ag}$, $V_{\rm bg}$, and $V_{\rm cg}$ are normally given by

$$\begin{bmatrix} V_{\rm ag\_ref} \\ V_{\rm bg\_ref} \\ V_{\rm cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{\rm dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos\left(wt - \frac{2\pi}{3}\right) \\ \cos\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{\rm dc}}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \tag{9}$$

where *wt* is the electrical angle. Or

$$\begin{bmatrix} V_{\rm ag\_ref} \\ V_{\rm bg\_ref} \\ V_{\rm cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{\rm dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos\left(wt - \frac{2\pi}{3}\right) \\ \cos\left(wt + \frac{2\pi}{3}\right) \end{bmatrix} + \frac{4V_{\rm dc}}{2} * \left[1 - \frac{M_a}{6}\cos(3wt)\right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix}. \tag{10}$$

From (10), it can be noticed that the third harmonic component is added to the three-line-to-ground voltages. The third harmonic injection may increase the inverter fundamental voltage without causing overmodulation. As a result, M_a can reach to 1.15 and *Sa*, *Sb*, and *Sc* can be simply determined by integerzing the reference line-to-ground voltages as

$$\begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix} = \text{integer}\left(\frac{N-1}{4V_{\rm dc}} * \begin{bmatrix} V_{\rm ag\_ref} \\ V_{\rm bg\_ref} \\ V_{\rm cg\_ref} \end{bmatrix}\right). \tag{11}$$

Comparison of the proposed modulation method with the staircase modulation with the selective harmonic method shows that the proposed modulation features less time and needs simple calculations. The inverter's operating switching states *Sa*, *Sb*, and *Sc* and corresponding switching gate signals based on the proposed modulation method are shown in Fig. 5. It is clear

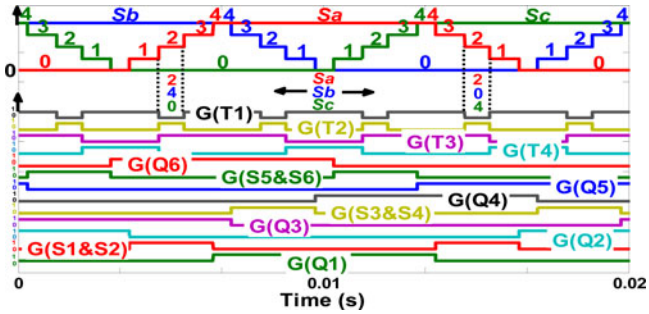


Fig. 5. Inverter's operating switching states *Sa*, *Sb*, and *Sc* with corresponding switching gate signals based on the proposed modulation method.

TABLE III
SWITCHING STATE *Sa*1 AND INVERTER LINE-TO-GROUND VOLTAGE $V_{\rm ag}$ AT $M_a < 0.9$ (LEG *a*)

Sa1	Q1	S1	S2	Q2	T1	T2	T3	T4	*Vag*
2	on	off	off	off	off	on	on	off	*+4Vdc*
1	off	on	on	off	off	on	on	off	*+2Vdc*
0	off	off	off	on	off	on	on	off	*0*

that the switching gate signals are generated within 24 different modes starting from (044) to (034).

Since the proposed inverter has been designed to achieve five voltage levels, the modulation index must be within range $0.9 \le M_a \le 1.15$. For modulation index $M_a < 0.9$, only two dc voltage supplies $4V_{\rm dc}$ and $2V_{\rm dc}$ are utilized and the behavior of the proposed inverter becomes similar to the three-level multilevel inverter. Using (9)–(11) and substituting $N = 3$, the inverter's operating switching states *Sa*, *Sb*, and *Sc* at $M_a < 0.9$ can be defined. The operation principle of the proposed inverter at $M_a < 0.9$ is illustrated in Table III. Fig. 6(a) and (b) shows the inverter line-to-line voltage waveforms at five different modulation indices including the overmodulation operation $M_a = 0.8$, 0.9, 1.05, 1.15, and 1.3.

IV. EXTENDED STRUCTURE

It is noticeable that there is possibility to reach an output voltage with higher number of steps in the proposed multilevel inverter by extending the CHB circuit. Such extending can be done by adding more half-bridge cells connected in series as shown in Fig. 7(a) and (b). In order to achieve the desired number of voltage levels, three methods can be followed to determine the magnitudes of utilized dc voltage supplies.

1) All cells have an equal dc supply in magnitude.

$$V_{\rm dc1} = V_{\rm dc2} = \cdots = V_{\rm dcn} = V_{\rm dc}. \tag{12}$$

Then, the magnitude of fixed dc supply can be chosen as

$$V_{\rm fix} = (N-1)V_{\rm dc} = (1+n)V_{\rm dc} \tag{13}$$

where n is the number of utilized cells. The maximum number of voltage steps is related to the number of utilized cells by

$$N = n + 2. \tag{14}$$

The number of operation modes that makes the switching states sequence achieves the required output voltage waveform

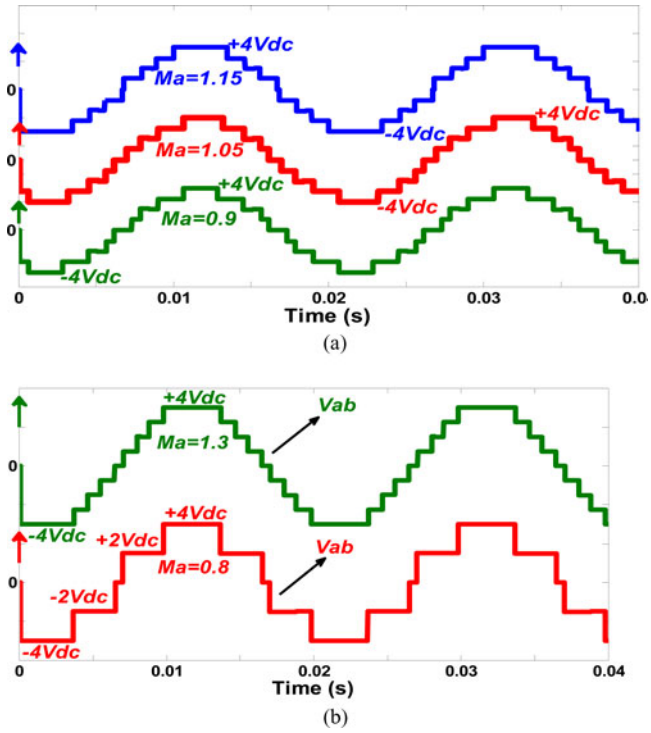


Fig. 6. Simulated waveforms of V_{ab} at different modulation indices for the proposed inverter: (a) $M_a = 0.9$, 1.05, and 1.15 and (b) $M_a = 0.8$ and 1.3.

can be expressed as

$$M = 6(N-1). \tag{15}$$

2) The magnitude of dc voltage supply used in each and every cell in a particular inverter is obtained as follows:

$$V_{\mathrm{dc1}} = V_{\mathrm{dc}} \tag{16}$$

$$V_{\mathrm{dc2}} = 2V_{\mathrm{dc}} \tag{17}$$

$$V_{\mathrm{dcn}} = nV_{\mathrm{dc}} \tag{18}$$

$$V_{\mathrm{fix}} = (N-1)V_{\mathrm{dc}} = \left[1 + \frac{n(n+1)}{2}\right] V_{\mathrm{dc}} \tag{19}$$

$$N = 2 + \frac{n(n+1)}{2} \tag{20}$$

$$M = 6(N-1). \tag{21}$$

3) By making a binary (power of 2) relationship between the dc supplies of the CHB structure as follows:

$$V_{\mathrm{dc1}} = 2^{(0)}(V_{\mathrm{dc}}) \tag{22}$$

$$V_{\mathrm{dc2}} = 2^{(1)}(V_{\mathrm{dc}}) \tag{23}$$

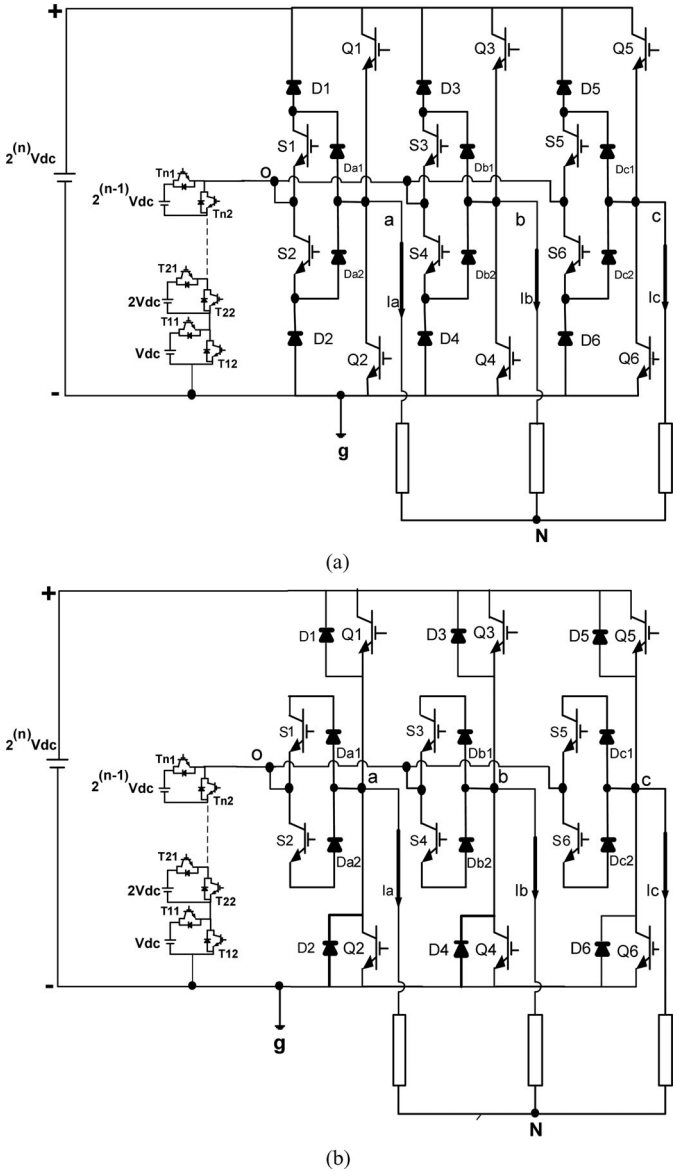


Fig. 7. Circuit diagram of the proposed three-phase N-level multilevel inverter (third method).

$$V_{\mathrm{dcn}} = 2^{(n-1)}(V_{\mathrm{dc}}) \tag{24}$$

$$V_{\mathrm{fix}} = (N-1)V_{\mathrm{dc}} = \left[1 + \sum_{\mathrm{j}=1}^{n} 2^{j-1}\right] V_{\mathrm{dc}} = (2^n)V_{\mathrm{dc}} \tag{25}$$

$$N = 1 + 2^n \tag{26}$$

$$M = 6(N-1). \tag{27}$$

Table IV illustrates some characteristics of the proposed methods.

TABLE IV
COMPARISON OF THE MAXIMUM NUMBER OF VOLTAGE LEVELS WITH THE REQUIRED VALUE OF DC VOLTAGE SUPPLIES AMONG THE PROPOSED METHODS

Number of cells	1st method			2nd method			3rd method		
n	*N*	*M*	*Vfix*	*N*	*M*	*Vfix*	*N*	*M*	*Vfix*
2	4	18	*3Vdc*	5	24	*4Vdc*	5	24	*4Vdc*
3	5	24	*4Vdc*	8	42	*7Vdc*	9	48	*8Vdc*
4	6	30	*5Vdc*	12	66	*11Vdc*	17	96	*16Vdc*
5	7	36	*6Vdc*	17	96	*16Vdc*	33	192	*32Vdc*
6	8	42	*7Vdc*	23	132	*22Vdc*	65	384	*64Vdc*

Based on the comparison carried among the proposed methods, the following are some observations.

1) Comparing to the second and third methods, the first method has a high modularity degree since the symmetric structure of CHB makes use of equal dc voltage supplies. This method helps the proposed inverter to reach all maximum number of voltage levels (4, 5, 6, 7, 8,. . .,N).
2) Since the second and third methods use the asymmetrical structure of CHB, the proposed inverter can reach the required output voltage and the maximum number of voltage levels such as 5, 8, 9, 12, 17,. . . with less number of dc voltage supplies and power electronic components.

V. COMPARISON STUDY

In order to investigate the capability of the suggested configuration, the proposed inverter is compared with different types of multilevel inverters such as NPC, FC, and CHB. It is evident that the suggested three-phase N-level multilevel inverter can considerably minimize the required number of power components. For the same number of output voltage levels ($N \geq 4$), Table V explains the required number of dc voltage supplies, switches, clamping diodes, control signals, and balancing capacitors of the proposed N-level inverter compared with three existing inverters NPC, FC, and CHB. As shown in Fig. 8, it can be noticed that nearly more than two-thirds of number of switches can be counted out as N increases. For instance, at the same number of voltage levels $N = 17$, and compared with the existing multilevel inverters which require 96 switches, the required number of switches for the proposed inverter is less since it requires 42 switches based on the first method, 22 switches based on the second method, and 20 switches based on the third method. On the other hand, it is well known that the voltage and current ratings of the power components have an effect on the cost and realization of the multilevel inverter. Assuming that all power components have an equal current rating which is the rated current of the load (*IL*), the voltage ratings of these components depend on the magnitude of dc voltage supplies, voltage stress, and structure of the inverter. Considering that all inverters have the same input dc link which equals $(N–1)V_{\rm dc}$, Table VI illustrates the rating requirements for the proposed inverter comparing with the rating requirements for the existing inverters. It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are involved, the semiconductor devices expenses are considerably recovered.

VI. POWER CONVERSION EFFICIENCY AND TOTAL HARMONIC DISTORTION (THD%)

In order to determine the efficiency of the proposed inverter, it is necessary to determine the value of conduction and switching power losses generated by the semiconductor components. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: conduction loss ($P_{\rm con}$) and switching loss ($P_{\rm sw}$) as follows:

$$P_{\rm sw\_IGBT} = \frac{1}{T}\int_0^T E_{\rm on}(t)dt + \frac{1}{T}\int_0^T E_{\rm off}(t)d(t) \quad (28)$$

$$P_{\rm sw\_diode} = \frac{1}{T}\int_0^T E_{\rm rr}(t)dt \quad (29)$$

where $E_{\rm on}(t)$ is a turn-on loss and $E_{\rm off}(t)$ is a turn-off loss. Switching losses $E_{\rm on}(t)$ and $E_{\rm off}(t)$ are experienced during the ON and OFF states, respectively. While $E_{\rm rr}(t)$ is the reverse recovery loss of the diode, the majority of switching loss, which is experienced when the diode is turned OFF (OFF state)

$$P_{\rm con\_IGBT} = \frac{1}{T}\int_0^T V_{\rm on\_IGBT} i(t)dt \quad (30)$$

$$P_{\rm con\_Diode} = \frac{1}{T}\int_0^T V_{\rm on\_diode} i(t)dt. \quad (31)$$

Conduction power losses of IGBT and diode are approximated based on their forward voltage drops $V_{\rm on\_IGBT}$, $V_{\rm on\_diode}$, and the instantaneous current $i(t)$ flowing through IGBT or diode. The total losses P_t are expressed as follows:

$$P_t = P_{\rm con} + P_{\rm sw}\,. \quad (32)$$

Once the total semiconductors losses P_t in the introduced inverter are defined, the relative inverter efficiency is determined based on the following expression:

$$\eta\% = \frac{P_{\rm out}}{P_t + P_{\rm out}} \times 100. \quad (33)$$

Table VII provides the possible current directions with corresponding conducting devices in phase a.

MATLAB/Simulink model of the proposed inverter shown in Fig. 1 has been developed to study the conduction and switching power losses. The proposed inverter is designed to deliver output power of $P_{\rm out} = 1.9$ kW. Three-phase series resistive–inductive (23 Ω–3 mH/Phase) in star connection is used as load. The multilevel dc link is determined as $V_{\rm dc} = 75$ V, $2V_{\rm dc} = 150$ V, and $V_{\rm fix} = 4V_{\rm dc} = 300$ V and the proposed staircase modulation technique at $M_a = 1$ is implemented to generate the appropriate switching gate signals. Three different types of semiconductor components are selected to build the prototype of the proposed inverter power circuit as following: IGBT (HGTG20N60B3D) 600 V/40 A for the two-level bridge and CHB switches, IGBT (IRG4BC40W) 600 V/20 A for bidirectional switches, and Diode (RHRP1540) 400 V/15 A for embedded diodes in

TABLE V
COMPARISON OF THE PROPOSED N-LEVEL INVERTER WITH THE EXISTING INVERTERS

Converter type	NPC	FC	CHB	Proposed		
				1st method	2nd method	3rd method
Switches	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Gate drivers	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$
Diodes	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+10$	$\sqrt{8N-15}+11$	$2Log_2(N-1)+12$
Clamping diodes	$6(N-2)$	0	0	0	0	0
DC supplies	$N-1$	$N-1$	$3(N-1)/2$	$N-1$	$1+[(\sqrt{8N-15}-1)/2]$	$1+Log_2(N-1)$
Clamping capacitors	0	$3(N-2)$	0	0	0	0
Control signals	$6(N-1)$	$6(N-1)$	$6(N-1)$	$2(N-1)+7$	$\sqrt{8N-15}+8$	$2Log_2(N-1)+9$

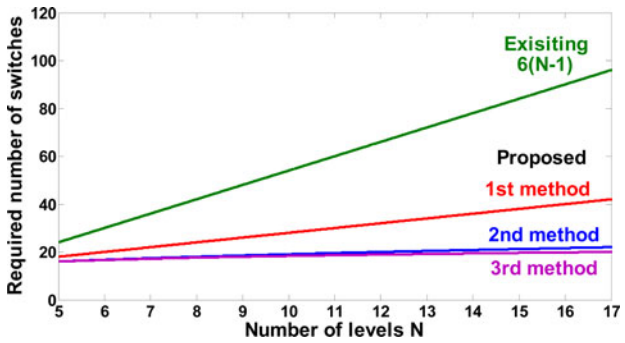


Fig. 8. Comparison of required number of switches among existing inverters and the proposed topology.

bidirectional switches and freewheeling diodes. The datasheets of the utilized semiconductor components are easily accessed to acquire their characteristics curves. To simplify the losses calculation, a curve-fitting tool of MATLAB is used to approximate these curves by exponential equations [35]. The mathematical models obtained for HGTG20N60B3D 600 V/40 A are given by

$$V_{\text{on\_IGBT1}} = 1.418e^{0.016i(t)} \tag{34}$$

$$E_{\text{on\_IGBT1}} = (201.6e^{0.04418i(t)} - 291.6e^{-0.1265i(t)}) \times 10^{-6} \tag{35}$$

$$E_{\text{off\_IGBT1}} = (323.9e^{0.05125i(t)}) \times 10^{-6}. \tag{36}$$

While the mathematical models obtained for IRG4BC40W 600 V/20 A are given by

$$V_{\text{on\_IGBT2}} = 1.555e^{0.0085371i(t)} \tag{37}$$

$$E_{\text{sw\_IGBT2}} = (0.3405e^{0.04472i(t)}) \times 10^{-3}. \tag{38}$$

And finally, the mathematical models obtained for RHRP1540 400 V/15 A are given by

$$V_{\text{on\_diode}} = 1.325e^{0.006424i(t)} - 0.8571e^{-0.07183i(t)} \tag{39}$$

$$E_{\text{rr\_diode}} = (15.7e^{-0.002733i(t)} + 2.74e^{-0.1413i(t)} - 3.162e^{-0.05923i(t)} - 8e^{-0.09452}) \times 10^{-6}. \tag{40}$$

Therefore, the conduction and switching power losses for the inverter switches and diodes can be estimated by substituting (34)–(40) into (28)–(33). The efficiency of the proposed inverter is estimated while the input voltage is raised in small steps. Fig. 9(a) depicts the estimated value of efficiency over a wide range of the output power. It is clear that the inverter's efficiency varies directly proportional to the output power and reaches its maximum value of 96.53% at 1.9 kW. It is a result of more power being effectively transferred with respect to the power losses. Furthermore, the power losses distribution among the inverter's legs and the CHB cells are shown in Fig. 9(b). The power losses distribution is obtained during the operation of the proposed inverter to deliver $P_{\text{out}} = 1.287$ kW at voltage step $V_{\text{dc}} = 62.5$ V, $2V_{\text{dc}} = 125$ V, and $V_{\text{fix}} = 4V_{\text{dc}} = 250$ V. The power losses generated by legs a, b, and c are almost equal and slightly higher than those generated by CHB cells. According to Fig. 9(b), 53.3% of the total value of power loss is experienced in the conventional two-level bridge since 3×9.92 W in term of conduction power losses is generated by Q1–Q6. It is definitely due to fact that the conduction power loss is directly proportional to the switch conduction time and the value of conducting current (for instance, Q1 and Q2 conduct the load current in 18 modes). Negligible conduction power losses are generated by the free whiling diodes (D1–D6). Further measurements show that $9.68 + 2.2$ W is the estimated value of the conduction power losses generated by CHB's switches and diodes. It is almost 21.3% of total power loss. The higher conduction power loss is experienced in T3 followed by T1, T4, and T2. The three bidirectional switches contribute to 19.6% of the total power loss as 3×3.66 W is the estimated value of conduction power loss generated by S1–S6 and Da1–Dc2. Finally, it can be observed that a negligible switching loss is generated since the fundamental frequency is implemented. Furthermore and in order to assess the performance of the proposed inverter comparing with other type of the multilevel inverter, a five-level NPC multilevel inverter built by IRG4BC40W 600 V/20 A and RHRP1540 400 V/15 A semiconductor component types has been modeled and operated under the same conditions to the proposed inverter. The estimated value of efficiency and power losses distribution of the NPC multilevel inverter are shown in Fig. 9(c) and (d). Comparison of the proposed inverter' efficiency with the five-level NPC multilevel inverter's efficiency shows that the proposed inverter has a higher efficiency since the

TABLE VI
PROPOSED AND THE EXISTING TOPOLOGIES RATING REQUIREMENTS PER LEVEL N

Proposed inverter	Main bridge Q1 ~ Q6 D1a ~D2c	Bidirectional switches S1 to S6 D1 to D6	Cascaded half-bridge switches T11 to Tn2			Converter type	NPC	FC	CHB
			1st method	2nd method	3rd method	switches voltage rating	*Vdc*	*Vdc*	*Vdc*
Component voltage rating	(*N*-1)*Vdc*	(*N*-2) *Vdc*	*Vdc*	*nVdc*	$2^{(n-1)}$ *Vdc*	Clamping diode voltage rating	*Vdc*	0	0
						Clamping capacitor voltage rating	0	*Vdc*	0
Active Component current	*IL*	*IL*	*IL*	*IL*	*IL*	Active component current	*IL*	*IL*	*IL*

TABLE VII
CONDUCTING DEVICES OF THE PROPOSED INVERTER PHASE a

Current	Conducting Devices Phase *a*. Fig. 1(a)	*Vag*	Conducting Devices Phase *a*. Fig. 1(b)	*Vag*
Ia > 0	Q1	+4*Vdc*	Q1	+4*Vdc*
	T1, T3, S2, Da2	+3*Vdc*	T1, T3, S2, Da2	+3*Vdc*
	Dz2, T3, S2, Da2	+2*Vdc*	Dz2, T3, S2, Da2	+2*Vdc*
	T1, Dz4, S2, Da2	+*Vdc*	T1, Dz4, S2, Da2	+*Vdc*
	D2, Da2	0	D2	0
Ia < 0	D1, Da1	+4*Vdc*	D1	+4*Vdc*
	Dz1, Dz3, S1, Da1	+3*Vdc*	Dz1, Dz3, S1, Da1	+3*Vdc*
	T2, Dz3, S1, Da1	+2*Vdc*	T2, Dz3, S1, Da1	+2*Vdc*
	Dz1, T4, S1, Da1	+*Vdc*	Dz1, T4, S1, Da1	+*Vdc*
	Q2	0	Q2	0

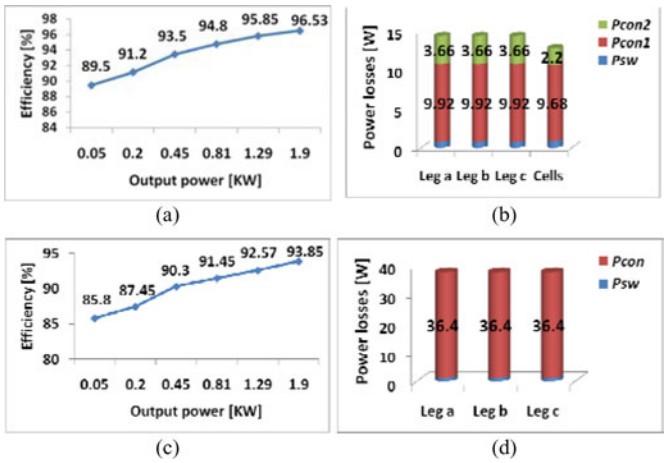


Fig. 9. Power loss and efficiency comparison. For the proposed inverter: (a) output power versus efficiency, (b) $P_{\rm con}$ and $P_{\rm sw}$ distribution among legs a, b, c, and CHB cells for $M_a = 1$ and $P_{\rm out} = 1.287$ kW. For the NPC inverter: (c) output power versus efficiency and (d) $P_{\rm con}$ and $P_{\rm sw}$ distribution among legs a, b, and c for $M_a = 1$ and $P_{\rm out} = 1.285$ kW.

maximum estimated efficiency of the NPC multilevel inverter is 93.85%. The lower P_t generated by the proposed inverter comparing with P_t generated by the five-level NPC multilevel inverter is a result of the low conduction power losses and reduced number of power components. A lower voltage stress leads to a lower switching power loss. However, the more the switching devices, the higher the conduction power losses. At the same operating point $P_{\rm out} \approx 1.287$ kW and compared with the estimated value of $P_{t\_\rm proposed} = 3 \times 14.4 + 12.78 \approx 55.9$ W generated by the proposed inverter, the estimated value of P_t

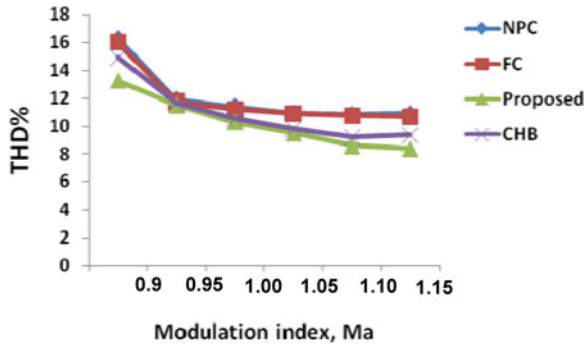


Fig. 10. NPC, FC, CHB, and proposed inverter: line-to-line voltage THD% versus M_a.

generated by the NPC multilevel inverter is two times higher. It is nearly $P_{t\_\rm NPC} = 3 \times 37.5 \approx 112.5$ W.

Moreover, the proposed inverter has been tested under different modulation indices ($M_a = 0.9$, 1, and 1.15). THD% of the output voltage can be calculated by

$$\text{THD\%} = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} \times 100\% \tag{41}$$

where V_1 and V_k are the fundamental component and harmonic order, respectively. NPC, FC, and CHB multilevel inverters have been tested under the same operating conditions. The goal of this test is to compare the proposed inverter with the existing inverters in term of THD%. Fig. 10 depicts THD% of the line-to-line voltage for all inverters within specific range of modulation indices [0.9–1.15]. It can be seen that the THD% of all inverter is slightly different. The measured values of THD% for the proposed inverter are within a range of 8.4–13.25%. As a result, the proposed inverter essentially adds the attractive aspects of the traditional two-level inverter such as less power components, simple working principle, and minimum conduction power loss to the main advantages of the multilevel inverter such as low THD% and high output voltage quality.

VII. EXPERIMENTAL RESULTS

To ensure the feasibility of the proposed topology, the inverter was implemented and its prototype has been manufactured. During the hardware implementation, the inverter shown in Fig. 1 was tested under $V_{\rm dc} = 22.5$ V in the first cell and $2V_{\rm dc} =$

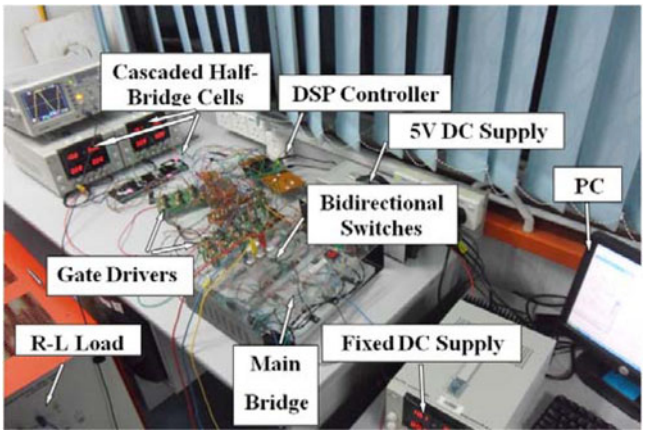


Fig. 11. Prototype of the proposed multilevel inverter.

TABLE VIII
SPECIFICATIONS OF THE SEMICONDUCTORS

Six-switch bridge IGBTs (Q1 ~ Q6)	HGTG20N60B3D, 40A, 600V
half-bridge cells IGBTs (T1 ~ T4)	HGTG20N60B3D, 40A, 600V
Bidirectional switches IGBTs (S1 ~ S6)	IRG4BC40W, 20A, 600V
Diodes	RHRP1540, 15A, 400V

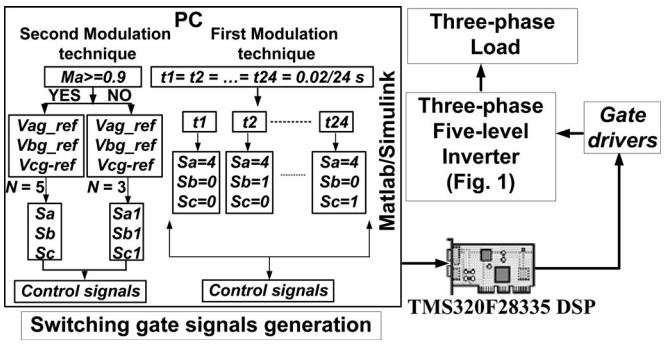


Fig. 12. Control block diagram.

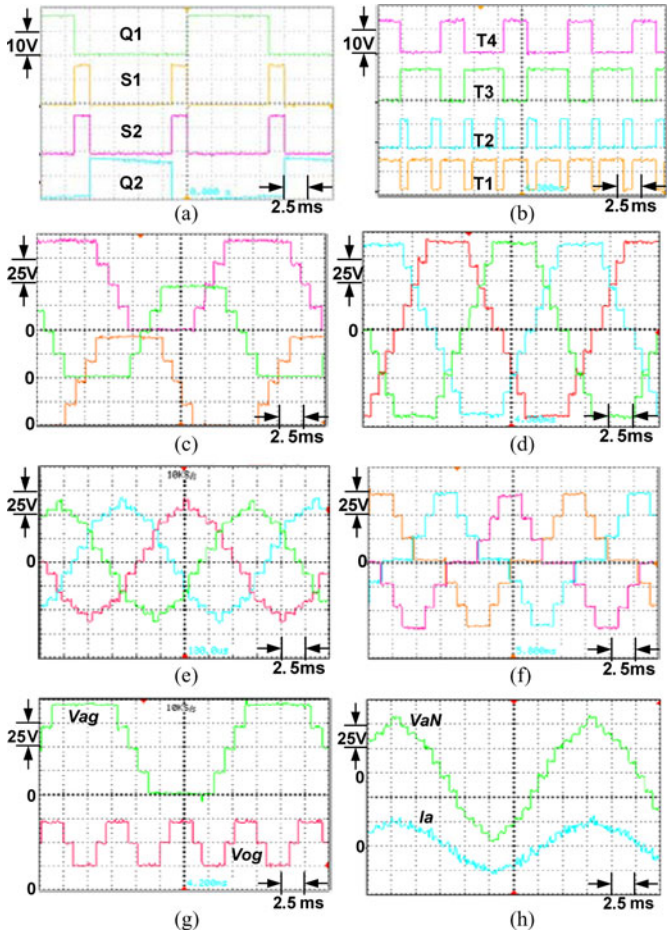


Fig. 13. (a) Switching gate signals of Q1, S1, S2, and Q2, (b) switching gate signals of T1, T2, T3, and T4, (c) three-line-to-ground voltages, (d) three-line-to-line voltages, (e) three-line to neutral voltages, (f) three-line to midpoint voltages, (g) midpoint to ground and line-to-ground voltages, and (h) load current I_a and line-to-neutral voltage V_{aN}.

45 V in the second cell. The magnitude of the fixed dc supply is determined as $V_{\mathrm{fix}} = 4V_{\mathrm{dc}} = 90$ V. Fixed three-phase series resistive–inductive load (23Ω–3 mH/Phase) in star connection was used. For the purpose of generating the appropriate switching gate signals, a DSP controller was used. The fundamental frequency $f = 50$ Hz staircase modulation technique was employed. In Fig. 11, the prototype of the proposed inverter is shown. It consists of the following components: personal computer, TMS320F28335 DSP controller, fixed dc voltage supply, conventional six-switch bridge, three bidirectional switches, two half-bridge cells, 13 gate drivers powered by 5 V dc supply, and fixed three-phase $(R - L)$ load. The type of semiconductors used for the power circuit is provided in Table VIII. Two modulation techniques are implemented to operate the proposed inverter as illustrated in the control block diagram (see Fig. 12). In the first modulation technique, the generation principle of the switching gate signals depends on time duration presented in Table II, where the time duration of a cycle of the output waveform ($t = 1/50 = 0.02$ s) is divided into 24 equal time periods: t_1=$t_2 = \cdots t_{24} = 0.02/24$ s. During each period, the proposed inverter' switches are turned ON/OFF following the switching sequence illustrated in Table II.

In Fig. 13(a) and (b), there is an illustration of the switching gate signals of the four switches (Q1, S1, S2, and Q2) in leg a of the main bridge and the four switches (T1, T2, T3, and T4) in the CHB circuit. The shapes of switching gate signals of switches in legs b and c are similar to those shown in Fig. 13(a) but they are shifted by 0.02/3 and 0.04/3 s, respectively. The operating frequencies f_{sw} of the proposed inverter' switches can be determined by means of the number of pulses per cycle as following: Q1–Q6 of the conventional bridge are turned ON/OFF at $f_{\mathrm{sw}} = f = 50$ Hz, while the bidirectional switches (S1–S6) are turned ON/OFF at $f_{\mathrm{sw}} = 2f = 100$ Hz. $f_{\mathrm{sw}} = 6f = 300$ Hz and $f_{\mathrm{sw}} = 4f = 200$ Hz are the operating frequency of the first cell switches T1 and T2 and the second cell switches T3 and T4, respectively. Fig. 13(c) depicts the inverter line-to-ground voltages V_{ag}, V_{bg}, and V_{cg}. It is clear that the controller manages to generate the appropriate switching gate signals that lead the inverter to output the desired waveform with five voltage steps. The inverter line-to-line voltages V_{ab}, V_{bc}, and V_{ca} waveforms with nine levels and the inverter line–to-neutral voltages V_{aN}, V_{bN}, and V_{cN}

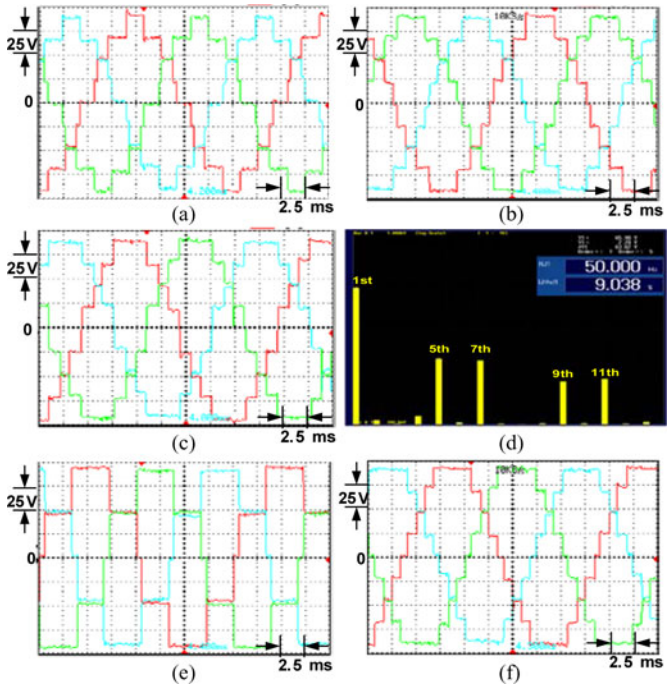


Fig. 14. (a) Three-line-to-line voltages at $M_a = 0.9$, (b) three-line-to-line voltages at $M_a = 1.05$, (c) three-line-to-line voltages at $M_a = 1.15$, (d) THD% at $M_a = 1.15$, (e) three-line-to-line voltages at $M_a = 0.8$, and (f) three-line-to-line voltages at $M_a = 1.3$.

waveforms with 13 levels are shown in Fig. 13(d) and (e), respectively. In Fig. 13(f), the inverter terminal voltages $V_{\rm ao}, V_{\rm bo}$, and $V_{\rm co}$ reached their maximum value $3V_{\rm dc}$ with seven voltage steps as designed. Based on shapes of $V_{\rm ag}$ and $V_{\rm og}, V_{\rm og}$ takes three different voltage values and it repeats itself three times within a full cycle of $V_{\rm ag}$ as shown in Fig. 13(g). In Fig. 13(h), the experimental waveforms of load current and line-to-neutral voltage of phase a are shown.

In order to investigate the performance of the proposed inverter at different modulation indices, the modulation technique presented in Section III is implemented. The proposed configuration was tested under different modulation indices $M_a =$ 0.9, 1, and 1.15. Fig. 14(a), (b), and (c) shows the inverter balanced line-to-line voltage waveforms. These voltage waveforms are similar to those obtained through simulation in Section III. THD% and the harmonic content of the line-to-line voltage $V_{\rm ab}$ at $M_a = 1.15$ are shown in Fig. 14(d). The graph contains the fundamental frequency component followed by 14 harmonics components. Due to the symmetry attained in the inverter output line-to-line voltage, all even harmonics components are nearly eliminated. Moreover, the triplen harmonic components such as 3rd, 9^{th}, and 15th are also eliminated. A lower harmonic components lead to a lower THD%. The measured THD% is found around 9.038%. The measured (rms) value of the fundamental frequency component of the line-to-line voltage waveform $V_{\rm ab}$ is 63.61 V. It is nearly $1.15 \times (0.612 \times 4V_{\rm dc})$ where $0.612 \times 4V_{\rm dc} = 55.08$ V is the maximum (rms) value of the fundamental frequency component at $M_a = 1$. It can be seen that the (rms) value of the fundamental frequency component shown in Fig. 14(d) is increased by 15% at low THD%. The

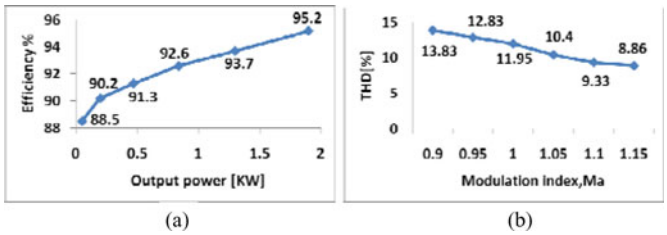


Fig. 15. Experimental results of (a) output power versus efficiency for the proposed inverter and (b) line-to-line voltage THD% versus M_a for $V_{\rm dc} =$ 75 V.

normalized value of the larger harmonic component 5th is 3.42/63.61 = 0.053. The existing harmonic components such as 5th, 7th, and 11th can be eliminated by applying staircase modulation with selective harmonic. It is worth noting that the estimation of optimal switching angles is not the objective of this paper. Decreasing the modulation index to $M_a = 0.8$ results in three positive levels (0, $+2V_{\rm dc}$, and $+4V_{\rm dc}$) in the inverter output line-to-line voltage waveforms as shown in Fig. 14(e). Such decreasing makes the proposed configuration operates as a traditional three-level inverter. The overmodulation happens when the proposed inverter is operated at $M_a > 1.15$. Fig. 14(f) depicts the experimental voltage waveform of the proposed inverter at $M_a = 1.3$. Further studies were conducted in order to verify the efficiency of the proposed inverter at the fixed $R - L$ load. The efficiency took different values at different voltages supplied from the dc link as depicted in Fig. 15(a). 1.9 kW of power was reached at modulation index $M_a = 1$. However, $V_{\rm dc}$ took the maximum value of 75 V. Since $V_{\rm fix} = 4V_{\rm dc}$ and during the testing the maximum dc value was supplied from $V_{\rm fix}$ that increased up to 300 V, the inverter' efficiency can be calculated based on the measured data as follows:

$$\eta\% = \frac{P_{\rm out}}{P_{\rm in}} \times 100 \tag{42}$$

where $P_{\rm in}$ and $P_{\rm out}$ are the inverter input and output power, respectively. The digital meter was utilized to measure $P_{\rm in}$ and $P_{\rm out}$. The efficiency takes values around 88% under low power conditions. However, better efficiency is attained at higher power as 95.2% is the measured efficiency at 1.9 kW. By comparing the measured efficiency shown in Fig. 15(a) with the calculated efficiency shown in Fig. 9(a), it can be seen that the measured efficiency is slightly lower than calculated. It is due to additional loss generated by cables resistance and measurements accuracy. If this further loss is considered and added, both measured and calculated efficiencies show a close agreement. Therefore, the proposed inverter is promising configuration that may serve in many applications. The variation of THD% with the modulation index for the inverter line-to-line output voltage is shown in Fig. 15(b). This illustrates that THD% is inversely proportional to the modulation index M_a. In other words, a lower THD% in the output voltage is experienced at higher modulation index.

VIII. Conclusion

A new topology of the three-phase five-level multilevel inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components.

Therefore, the proposed topology results in reduction of installation area and cost. The fundamental frequency staircase modulation technique was comfortably employed and showed high flexibility and simplicity in control. Moreover, the proposed configuration was extended to N-level with different methods. Furthermore, the method employed to determine the magnitudes of the dc voltage supplies was well executed. In order to verify the performance of the proposed multilevel inverter, the proposed configuration was simulated and its prototype was manufactured. The obtained simulation and hardware results met the desired output. Hence, subsequent work in the future may include an extension to higher level with other suggested methods. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation technique can be also implemented.

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