A New Boost Switched-Capacitor Multilevel Converter with Reduced Circuit Devices

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***Abstract*— In this paper, a novel platform for the single phase switched-capacitor multilevel inverters (SCMLIs) is presented. It has several advantages over the classical topologies such as: An appropriate boosting property, higher efficiency, lower number of required dc voltage sources and other accompanying components with less complexity and lower cost. The basic structure of the proposed converter is capable of making nine-level of the output voltage under different kinds of loading conditions. Hereby, by using the same two capacitors paralleled to a single dc source, a switched-capacitor (SC) cell is made that contributes to boosting the value of the input voltage. In this case, the balanced voltage of the capacitors can be precisely provided on the basis of the series-parallel technique and the redundant switching states. Afterwards, to reach the higher number of output voltage levels, two suggested SC cells are connected to each other with a new extended configuration. Therefore, by the use of a reasonable number of required power electronic devices, and also by utilizing only two isolated dc voltage sources, which their magnitudes can be designed based on either symmetric or asymmetric types, a 17- and 49-level of the output voltage are obtained. Based on the proposed extended configuration, a new generalized version of SCMLIs is also derived. To confirm the precise performance of the proposed topologies, apart from the theoretical analysis and a complete comparison, several simulation and experimental results are also given.**

***Index Terms*— Charge balancing control, multilevel inverters, reduced circuit devices, switched-capacitor cell**

NOMENCLATURE

φ : A phase difference between the output voltage and the load current.

K : Allowable voltage ripple across the capacitors.

ω : Angular frequency of the output waveforms.

CF : Cost function.

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t_{OFF} : Delay time for being OFF of each power switch

t_{on} : Delay time for being ON of each power switch

E_{OFF} : Dissipated energy for turning OFF of power switches

E_{On} : Dissipated energy for turning ON of power switches

r_{ESR} : Equivalent series resistance of each capacitor.

V_F : Forward biased voltage of power diode.

$R_{On,b}$: Internal resistance of each bi-directional power switch.

$R_{On,u}$: Internal resistance of each unidirectional power switch.

$R_{On,D}$: Internal resistance of power diode.

$I_L(t)$: Load current function

$N_{C,\max}$: Maximum number of power switches involved into the current path.

$I_{\max}$: Maximum value of the load current.

N_{Cap} : Number of required capacitors.

N_{Source} : Number of required DC sources.

N_{Driver} : Number of required gate drivers.

N_{IGBT} : Number of required isolated gate bi-polar transistors

N_{Level} : Number of output voltage levels.

N_{Diode} : Number of required power diodes.

N_{ON} : Number of turning OFF of each power switch.

N_{OFF} : Number of turning ON of each power switch.

C_{Opt} : Optimum capacitance of the capacitors.

P_{Out} : Output power

I : Passing current of each power switch before turning OFF.

I' : Passing current of each power switch after turning ON.

$i_C(t)$: Passing current function of each capacitor.

PIV : Peak inverse voltage of each power switch.

R_L : Resistive load value.

P_{Rip} : Ripple losses of the capacitors.

ΔV_C : Ripple voltage of each capacitor.

V_C : Steady state voltage of each capacitor.

V_{Sw} : Switching voltage of each power switch.

$P_{Con,T}$: Total conduction losses

$P_{sw,T}$: Total switching losses of power switches.

T : Total time period of a full cycle of the output waveforms.

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I. INTRODUCTION

NOWADAYS, the application of renewable energy (RE) resources like photovoltaic (PV) arrays that are incorporated into distributed generation (DG) systems, electric vehicles (EVs), motor drives, and unified power flow controllers (UPFCs), have become important research fields. In order to get a suitable ac waveform through RE resources for such applications, the dc-ac power converters including the voltage and current source inverters play an important role [1]-[2].

Obviously, due to less reliability, higher blocking voltage rating, and additional costs for designing a bulky filter at the output of the conventional two-level inverters, researchers are willing to replace them with new configurations of dc-ac converters that can be based on either impedance Z-source or multilevel voltage source inverters (MLVSIs) [3]-[9].

Hereby, MLVSIs are basically able to produce a staircase output voltage waveform with a high quality and an acceptable output harmonic spectrum. However, traditional types of such converters are always suffering from requiring many accompanying circuit devices, isolated dc voltage sources, and particularly the charge balancing control of capacitors due to possible usage of them instead of isolated dc sources [6]-[9]. Apart from these demerits, the amplitude of the output voltage cannot be higher than the scalar superposition of the dc link magnitudes, which means that they will fail to possess any boosting property.

Recently, many configurations of the developed MLVSIs have been recommended in the literature to decrease the aforementioned setbacks of the conventional ones [10]-[28]. Regarding the basic concept of MLVSIs and by the aim of some modulation-based methods, [12]-[13] could generate seven-level of the output voltage by using single dc source and paralleled capacitors. Also, the same controlling equipment is used in the flying capacitor multi cell (FCMC)-MLVSIs to generate a higher number of output voltage levels with single dc source and floated capacitors [14]-[16]. In addition, to eliminate the voltage sensors during the charge balancing process, a packed U-cell topology named as 5-PUC has also been recommended in [17] that could generate only 5-level of the output voltage with six power switches and a single dc source.

Contemporary, [18]-[20] have presented some reduced switch structures of the MLVSIs that can increase the output voltage levels with a contribution of multiple dc sources and capacitors. Owing to the self-charge balancing property of the circuits in these cases, the overall cost can be quite reduced since the matter of charge balancing strategy is mitigated. Hence, based on symmetrical and asymmetrical dc voltage sources, various number of output voltage levels could be obtained. However, although the use of capacitors can reduce the number of required dc sources, none of such topologies possess any boosting features.

Alternatively, switched-capacitor multilevel inverters (SCMLIs) that have recently emerged, can be counted as a valuable case study for further decreasing the number of required components and the dc sources associated with a boosting property and self-charge balancing capability for the involved capacitors [21]-[28]. Hereby, a single dc source nine-level SCMLI was proposed in [22] for high frequency applications. However, for further improving the number of output voltage levels, more active and passive circuit devices are required. Moreover, authors of [23]-[26] have presented a switched-capacitor (SC) cell that is able to boost the output voltage through the series-parallel conversion of two switches and a single capacitor. Having taken this concept in the developed cases, some new configurations of SCMLIs were suggested in the literature [23]-[28]. For instance, with a cascaded connection of several SC cells connected to the conventional full H-bridge cell, the number of output voltage levels could be symmetrically and asymmetrically increased [23]-[24]. A generalized SCMLI has also been presented in [25] in which the conventional full H-bridge cell has been removed. However, the effectiveness of [25] has been limited due to the fact that only the asymmetrical version of the dc voltage sources has been provided.

On the contrary, by integrating two isolated dc voltage sources and series-connections of two SC cells into each side of an improved H-bridge unit in [27], 13 output voltage levels can be symmetrically achieved. Here, 14 power switches, four capacitors and four power diodes have been used. In addition, based on the asymmetric design of this structure, 49-level of the output voltage could be given by employing 18 power switches and six capacitors. In order to reach higher number of output voltage levels, Ref [28] also presented a binary asymmetrical charging pattern for the capacitors of the SCMLI based on an improved series-parallel technique. Herein, since the capacitors' voltages are forced to be maintained on the higher value of the dc sources' magnitude, the output power limitations and severe capacitor ripple losses should have been addressed.

A new configuration of the SCMLIs has been proposed in this research that can produce more number of output voltage levels compared to the existing topologies with a reduced number of switching devices and particularly less number of required dc sources. The basic structure of the proposed SCMLI is able to generate nine-level of the output voltage. Hence, it has been made of a novel SC cell that includes only one dc voltage source, two capacitors and several active and passive semiconductor devices. In this regard, both the capacitors will be periodically charged and discharged without aiming any voltage sensors or intricate modulation methods. Also, in the succeeding, an extended structure of the proposed SCMLI is presented to enhance the number of output voltage levels. In this case, by aiming the same two proposed SC cells in a packed unit, 17- and 49-level of the output voltage can be obtained through symmetrical and asymmetrical designs of two integrated dc voltage sources, respectively. In respect to the extended concept of the proposed SCMLI, a new generalized version of the proposed converter will be also built. This paper is organized as follows:

The working principle and power circuit analysis for the basic structure of the proposed SCMLI is discussed in section II. Also, an extended structure of the proposed SCMLI besides its generalized form will be introduced in section III and IV. Afterwards, the principles of selecting an appropriate capacitance for the involved capacitors are presented in section V. Then, a power loss analysis will be conducted in

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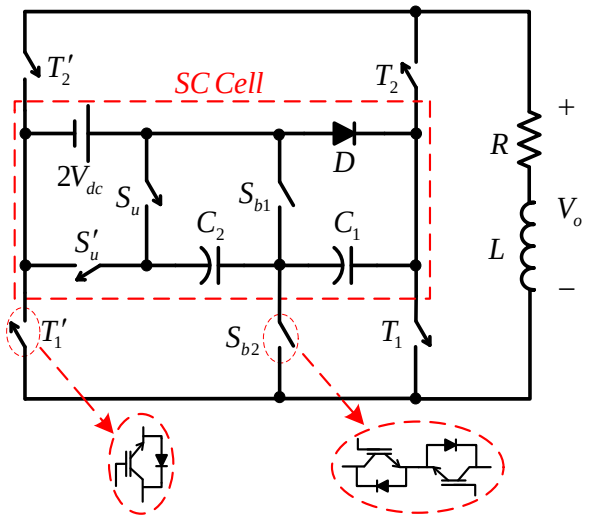

Fig. 1. Proposed Switched-capacitor multilevel inverter (SCMLI) structure

section VI. Also, to demonstrate the main benefits of the proposed SCMLIs, a comparative study with other recently presented structures and from different aspects will be done in Section VII. Finally, to show the precise performance of the proposed system, simulation and experimental results are given in section VIII.

II. Operating Principles of the Proposed SCMLI

Fig. 1 shows the proposed SCMLI structure, which is able to make nine-level of the output voltage by the contribution of a novel SC cell, four unidirectional and one bi-directional power switch. As it can be seen from the SC cell block, one power diode, two complement unidirectional power switches (S_u and S_u'), one bi-directional power switch (S_{b1}) along with two floating capacitors, which have been paralleled to a single dc source, are required to increase the number of dc-link as well as having the boosting property for the overall configuration. The use of bi-directional switches is imperative as long as they should block a stress voltage with positive and negative polarities in the general case of different loading conditions.

To prove the self-charge balancing and boosting capability of the proposed structure, different current flowing paths of the proposed nine-level inverter are depicted in Fig. 2(a)-(i), when a resistive-inductive load has been connected to the output. Here, the red and blue (dashed) lines represent the load current flowing path and the capacitors' charging loop, respectively.

First of all, in order to make the zero level of the output voltage, two different current flowing paths can be used with respect to Fig. 2(a). In this operating mode, both the capacitors are forced to be charged on the half of dc source's voltage or V_{dc} through a closed path drawn by the dashed line in the SC cell. Then, based on Fig. 2(b), to make the first positive level of the output voltage (V_{dc}), the bi-directional switch (S_{b2}) associated with T_2 should be ON. Therefore, the energy of capacitor C_1 is pumped to the output and also to provide the required charging current of C_2 from the dc source, the parallel switch S_U' in the SC cell must be ON.

In the following, to create the second positive level of the output voltage ($2V_{dc}$), without involving any of the capacitors into the load current path, the dc source is connected to the output through the forward-bias of the power diode in the proposed SC cell and turning ON the power switches T_1' and T_2. As it can be seen from Fig. 2(c), both the capacitors are again charged on V_{dc} during this time interval with contribution of switch S_U' in the ON state.

Based on Fig. 2(d), to generate the third positive level of the output voltage, voltage of the charged capacitor C_1 should be added to the dc source's voltage through turning ON the unidirectional power switches T_2 and T_1', and the bi-directional power switch S_{b1} in the SC cell. Herein, the power diode D is reverse biased. Therefore, the output voltage will be fixed on $3V_{dc}$. In order to avoid any malfunctioning operation in the proposed charging platform for each capacitor, the paralleled switch S_U' should not be ON, and therefore, the capacitor C_2 will be disconnected during this time interval. In respect to Fig. 2(e), the fourth level of the output voltage in the positive half-cycle is built by the series-connection of both the capacitors and the dc source together. As a result, both capacitors will theoretically be discharged and the output voltage level is fixed to $4V_{dc}$. As it is evident, excluding the top levels of the output voltage, the capacitor C_2 will be always charged by the dc source in the positive half-cycle of the output voltage level.

The related current flowing path of the first negative output voltage level ($-V_{dc}$) has been illustrated in Fig. 2(f). As it can be realized, the capacitor C_2 is discharged and its voltage will be pumped to the output, while the remaining capacitor (C_1) is being charged by the power supply by turning ON the parallel switch S_U' in the SC cell's loop. Also, the second negative output voltage level ($-2V_{dc}$) is properly made by the contribution of two power switches T_1 and T_2', while both the capacitors are being charged on the V_{dc} through the SC cell's loop implied by the blue dash lines in Fig. 2(g). The next negative level of the output voltage can be synthesized through the series connection of C_2 and the dc source and by contribution of S_U as shown in Fig. 2(h). Hereby, similar to the third positive level, the paralleled switch S_U' should not be ON. Therefore, during this time interval, C_1 will be disconnected from the load and the dc source.

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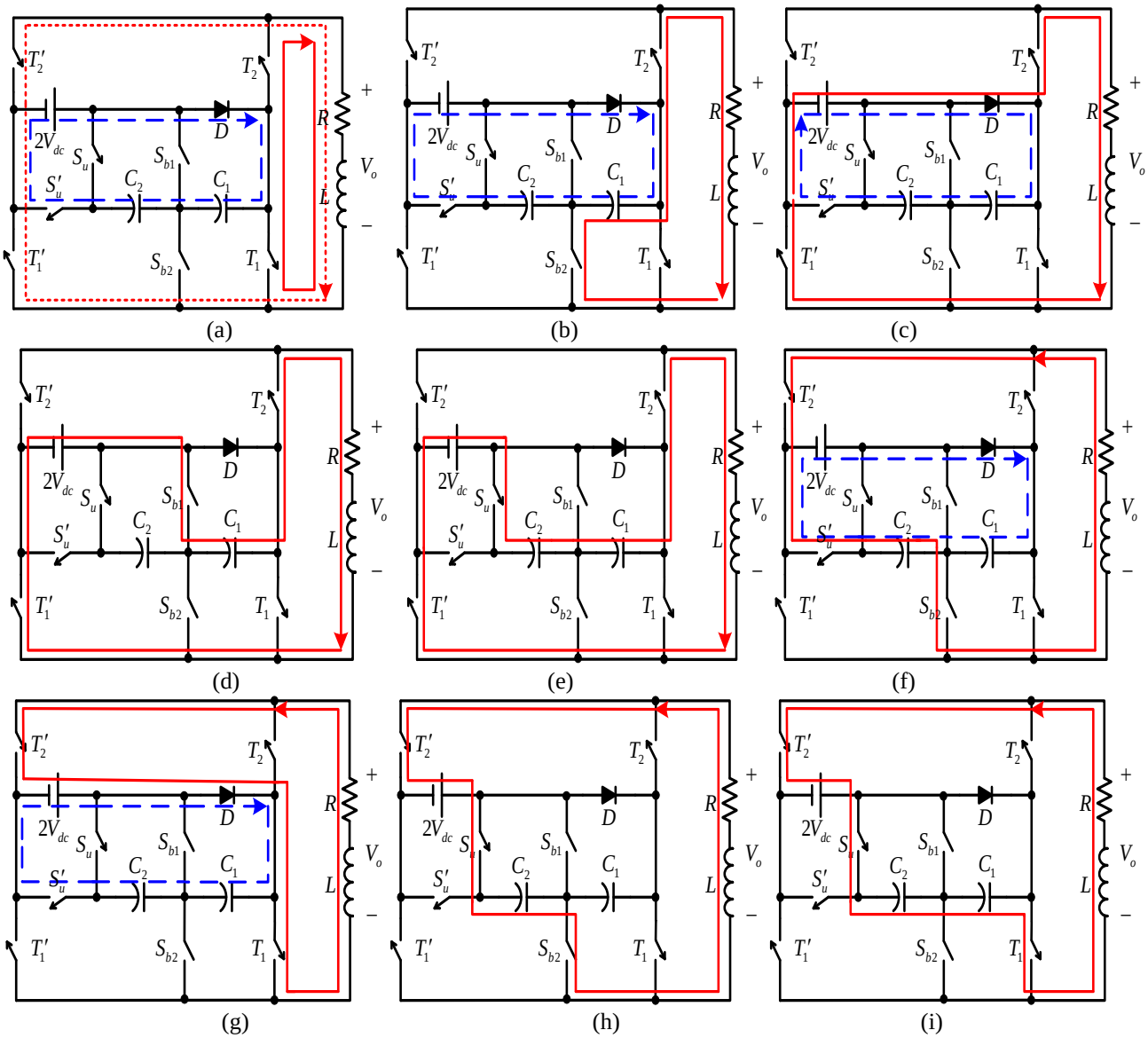

Fig. 2. Different current flowing paths of the proposed nine-level inverter for (a) zero-level (b) first positive level (c) second positive level (d) third positive level (e) fourth positive level (f) first negative level (g) second negative level (h) third negative level (i) fourth negative level.

Finally, with respect to Fig. 2(i), the fourth negative level of the output voltage ($-4V_{dc}$) can be made through the series connection of both the involved capacitors with the dc source and thereby turning ON the power switches T_1, T_2' and S_U, while the power diode becomes reverse biased. It is clear that regardless of the top negative output voltage level, the capacitor C_1 will always be charged during the negative half-cycle of the output voltage similar to what happened for C_2 in the positive half-cycle.

Therefore, since the duration of charging, discharging and un-connecting modes for both the capacitors are the same, their voltage will be fixed on V_{dc} at the end of one full cycle of the output voltage waveform without any requirement of charge balancing or external voltage sensors. In this case, the amplitude of the output voltage has been twice of the input one, which can precisely reflect the boosting property of the proposed system. In this regard, the maximum value of the output voltage, which must be tolerated by T_1, T_1', T_2 and T_2' in their OFF state condition as the peak inverse voltage (PIV) is equal to (1):

$$V_{o,\max} = 2V_{dc} + V_{C1} + V_{C2} = 4V_{dc} \quad (1)$$

From this perspective, the maximum PIV of each incurred series-parallel unidirectional power switch (S_U and S_U') is $2V_{dc}$, whereas this value for the involved bi-directional power switches of S_{b1} and S_{b2} is V_{dc} and $3V_{dc}$, respectively. So by summing the respective PIV of each power switch, the value of total standing voltage (TSV) on the switches will be $24V_{dc}$.

From the current flowing paths analysis, it can also be found that during the generation of each level of the output voltage, only three semiconductor devices should be ON. Therefore, the proposed configuration can also possess a suitable condition in terms of the overall conduction losses.

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III. EXTENDED STRUCTURE OF THE PROPOSED SCMLI

Reaching higher levels of the output voltage is always counted as a promising advantage of each SCMLI structure; therefore having taken the analyzed nine-level inverter principle into account, by adding another SC cell in a new configuration, an extended topology of the proposed SCMLI can be constructed as shown in Fig. 3.

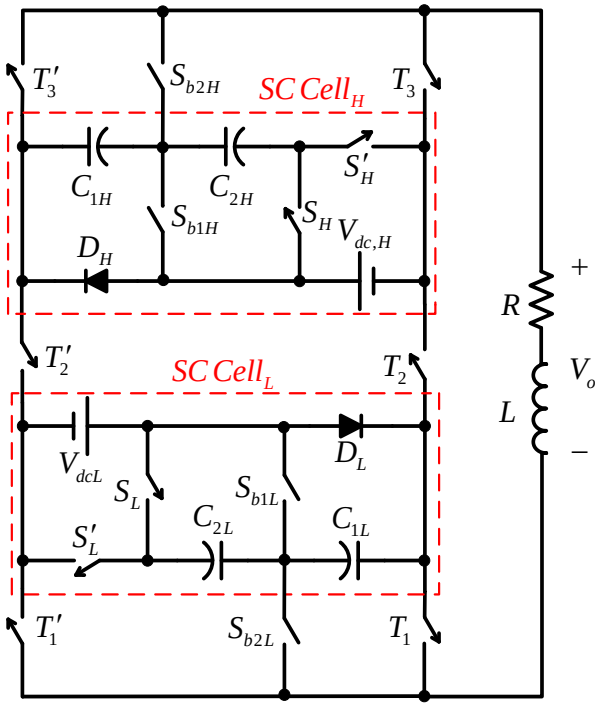

Fig. 3. Extended structure of the proposed SCMLI.

As it can be observed, based on the proposed extended SCMLI, only two isolated SC cells labeled as cell L and H, besides six unidirectional and two bi-directional power switches are required. Hereby, through choosing the same values of the integrated dc voltage sources, a symmetric structure is made that is able to produce 17-level of the output voltage (even and odd levels) in every condition.

Apart from this merit, the proposed extended SCMLI with the same circuit configuration is also capable of working based on the asymmetric principles. Here, the magnitudes of the two involved dc voltage sources can be set based on binary and trinary patterns ($V_{dc,\mathrm{H}}=2V_{dc,\mathrm{L}}=4V_{dc}$ or $V_{dc,\mathrm{H}}=3V_{dc,\mathrm{L}}=6V_{dc}$) that give 25 and 33 levels of the output voltage, respectively. However, in order to obtain the maximum possible number of output voltage levels that is a 49-level of the output voltage (24 positive levels, 24 negative levels and one zero level), the amplitudes of the dc voltage sources must meet the following equation:

$$V_{dc,\mathrm{H}}=5V_{dc,\mathrm{L}}=10V_{dc} \qquad (2)$$

Herein, the boost factor of the proposed SCMLI based on either symmetric or asymmetric assumptions of the dc sources is again two. Also, all the capacitors in both the SC cells can be remained charged at the half value of their respective dc voltage source with a self-voltage balancing strategy similar to the one presented for the proposed nine-level inverter.

TABLE I.
DIFFERENT SWITCHING AND CAPACITORS' STATES OF THE PROPOSED SYMMETRIC 17-LEVEL SCMLI

		ON Switches	v_o	Capacitor's states			
				C_{1L}	C_{2L}	C_{1H}	C_{2H}
Switching States	1	T_1',T_2,T_3',S_L,S_H	$8V_{dc}$	D	D	D	D
	2	$T_1',T_2,T_3',S_{b1L},S_H$	$7V_{dc}$	D	U	D	D
		T_1',T_2,S_{b2H},S_L,S_H		D	D	U	D
	3	T_1',T_2,T_3',S_L,S_H'	$6V_{dc}$	D	D	C	C
		T_1',T_2,T_3',S_L',S_H		C	C	D	D
	4	$T_1',T_2,S_{b2H},S_L',S_H$	$5V_{dc}$	C	C	U	D
		$T_1',T_2,T_3',S_{b1L},S_H'$		D	C	C	C
	5	T_1',T_2,T_3',S_L',S_H'	$4V_{dc}$	C	C	C	C
	6	$T_1',T_2,S_{b2H},S_L',S_H'$	$3V_{dc}$	C	C	C	D
		$T_3',T_2,S_{b2L},S_L',S_H'$		D	C	C	C
	7	T_1',T_2,T_3,S_L',S_H'	$2V_{dc}$	C	C	C	C
		T_1,T_2,T_3',S_L',S_H'					
	8	$S_{b2L},T_2,T_3,S_L',S_H'$	V_{dc}	D	C	C	C
		$T_1,T_2,S_{b2H},S_L',S_H'$		C	C	C	D
	9	T_1,T_2,T_3,S_L',S_H'	0	C	C	C	C
		T_1',T_2',T_3',S_L',S_H'					
	10	$T_3',T_2',S_{b2L},S_L',S_H'$	$-V_{dc}$	C	D	C	C
		$S_{b2H},T_2',T_1',S_L',S_H'$		C	C	D	C
	11	T_1,T_2',T_3',S_L',S_H'	$-2V_{dc}$	C	C	C	C
		T_1',T_2',T_3,S_L',S_H'					
	12	$T_1,T_2',S_{b2H},S_L',S_H'$	$-3V_{dc}$	C	C	D	C
		$T_3,T_2',S_{b2L},S_L',S_H'$		C	D	C	C
	13	T_1,T_2',T_3,S_L',S_H'	$-4V_{dc}$	C	C	C	C
	14	$T_1,T_2',T_3,S_L',S_{b1H}$	$-5V_{dc}$	C	C	D	U
		$S_{b2L},T_2',T_3,S_L,S_H'$		U	D	C	C
	15	T_3,T_2',T_1,S_L,S_H'	$-6V_{dc}$	D	D	C	C
		T_3,T_2',T_1,S_L',S_H		C	C	D	D
	16	T_3,T_2',S_L,S_H,S_{b2L}	$-7V_{dc}$	U	D	D	D
		T_3,T_2',T_1,S_L,S_{b1H}		D	D	D	U
	17	T_1,T_2',T_3,S_L,S_H	$-8V_{dc}$	D	D	D	D

Accordingly, Table I has summarized the switches and capacitors states of different output voltage levels for the

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proposed symmetric 17-level structure. In this Table, the terms of C, D and U stand for charging, discharging and un-connected modes for the capacitors in each level of the output voltage waveform. Also, the amplitude of both dc sources is assumed to be same as $2V_{dc}$.

An important point that can be found from this Table is that the discharging priority of the SC cells' capacitors in the positive half-cycle is C_{1L} and C_{2H}, and they will transfer their stored voltage to the output in the middle levels of the output voltage. In the negative half-cycle, this priority should be turned towards two charged capacitors of the positive half cycles or in other words C_{2L} and C_{1H}. With hindsight to this switching algorithm, the duration of charging modes for each capacitor can also be extended and therefore the ripple losses of the involved capacitors can offer very acceptable values.

It is also worth to note that the maximum number of power switches that should be ON at each instant is always five for making each level of the output voltage in the proposed symmetric 17-level and asymmetric 49-level structures as it can be found from Table I. Therefore, the proposed SCMLI possesses a great advantage in terms of minimizing the overall value of switches' voltage drop as well as conduction losses. This feature makes the proposed circuit suitable for high and medium voltage applications. In addition, the maximum value of the output voltage in the proposed extended SCMLI is obtained by (3); so, T_2 and T_2' should be designed based on the following voltages.

$$V_{o,\max} = V_{dc,L} + V_{dc,H} + V_{C1L} + V_{C2L} + V_{C1H} + V_{C2H} \quad (3)$$

IV. Generalized Structure of the Proposed SCMLI

Extension of the proposed SCMLI can be further intensified by integrating more numbers of the proposed SC cells into a packed unit as shown in Fig. 4. Regarding this concept, the number of output voltage levels can be enhanced in both the symmetric and asymmetric versions of the dc voltage sources. Here, during the generation of each output voltage level, the capacitors of those SC cells that are not involved into the load current path will be connected in parallel to their respective dc voltage source in each SC cell. Therefore, excluding the capacitors of the involved SC cells that are into the load current path, all the capacitors of non-involved SC cells will be charged by their respective dc voltage source. Therefore, having taken Fig. 4 as a proper connection for n numbers of the proposed SC cells, the required count of different components number for the proposed generalized SCMLI can be expressed as follows:

$$N_{Driver} = N_{Switch} = 6n + 2 \quad (4)$$

$$N_{Cap} = 2n \quad (5)$$

$$N_{Diode} = N_{Source} = n \quad (6)$$

Here, since in the medium voltage applications, each involved bi-directional power switch can be built through a back-to-back connection of two ordinary power switches, two insulated gate bi-polar transistors (IGBTs) for each of them are needed. So, the total number of required IGBTs for the generalized version of the proposed SCMLI can be written as:

$$N_{IGBT} = 8n + 2 \quad (7)$$

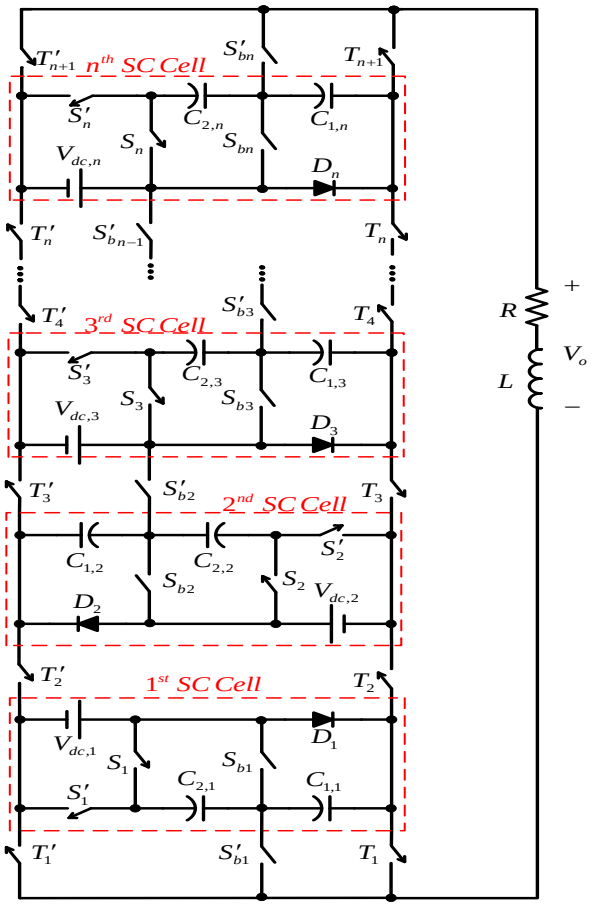

Fig. 4. A generalized structure of the proposed SCMLI.

Now, if the magnitudes of all the integrated dc voltage sources have been assumed to be quite the same ($2V_{dc}$), the maximum value of the output voltage, the overall value of TSV for the power switches and also the total number of generated output voltage levels for the proposed symmetric generalized SCMLI can also be obtained from (8)-(10) respectively.

$$N_{Level,Sym} = 8n + 1 \quad (8)$$

$$TSV_{Sym} = (16n + 8)V_{dc} \quad (9)$$

$$V_{o,\max,Sym} = 4nV_{dc} \quad (10)$$

Contemporary, in order to optimally use whole the potential of the proposed generalized SCMLI in the asymmetric design of the involved dc voltage sources, similar to one presented in (2) for the extended structure of the proposed SCMLI, the appropriate relationship between the involved dc voltage sources can be functionalized as follows:

$$V_{dc,i} = 2 \times (5)^{i-1} V_{dc} \quad i = 2, \ldots, n \quad (11)$$

Therefore, concerning (11) and similar to the proposed symmetric structure, the following equations can be derived as for the proposed generalized asymmetric SCMLI.

$$N_{Level,Asym} = 2 \times 5^n - 1 \quad n \geq 2 \quad (12)$$

$$V_{o,\max,Asym} = (5^n - 1)V_{dc} \quad n \geq 2 \quad (13)$$

$$TSV_{Asym} = \frac{(13 \times 5^n - 37)V_{dc}}{2} \quad n \geq 2 \quad (14)$$

In respect to (8) and (12), it is clear that by adding only one more of the proposed SC cell into the extended structure of the

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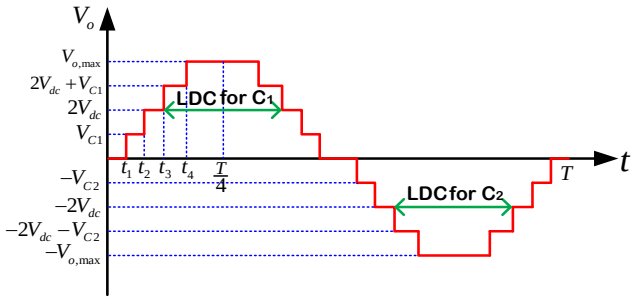

Fig. 5. A typical nine-level output voltage waveform.

proposed SCMLI ($n=3$), the number of output voltage levels can be remarkably enhanced (25 and 249 levels of the output voltage as for the proposed symmetric and asymmetric structures, respectively). In this case, since only one dc voltage source is used in each SC cell, such considerable number of output voltage levels can be made by the contribution of only three isolated dc voltage sources.

It should be pointed out that similar to other recommended topologies in the literature, the required values of the dc voltage sources for both the symmetric and asymmetric versions of the proposed SCMLI can be provided by using either a multi-tap transformer associated with the front-end diode-bridge rectifiers or the single input- multi output dc-dc converters [29]-[31].

Also, on the basis of the generalized platform for the proposed SCMLI, the maximum number of power switches involved into the current path can be written as (15). Herein, $N_{C,\max}$ is quite the same as for both the symmetric and asymmetric designs of the proposed SCMLI.

$$N_{C,\max}=2n+1 \tag{15}$$

V. Determination of Capacitance

To select an appropriate value of the capacitance for the used capacitors in the proposed nine-level structure, the longest discharging cycle (LDC) of each capacitor should be addressed. Having taken Fig. 5 as a typical nine-level output voltage waveform of the proposed inverter in the fundamental switching frequency, the LDC occurs in the positive and negative half-cycle of the output voltage waveform for C_1 and C_2, respectively. Herein, since the output voltage waveform offers only odd harmonics, the LDCs of C_1 and C_2 will be equal to each other. Therefore the maximum discharging value of each capacitor during the depicted LDCs in Fig. 5 is equal to (16).

$$Q_{C1}=Q_{C2}=2\times\int_{t_3}^{T/4} I_L(t)\,\mathrm{dt} \tag{16}$$

So, regarding $k\times V_{dc}$ as the maximum allowable value for the voltage ripple across the capacitors, the optimum value of capacitance for both the involved capacitors can be expressed as:

$$C_{Opt,i}\geq\frac{Q_{Ci}}{k\times V_{dc}}\quad for\ i=1and\ 2 \tag{17}$$

It is obvious that in order to solve (16) and in consequence (17), finding the equation of the load current is necessary. In this case, by considering Fig. 5 and for a pure resistive loading condition (R_L) at the steady state instants of the involved capacitors, the load current function during the generation of the third and fourth positive output voltage levels can be expressed as:

$$I_L(t)=\begin{cases}\dfrac{3V_{dc}}{R_L} & t_3\leq t\leq t_4\\ \dfrac{4V_{dc}}{R_L} & t_4\leq t\leq\dfrac{T}{4}\end{cases} \tag{18}$$

Here, by cutting some available dc levels to a sinusoidal function of the reference waveform in the fundamental switching frequency, the value of t_3 and t_4 will be equal to $\frac{3T}{20}$ and $\frac{T}{5}$, respectively [23].

On the other hand, as for the resistive-inductive loading condition, the function of $I_L(t)$ can be supposed to be:

$$I_L(t)=\mathrm{I}_{\max}Sin(\omega t-\varphi) \tag{19}$$

Therefore, by solving (16) with the aim of (18) and (19) at the fundamental switching frequency, the optimum capacitance of the involved capacitors under the pure resistive and resistive-inductive loading conditions will be obtained as (20) and (21), respectively.

$$C_{Opt,i}\geq\frac{7\pi}{5R_L\times k\times\omega}\quad for\ i=1and\ 2 \tag{20}$$

$$C_{Opt,i}\geq\frac{2I_{\max}}{k\times V_{dc}\times\omega}\left[\cos(\frac{3\pi}{10}-\varphi)+\sin\varphi\right]\quad for\ i=1and\ 2 \tag{21}$$

As it is obvious from (20) and (21), the optimum capacitance of both the involved capacitors in the proposed nine-level topology offers an inverse relation with k , ω and R_L. Regarding (20), to better conceptualize the effects of such parameters for determining an appropriate capacitance, the variations of C_{Opt} versus different values of R_L have been illustrated in Fig. 6(a). In this case, different rates of allowable voltage ripple for a fixed value of ω (100π) has been considered. Herein, it is clear that the larger rate of allowable voltage ripple across on capacitors leads to choosing a smaller capacitance. In respect to Fig. 6(a) and the expressed relation in (20), it can be properly realized that by increasing the value of the output frequency for different values of R_L, the required optimum capacitance of the capacitors will be much reduced.

It is also notable that in the fundamental switching frequency strategy, the lower rate of output frequency will contribute to lower rate of the switching frequency of the power switches [23], [24]. So, although increasing the range of the output frequency in this type of modulation strategy eventuates to choose smaller values of the capacitance, it can remarkably increase the rate of switching losses. In respect to (20), to better illustrate the impact of output frequency on the optimum value of the capacitors, the variations of C_{Opt} against different ranges of the output frequencies for a specific value of a

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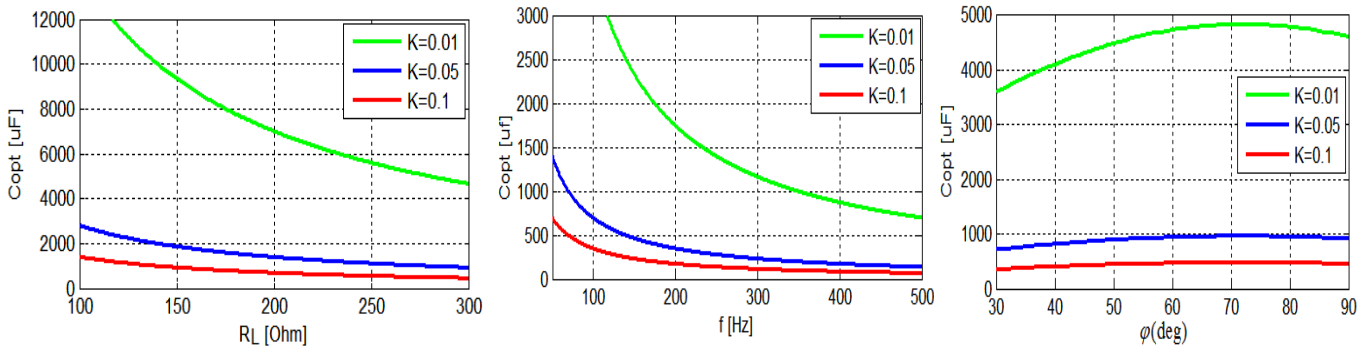

(a) (b) (c)

Fig. 6. The variations of C_{Opt} versus (a) R_L at $\omega=100\pi$ (b) different output frequencies at $R_L=200\Omega$ (c) different values of φ at $\omega=100\pi$

Resistive load $R_L=200\Omega$ has been plotted in Fig. 6(b). From this perspective, it is clear that for a five-percent allowable voltage ripple across the capacitors ($k=0.05$) and in the 50 Hz output frequency applications, the required capacitance of both the involved capacitors will be around 1000 μF .

Similarly, having considered a constant value for $I_{max}=4\,A$, $V_{dc}=100V$ and $\omega=100\pi$ (50 Hz) in (21), the respective variations of C_{Opt} versus a wide range of phase difference (φ) has been plotted in Fig. 6(c). As it is clear from these variations, C_{Opt} possesses a relatively constant relationship with different ranges of φ for both $k=0.05$ and $k=0.1$ conditions. Here, as for 50 Hz output frequency applications and under five-percent of the allowable voltage ripple across the capacitors, a value of $1000\mu F$ for C_{Opt} can be selected, while for a 10% allowable voltage ripple, this value can be halved. In this regard, by replacing $\omega=1000\pi$ (500 Hz) instead of $\omega=100\pi$ (50 Hz) in (21) and also by taking Fig. 6 (c) into account, it can be reconfirmed that C_{Opt} can also offer a much smaller value at the higher output frequency range.

VI. Power Losses Analysis

In this section, the theoretical values of the total power losses including switching, conduction and ripple losses for the proposed nine-level inverter (Fig.1) are analyzed.

A. Switching Losses

With a linear approximation between the passing current and the voltage across of a typical power switch, the dissipated energy during turning ON and OFF of the j^{th} involved power switch can be obtained from (22) and (23), respectively [28]. Therefore, by considering the number of turning ON (N_{on}) and OFF (N_{off}) of the switches during a full cycle of the output waveform, the average value of the switching losses for each level of the output voltage and for each of the involved power switches is calculated by (24) [28]. Regarding (24), in order to find the total value of the switching losses for the proposed nine-level inverter, the switching pulses of all the involved power switches will be important. These switching voltages will be illustrated in section VIII based on the fundamental switching strategy (50 Hz).

$$E_{On,j}=\int_0^{t_{on}} v(t)i(t)dt = \int_0^{t_{on}}\left[\left(\frac{V_{Sw,j}}{t_{on}}t\right)\left(-\frac{I'_j}{t_{on}}(t-t_{on})\right)\right]dt=\frac{1}{6}V_{SW,j}I'_j t_{on} \tag{22}$$

$$E_{OFF,j}=\int_0^{t_{Off}} v(t)i(t)dt = \int_0^{t_{off}}\left[\left(\frac{V_{Sw,j}}{t_{off}}t\right)\left(-\frac{I}{t_{off}}(t-t_{off})\right)\right]dt=\frac{1}{6}V_{Sw,j}I_j t_{off} \tag{23}$$

$$P_{sw,j}=\frac{1}{6T}\left[t_{on}\left(\sum_{k=1}^{N_{on}}V_{sw,kj}\times\left|I'_j\right|\right)+t_{off}\left(\sum_{k=1}^{N_{off}}V_{sw,kj}\times\left|I_j\right|\right)\right] \tag{24}$$

On the other hand, for a typical resistive loading condition, the passing current of j^{th} power switch for λ^{th} level of the output voltage can be expressed as:

$$\left|I_j\right|=\left|I'_j\right|=\left(\frac{\lambda V_{dc}}{R_L}\right)\qquad \lambda=1,...,4 \tag{25}$$

Using (25) in (24), the value of $\sum_{k=1}^{N_{on}}V_{sw,kj}\times\left|I'_j\right|$ and $\sum_{k=1}^{N_{off}}V_{sw,kj}\times\left|I_j\right|$ for each power switch during the generation of whole the output voltage levels can be obtained. Such values have been listed in Table II. So, P_{sw} of all the power switches for the proposed nine-level inverter can be taken by:

$$P_{sw,T}=\frac{22}{3T}\times\frac{V_{dc}^{\ 2}}{R_L}(t_{on}+t_{off}) \tag{26}$$

From (26), it is clear that for the same value of the input voltage, $P_{sw,T}$ is only inversely related to the load resistance and the cycle of switching frequency. Also, it is notable that the constant coefficient of $\frac{22}{3}$ in (26) is a specific value for the proposed topology. This constant coefficient has been obtained from Table II by summing all the calculated values of $\sum_{k=1}^{N_{on}}V_{sw,kj}\times\left|I'_j\right|$ and $\sum_{k=1}^{N_{off}}V_{sw,kj}\times\left|I_j\right|$ for each involved power switch operating within a full cycle of the output voltage

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TABLE II.
SWITCHING LOSS CALCULATION OF THE INVOLVED POWER SWITCHES FOR THE PROPOSED NINE-LEVEL INVERTER TOPOLOGY

	Involved power switches							
	T_1	T_1'	T_2	T_2'	S_{b1}	S_{b2}	S_u	S_u'
$\sum_{k=1}^{N_{on}} V_{sw,k} \times \lvert I' \rvert = \sum_{k=1}^{N_{off}} V_{sw,k} \times \lvert I \rvert$	$8\frac{V_{dc}^2}{R_L}$	$2\frac{V_{dc}^2}{R_L}$	0	$2\frac{V_{dc}^2}{R_L}$	$6\frac{V_{dc}^2}{R_L}$	$10\frac{V_{dc}^2}{R_L}$	$10\frac{V_{dc}^2}{R_L}$	$6\frac{V_{dc}^2}{R_L}$

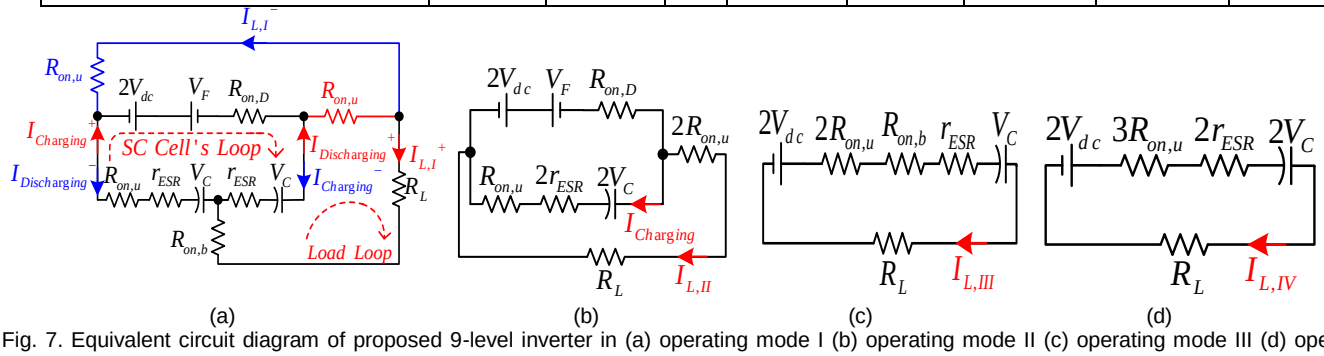

Fig. 7. Equivalent circuit diagram of proposed 9-level inverter in (a) operating mode I (b) operating mode II (c) operating mode III (d) operating mode IV.

frequency. Obviously, this constant coefficient is different in other structures since the switching voltages and also the numbers of turning ON and OFF for the involved switches are of particular for each structure.

B. Conduction Losses

In order to calculate the total conduction losses at the steady state conditions of the semiconductor devices and capacitors, the internal resistance of each component should be addressed. Here, the two used capacitors are assumed to be quite the same with the stored voltage of V_C on the steady state. Based on the overall circuit analysis conducted in Fig. 2(a)-(i), four different operating modes shown in Fig 7(a)-(d) can be extracted by the equivalent circuit diagrams of the proposed nine-level structure when a pure resistive load is connected to the output. The reason of selecting a resistive loading condition in the power loss analysis is due to the relationship between the load current and the output voltage; here there is not any auxiliary current path from the load to further facilitate the charging operation of the involved capacitors. Therefore, the resistive loading condition is seen as the worst case study in the power loss analysis of all SCMLIs [25],[28]. Accordingly, the first operating mode (see Fig. 7(a)) is attributed to the first positive and negative output voltage levels, where one of the capacitors are being involved in the load current path and another one is being charged through the SC cell's loop. Therefore, by applying the Kirchhoff Voltage Law (KVL) in the SC cell and in the load loop and also the Kirchhoff Current Law (KCL) in the connecting nodes, the following equations can be written:

$$(R_{On,u}+R_{On,b}+R_L)I_{L,I}^{+}+r_{ESR}\,I_{Discharging}^{+}=V_C \quad (27)$$

$$(R_{On,D}+r_{ESR}+R_{On,u})I_{L,I}^{+}-(R_{On,D}+2r_{ESR}+R_{On,u})I_{Discharging}^{+} = 2V_{dc}-V_F-V_C \quad (28)$$

$$(R_{On,D}+2r_{ESR}+R_{On,u})I_{Discharging}^{-}-(R_{On,D}+r_{ESR})I_{L,I}^{-}=V_F \quad (29)$$

$$(R_{On,u}+R_{On,b}+R_L)I_{L,I}^{-}+(R_{On,u}+r_{ESR})I_{Discharging}^{-}=V_C \quad (30)$$

$$I_{Discharging}^{+}+I_{Charging}^{+}=I_{L,I}^{+} \quad (31)$$

$$I_{Discharging}^{-}+I_{Charging}^{-}=I_{L,I}^{-} \quad (32)$$

where, $I_{L,I}^{+}$, $I_{Discharging}^{+}$ and $I_{Charging}^{+}$ are the load current, discharging current of the involved capacitor and charging current of non-involved capacitor in the first positive state, respectively. Also, $I_{L,I}^{-}$, $I_{Discharging}^{-}$ and $I_{Charging}^{-}$ are the same mentioned currents for the first negative output voltage level. As a result, the instantaneous amount of conduction losses during the positive and negative half-cycle of the first output voltage level can be expressed as (33) and (34).

$$p_{Con,I}^{+}=(R_{On,u}+R_{On,b})(I_{L,I}^{+})^2+r_{ESR}\,(I_{Discharging}^{+})^2 +(R_{On,D}+r_{ESR}+R_{On,u})(I_{Charging}^{+})^2 \quad (33)$$

$$p_{Con,I}^{-}=(R_{On,u}+R_{On,b})(I_{L,I}^{-})^2+(r_{ESR}+R_{On,D})(I_{Charging}^{-})^2 +(R_{On,u}+r_{ESR})(I_{Discharging}^{-})^2 \quad (34)$$

For the next output voltage level in both half-cycles, Fig. 7(b) should be taken into account. Thus, to find the load current in the second operating mode ($I_{L,II}$) and also the charging current of capacitors, the following equations should be solved:

$$(R_{On,D}+2R_{On,u}+R_L)I_{L,II}-R_{On,D}\,I_{Charging}=2V_{dc}-V_F \quad (35)$$

$$R_{On,D}I_{L,II}-(R_{On,D}+R_{On,u}+2r_{ESR})I_{Charging}=V_F \quad (36)$$

Therefore, the instantaneous value of the conduction losses during the second operating mode is:

$$p_{Con,II}=2R_{On,u}\,I_{L,II}^{2}+(2r_{ESR}+R_{On,u})I_{Charging}^{2} +R_{On,D}\,(I_{L,II}+I_{Charging})^2 \quad (37)$$

With respect to Fig. 7(c) and (d) and by applying the appropriate KVL, the load current of the third and fourth operating modes related to the third and fourth positive or negative output voltage levels can be obtained from (38) and (39), respectively.

$$I_{L,III}=\frac{2V_{dc}+V_C}{R_{On,b}+2R_{On,u}+r_{ESR}+R_L} \quad (38)$$

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$$I_{L,IV} = \frac{2(V_{dc} + V_C)}{3R_{On,u} + 2r_{ESR} + R_L} \quad (39)$$

Now, similar to the first and second defined modes, the related value of the instantaneous conduction losses in the third and fourth operating modes can be expressed through (40) and (41), respectively.

$$p_{Con,III} = (2R_{On,u} + R_{On,b} + r_{ESR}) I_{L,III}^{\ 2} \quad (40)$$

$$p_{Con,IV} = (3R_{On,u} + 2r_{ESR}) I_{L,IV}^{\ 2} \quad (41)$$

In order to calculate the total average value of the conduction losses during a full cycle of the output voltage waveform, the related time interval of each level of the output voltage should be considered. For a typical nine-level waveform shown in Fig.5, $[t_2 - t_1]$, $[t_3 - t_2]$, $[t_4 - t_3]$ and $\left[\frac{T}{4} - t_4\right]$ are supposed to be the relevant time intervals of the first, second, third, and fourth output voltage level, respectively. Therefore, by the contribution of the calculated instantaneous conduction losses, the average value of these losses in each defined mode and as a result the total value of conduction losses ($P_{Con,T}$) over the full cycle of the output voltage waveform are calculated as follows:

$$\overline{P_{Con,\mathrm{I}}} = \frac{2}{T}(t_2 - t_1) \times (p_{Con,I}^{\ +} + p_{Con,I}^{\ -}) \quad (42)$$

$$\overline{P_{Con,\mathrm{II}}} = \frac{4}{T} \times (t_3 - t_2)\, p_{Con,II} \quad (43)$$

$$\overline{P_{Con,\mathrm{III}}} = \frac{4}{T} \times (t_4 - t_3)\, p_{Con,III} \quad (44)$$

$$\overline{P_{Con,\mathrm{IV}}} = \frac{4}{T} \times (\frac{T}{4} - t_4)\, p_{Con,IV} \quad (45)$$

$$P_{Con,T} = \overline{P_{Con,\mathrm{I}}} + \overline{P_{Con,\mathrm{II}}} + \overline{P_{Con,\mathrm{III}}} + \overline{P_{Con,\mathrm{IV}}} \quad (46)$$

C. Ripple Losses of The Capacitors

Based on the conventional types of SCMLIs, the ripple losses would occur when the switching pattern is turning to charge the capacitors. Therefore, having considered $i_C(t)$ and C_i as the passing current and the pertinent capacitance of each capacitor, respectively, the ripple voltage of each capacitor can be expressed as (47) which comes from the voltage difference between the instant and the desired value of capacitor's voltage [21],[26].

$$\Delta V_{Ci} = \frac{1}{C_i} \int_{t'}^{t} i_{C_i}(t)dt \quad for\ i = 1\ and\ 2 \quad (47)$$

where $[t' - t]$ is the attributed time intervals pertaining to the charging modes of the capacitors. Hence, the total amount of ripple losses during a fundamental cycle of the output waveforms is obtained from (48).

$$P_{Rip} = \frac{1}{2T} \sum_{i=1}^{2} C_i \Delta V_{Ci}^{\ 2} \quad (48)$$

Since in every half-cycle of the output voltage waveform, both the involved capacitors can be charged for two specific time intervals (zero and the second output voltage levels) and considering the fact that only one of them should be discharged in the first and third output voltage levels, the calculated value in (48) for the proposed nine-level topology offers an acceptable amount. Now with respect to (26), (46) and (48), the theoretical value of the overall efficiency for the proposed nine-level SCMLI can be concluded according to (49).

$$\eta = \frac{P_{out}}{P_{out} + P_{sw,T} + P_{Con,T} + P_{Rip}} \quad (49)$$

Table III.
Comparison between the proposed topology and other recommended single dc source structures in [12],[17].[21] and [22].

Parameters	MLVSI [12]	5-PUC [17]	SCMLI [21]	SCMLI [22]	Proposed SCMLI
N_{Level}	7	5	7	7	9
N_{Driver}	7	6	10	10	8
N_{IGBT}	7	6	10	10	10
$TSV_{(pu)}$	5	4	6	6	6
N_{Cap}	3	1	2	2	2
$N_{C,\mathrm{Max}}$	3	3	5	5	3
N_{Diode}	2	-	-	-	1
Boosting Feature	No	No	Yes	Yes	Yes
Type of Charge Balancing	Modulation Based	Redundant States	Series-Parallel	Series-Parallel	Series-Parallel
Extended Ability	No	No	Yes	Not-Given	Yes

VII. COMPARISON WITH DIFFERENT TOPOLOGIES

In this section, in order to evaluate the number of required components used in the proposed SCMLI compared to some other recently presented SCMLIs and MLVSIs, a complete comparison from different point of views is done. Herein, to show all the potential of the proposed SCMLI compared to different recommended structures in the literature, the comparative study is divided into three different case studies as follows.

A. Comparison with Single dc Source Topologies

In this case study, the general features of the proposed single dc source nine-level SCMLI is compared with the recommended single dc source seven-level MLVSI in [12], the single dc source five-level 5-PUC in [17], the single dc source seven-level SCMLI in [21] and the single dc source nine-level SCMLI in [22]. Table III has listed the number of used components and also the overall features of each structure.

As it is obvious, with a contribution of reasonable counts of required circuit devices and having a boosting nature for the output voltage, the proposed topology generates the largest number of output voltage levels compared to the presented structures in [12], [17] and [21]. Here, none of the suggested structures in [12] and [17] possess any boosting feature with an extended ability to reach the higher output voltage levels, although some capacitors have been used in their structure. The charge balancing requirement of such capacitors depends on the redundant switching states along with a specific modulation-based method that can increase the complexity.

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Table IV. Comparison of different topologies at the symmetric condition of the involved dc voltage sources.

No. Ref	Parameters										
	N_{Level}	N_{Source}	N_{Driver}	N_{IGBT}	$TSV_{(pu)}$	N_{Cap}	N_{Diode}	$N_{C,\max}$	$\frac{CF}{N_{Level}}$		Boosting Feature
									$\alpha=0.5$	$\alpha=1.5$	
[19]	17	4	14	14	4.25	4	8	8	9.91	10.91	No
[23]	13	3	18	18	5	3	3	9	10.26	11.42	Yes
[27]	13	2	14	14	5.5	4	4	7	5.96	6.80	Yes
[28] (Non-Cascaded)	17	2	16	16	6	4	4	7	5.05	5.76	Yes
[28] (Cascaded)	17	4	20	20	5	4	4	10	12.47	13.05	Yes
Proposed Topology	17	2	14	18	6	4	2	5	4.82	5.52	Yes

Table V. Comparison of different topologies at the asymmetric condition of the involved dc voltage sources.

No. Ref	Parameters									
	N_{Level}	N_{Source}	N_{Driver}	N_{IGBT}	$TSV_{(pu)}$	N_{Cap}	N_{Diode}	$N_{C,\max}$	$\frac{CF}{N_{Level}}$	
									$\alpha=0.5$	$\alpha=1.5$
[24]	25	2	12	12	5	2	2	6	2.44	2.84
	125	3	18	18	5	3	3	9	1.06	1.19
[25]	49	3	14	14	5.5	3	3	7	2.25	2.58
	137	4	18	18	5.5	4	4	9	1.36	1.52
[27]	49	2	18	18	5.5	6	6	9	2.07	2.29
[28] (Non-Cascaded)	49	2	16	16	6	4	4	7	1.75	2.00
[28] (Cascaded)	169	4	20	20	5	4	4	10	1.19	1.31
Proposed Topology	49	2	14	18	6	4	2	5	1.67	1.91
	249	3	20	26	6	6	3	7	0.69	0.77

Also, even though the suggested SCMLI in [22] is able to generate the same number of output voltage levels with a generation of each output voltage level is higher than the proposed topology. A reduced number of required power diodes and having an extended ability to reach a higher number of output voltage levels are other advantages of the proposed topology in contrast to [22].

B. Comparison with Symmetric Topologies

The salient advantages of the proposed symmetric SCMLI based on its extended platform compared with some new and notable recently presented structures of SCMLIs and MLVSIs have been summarized in Table IV. In this case, a specific number of output voltage levels giving by each suggested topology are used for the evaluation. Here, the presented symmetric SCMLI in [28] can be extended with two different approaches. The first one is named as a none-cascaded structure that is using two capacitors in each side of the supposed SC cell, whereas the second derived topology in [28] is named as a cascaded platform by choosing only one capacitor in each side of the supposed SC cell. Also, in order to present an acceptable assessment for estimating the overall cost of each structure, a proportion of cost function (CF) equation expressed as (50) over the number of output voltage levels has been used in Table IV.

$$CF = (N_{IGBT} + N_{Driver} + N_{Diode} + N_{Cap} + \alpha TSV_{(pu)}) \times N_{Source} \quad (50)$$

boosting conversion similar to the proposed one, its maximum number of ON state power switches during the Having considered (50), the overall cost of all the required components counts including the number of required isolated dc voltage sources and also the number of required active and passive elements (gate drivers, IGBTs modules, electrolyte capacitors, and power diodes) are properly taken into account. Here, since in the selection of the appropriate power switches for each structure, the overall TSV will be important, so to precisely apply the impact of TSV into the proposed CF, a weight coefficient (α) can be multiplied in the per unit scale of TSV [25],[28]. Obviously, the value of α can vary between less and greater than one for different types of IGBTs modules in practice. Therefore, if α sets on a value that is less than one, the numbers of required power switches will be important, whereas by choosing a value of α that can be greater than one, the importance of TSV will be more weighted. From the defined ratio of $\frac{CF}{N_{Level}}$ in Table IV, it is clear that a cost-effective structure should simultaneously possess a lower rate of CF and a higher rate of N_{Level}. Concerning this concept, the lucrative benefit of the proposed 17-level symmetric SCMLI in contrast to all the mentioned cases can be seen in Table V in which the proposed topology

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offers a significant reduction in the value of $\frac{CF}{N_{Level}}$ for both conditions of $\alpha = 0.5$ and $\alpha = 1.5$. Apart from this merit, reduced number of $N_{C,\mathrm{Max}}$ for this considerable number of output voltage levels is another notable advantage of the proposed symmetric topology in contrast to others as one can be realized by Table IV. Here, although the presented 17-level symmetric MLVSI in [19] that cannot offer any boosting conversion, possesses the lowest rate of overall $TSV_{(pu)}$ among all the mentioned topologies, its overall number of required dc voltage sources and power diodes are respectively two and four times higher than the proposed 17-level symmetric structure.

C. Comparison with Asymmetric Topologies

Based on the asymmetric principles of the involved dc voltage sources in the higher number of output voltage levels, the overall benefits of the proposed topology over other recently proposed SCMLIs can be observed in Table V. Here, all the mentioned structures are using the SC concept with an asymmetric adjustment on the value of incurred isolated dc voltage sources. Therefore, all of them offer a boosting feature similar to the proposed asymmetric SCMLI. To have a fair comparison, two types of output voltage levels can be considered in respect to Table V.

Taking the medium number of output voltage levels (25 and 49 levels) into account, it is clear from Table V that the proposed 49-level asymmetric topology with a contribution of only two isolated dc voltage sources requires a cheaper design in contrast to other medium levels structures in both conditions of $\alpha = 0.5$ and $\alpha = 1.5$. In this case, the number of required gate drivers is exactly same with the presented 49-level asymmetric structure in [25], while it needs one more isolated dc voltage source and power diode compared to the proposed one. Moreover, the presented structure in [25] can only work based on the asymmetric designs of the involved dc voltage sources, whereas both the symmetric and asymmetric designs of the dc voltage sources can be used for the proposed topology.

Such advantages can be further seen in the higher number of output voltage levels, where the presented SCMLIs in [24],[25], and the cascaded scheme of [28] are generating 125,137 and 169 levels of the output voltage, respectively. By contrast, through a proper connection of the three proposed SC cells based on Fig. 4, 249 levels of the output voltage can be obtained with a remarkable reduction in the rate of $\frac{CF}{N_{Level}}$ compared to other topologies. Additionally, among both the medium and high output voltage levels SCMLIs, the proposed topology is able to diminish the number of ON state power switches during the generation of each output voltage level. This feature can also demonstrate another merit of the proposed asymmetric topology from the reduced conduction loss view point.

VIII. Simulation And Experimental Results

To verify the performance of the proposed single source nine-level SCMLI (Fig. 1) and also the proposed 17-level symmetrical extended SCMLI (Fig. 3), several simulation and experimental results are presented in the following. For the simulations, PSCAD/EMTDC software has been used.

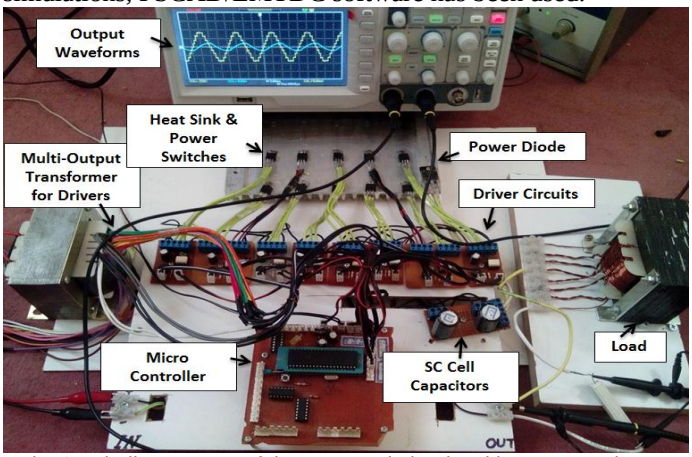

Fig. 8. A built prototype of the proposed nine-level inverter topology.

TABLE VI. THE LIST OF USED COMPONENTS IN THE EXPERIMENTAL TESTS.

Element	Type	Description
TLP 250	IC	Gate Drivers
PIC 18F452	IC Made by ATMEL COMPANY	Micro controller
IRFP460	Power MOSFET N-Chanel	$400V, 30A, R_{on} = 0.48\Omega$ $t_{on} = t_{off} = 5\mu s$
DCEC30-04A	Ultra-Fast Rectifier	$400V / 30A / R_{On} = 0.25\Omega /$ $V_F = 1.06V$
DC 85 C Series	Electrolytic Capacitor	$C = 1000\mu F / 550V /$ $r_{ESR} = 2.9m\Omega$

Also, as shown in Fig. 8, a prototype of the proposed topology has been built in order to obtain experimental results. Herein, a GPS (General Polytronic System)-1072B is used as the Oscilloscope to record the obtained experimental data. Since multiple power switches are used in the prototype, to avoid any short circuit problems, the GND of all the gate drivers should be isolated from each other. Concerning this issue, a transformer with one input and multi-output ports (eight ports for eight used gate drivers) has been used in the prototype as can be observed from Fig. 8. The output voltage of each port will be rectified and then they can make 15-20 V required DC voltage of each gate driver. Also, all the power switches and power diode are placed into a single heat sink plate. Here, a thin insulated film has been used behind each of semiconductor devices. Such thin insulated films can properly isolate the power switches from each other. The platform of the modulation strategy is on the basis of the fundamental switching frequency (50 Hz) for all the simulation and experimental verifications in which its details are beyond the scope of this paper.

A. Overall performance of the proposed nine-level SCMLI

In this subsection, the general performance of the proposed nine-level inverter (Fig. 1) is assessed. Table VI summarizes the list of used components and description thereof.

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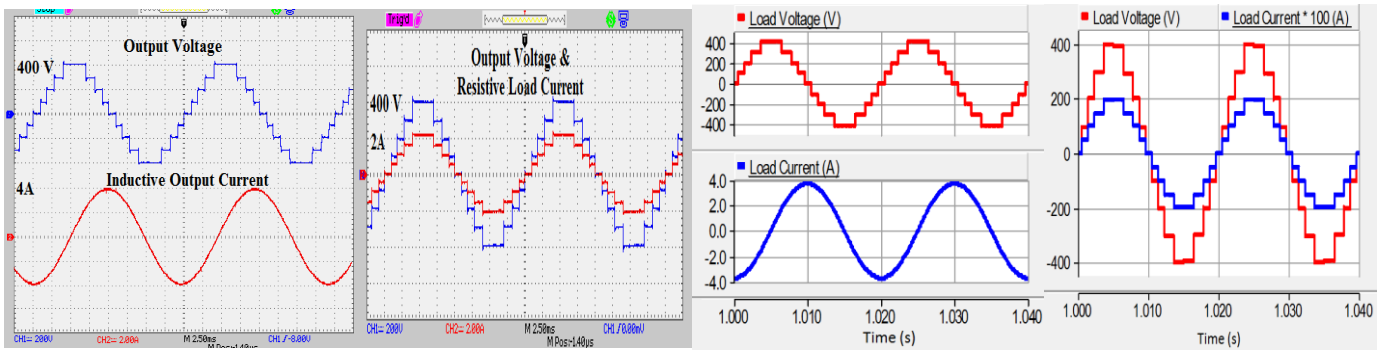

(a) (b) (c) (d)

Fig. 9. The nine-level output voltage and current waveforms (a) for inductive load (experiment) (200 V/div&2 A/div) (b) for resistive load (experiment) (200 V/div& 2 A/div) (c) for inductive load (simulation) (d) for resistive load (simulation).

Fig. 9(a)-(b) show the experimental results of the nine-level output voltage and the corresponding load current waveforms for the proposed topology and under the above-mentioned inductive and resistive loads. In this case, the relevant waveforms of the simulations are also shown in Fig. 9(c) and (d). As it can be seen, both types of results have a good agreement with each other. Hereby, the maximum amplitude of the output voltage is about 400 V that is twice of the input value for both types of loads, whereas the maximum amplitude of the output current is about 4 A for the inductive and 2 A for the resistive loading condition. As expected, the proper operation of the proposed circuit in terms of generating all the output voltage levels with boosting capability can be declared through both the simulation and experimental results. Also, the smooth levels of the output voltage under the resistive loading condition can be observed in Fig. 9 (b) and (d). This issue reconfirms the fact that the involved capacitors of the proposed topology have sufficient time for being charged by the power supply during each operating mode as discussed earlier.

In order to demonstrate the precise self-voltage balancing of two involved capacitors, the experimental voltage waveforms of C_1 and C_2 are demonstrated in Fig. 10. As it can be seen, both the capacitors of the proposed SCMLI have been balanced to half value of the respective dc voltage source's amplitude. In this case, the ripple voltage variations of the capacitors for one cycle of the output voltage waveform is about 9 V. Regarding (48), these ripple values create about 4.5 W ripple losses for both the involved capacitors during the above-mentioned loading condition.

In order to experimentally evaluate the switching losses of the proposed nine-level SCMLI, the PIV of all the involved power switches for two cycles is also illustrated in Fig. 11. Here, the maximum value of the PIVs is 400 V and all the power switches are being switched under the low switching frequency. Regarding the switching loss analysis and Table II, the total value of the switching losses is about 1.5 W in this case study. In addition, by taking the internal resistance of the semiconductor devices into the simulation, the input and output powers under the resistive loading condition are about 408 W and 400 W, respectively while under the severely inductive loading condition, these values are 780 VA and 740

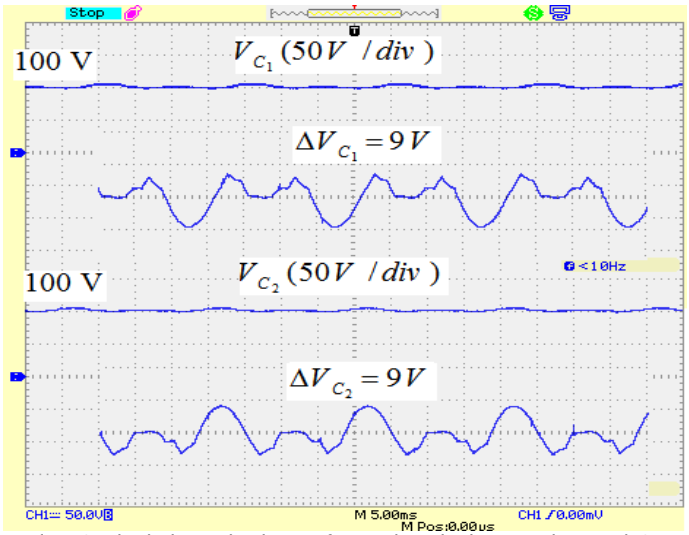

Fig. 10. The balanced voltage of capacitors in the experiments (50 V/div).

VA, respectively which enables to reach more than 95% efficiency for the proposed topology in both types of above-mentioned loads. Herein, to measure the overall efficiency of the proposed topology based on the experimental results, the input current waveform of the single dc source is important. So, a 350 mH inductive load has been connected at the output and the obtained input current waveform based on the experimental result is shown in Fig.12. Hereby, by multiplying the average value of the input current (about 4 A) with the mean value of input dc voltage (200 V), the measured value of the input power is obtained that is about 800 VA. Since the output voltage is a stepwise waveform, so in order to calculate the apparent value of the output power, the main harmonic order of the output waveforms are of importance [28]. Regarding, 385 V and 3.95 A as the maximum amplitude of the main harmonic order for the output voltage ($V_{main,out}$) and the load current ($I_{main,out}$) waveforms, the measured output power is about 760 VA as expressed in (51). Therefore, the measured value of the overall efficiency will be around 95%.

$$S_{out} = \frac{1}{2} V_{main,out} \times I_{main,out} \quad (51)$$

In order to further compare the performance of the proposed nine-level structure with other existing SCMLI topologies that are using the similar SC concept, the power losses under five

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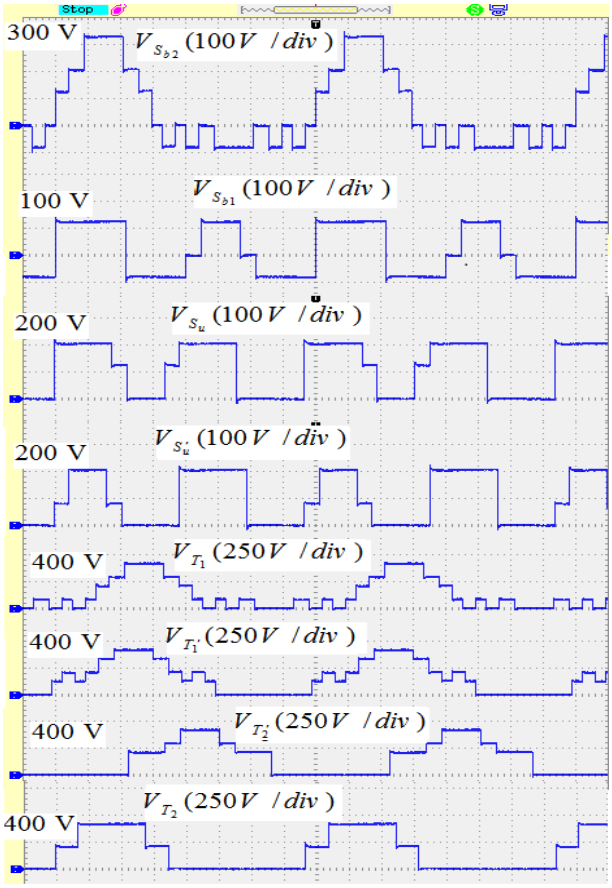


Fig. 11. The PIVs of the involved power switches based on the experimental result.

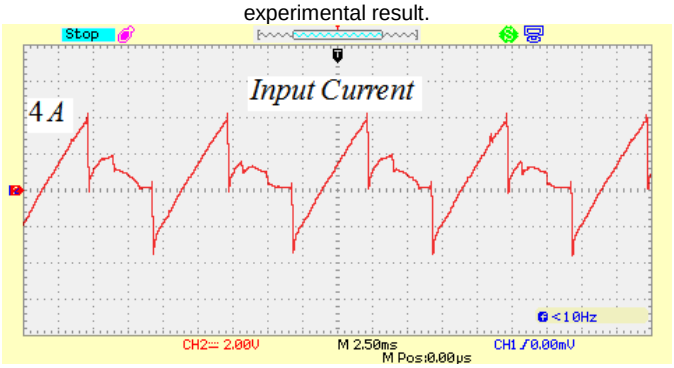
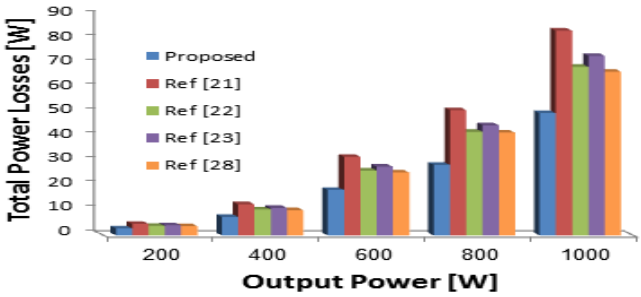
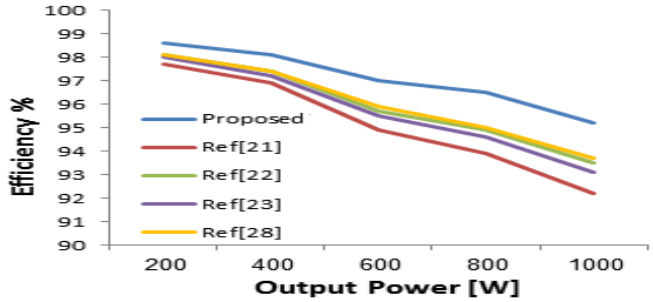


Fig. 12. The input current waveform under the inductive loading condition based on the experimental result (2 A/div).

different operating points of the output power has been summarized in Table VII. In this case, apart from the proposed topology, the derived nine-level topologies in Ref [21] (with a single dc source and 13 power switches), Ref [22] (with a single dc source and nine power switches), Ref [23] (with two symmetric dc sources and 12 power switches), and Ref [28] (with two symmetric dc sources and 10 power switches) have been chosen for comparison. To have a fair survey, all the calculations are done under the same conditions for the involved semiconductor devices and capacitors based on the presented power loss analysis in section V. In this case, the fundamental switching strategy (50 Hz) is selected and the maximum amplitude of the output voltage is assumed to be 400 V for all the mentioned cases. Here, to scrutinize the performance of different SCMLIs under the worst condition in delivering the output power, only the calculation of the



(a)



(b)

Fig. 13. Comparison of different nine-level structures (a) The total power losses variations versus output power (b) The overall efficiency versus output power.

resistive loading condition has been taken into account. From Table VII, it is obvious that as the output power increases, the performance of the proposed topology would be better than other structures since the ripple and conduction losses of the proposed topology are alleviated during the proposed series-parallel switching conversion. This issue can be further realized by considering the fact that owing to a significant value of ripple losses for the involved capacitors, the top level of the output voltage waveform for other SCMLIs' structures will not be quite smooth during the resistive loading condition. Also, regarding the above-mentioned calculation, the variations of total power losses versus different values of the output power for all the mentioned topologies are shown in Fig. 13(a). By considering these variations, the higher rate of overall efficiency for the proposed topology in contrast to others can be seen in respect to Fig. 13(b).

B. Dynamic performance of the proposed nine-level inverter

In this subsection, the transient and dynamic behaviors of output waveforms for the proposed nine-level topology are investigated by simulations and experiments. In this case, the magnitude of the single dc source is again set to be 200 V.

First, a 4 A resistive load is connected to the output. The obtained experimental results are the transient states waveforms from the no-load to full load and also from the full-load to no-load conditions that are shown in Fig. 14(a) and (b), respectively. Also, the corresponding waveforms taken from simulations can be observed in Fig. 14(c) and (d). Here, both types of results offer an acceptable accordance with each other and they can verify the fact that the nine-level output waveforms' behavior is very robust without any significant distortion in the transient state during the loading and no-loading conditions. In order to show the dynamic and also the accurate self-charge balancing behaviors of the output and the capacitors voltage waveforms, a step change load is considered. Fig. 15 shows these waveforms on the basis of the

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TABLE VII. LOSS COMPARISON OF DIFFERENT TOPOLOGIES AT DIFFERENT VALUES OF THE OUTPUT POWER

No. Ref	$P_{out}[\mathrm{W}]=200$			$P_{out}[\mathrm{W}]=400$			$P_{out}[\mathrm{W}]=600$			$P_{out}[\mathrm{W}]=800$			$P_{out}[\mathrm{W}]=1000$		
	Loss Distribution [W]														
	$P_{Sw,T}$	$P_{Con,T}$	P_{Rip}	$P_{Sw,T}$	$P_{Con,T}$	P_{Rip}	$P_{Sw,T}$	$P_{Con,T}$	P_{Rip}	$P_{Sw,T}$	$P_{Con,T}$	P_{Rip}	$P_{Sw,T}$	$P_{Con,T}$	P_{Rip}
[21]	0.91	0.65	3.1	1.8	2.6	8.3	2.7	5.8	23.6	3.6	10.4	37.2	4.5	16.2	63
[22]	0.88	0.58	2.4	1.8	2.3	6.5	2.6	5.2	18.7	3.5	9.3	29.5	4.4	14.5	50
[23]	0.78	0.70	2.6	1.6	2.8	6.8	2.3	6.3	19.5	3.1	11.2	30.7	3.9	17.5	52
[28]	0.84	0.55	2.4	1.7	2.2	6.4	2.5	4.9	18.3	3.3	8.8	28.9	4.2	13.7	49
Proposed Topology	0.75	0.35	1.7	1.5	1.5	4.5	2.25	3.5	12.8	3	5.7	20.1	3.5	12.5	34

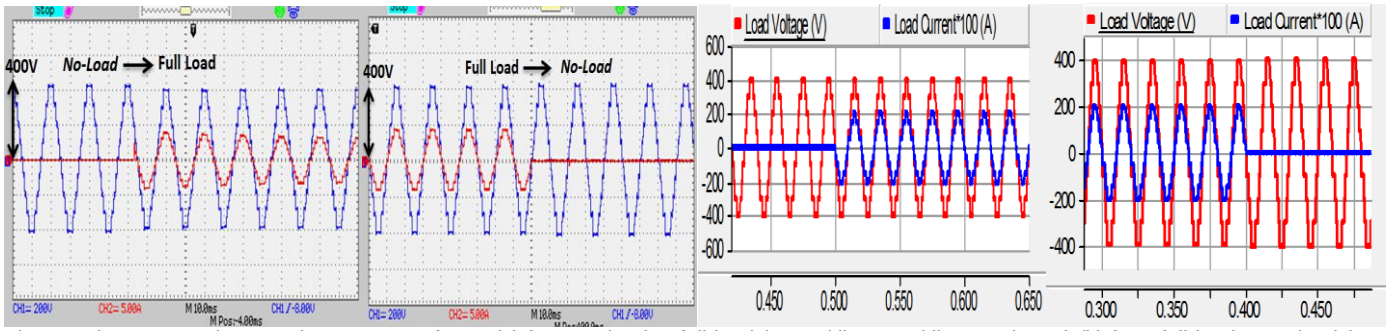

Fig. 14. The output voltage and current waveforms (a) from no-load to full-load (200 V/div & 5 A/div experiment) (b) from full-load to no-load (200 V/div & 5 A/div experiment) (c) from no-load to full-load (simulation) (d) from full-load to no-load (simulation).

experimental results. From these results, it is clear that changing the load does not have any considerable impact on the output waveforms, while the voltage across both the capacitors have been maintained at 100 V with allowable ripple values.

C. Overall performance of the proposed extended SCMLI

In this case study, the overall performance of the proposed symmetric extended SCMLI (see Fig.3), which is capable of making 17-level of output voltage, is experimentally evaluated. The two utilized dc voltage sources are quite the same and their amplitudes have been fixed to be 150 V ($V_{dc,\mathrm{H}}=V_{dc,\mathrm{L}}=2V_{dc}=150V$). Also the type of all the semiconductor devices and four involved capacitors are similar to those presented in Table VI, and the load is assumed severely inductive with a value of 250 mH. The fundamental switching strategy (50 Hz) is applied to the 14 involved power switches by taking Table I into account. Based on the mentioned considerations, the obtained experimental result from the output voltage and current waveforms is shown in Fig 16. As it can be observed, all the output voltage levels could precisely be made and the load current is nearly sinusoidal. Here, the maximum amplitude of the output voltage and the load current are 600 V and 5 A. Therefore, the proposed extended SCMLI can generate a two time boost factor at the output with only two of the same values of input dc voltages. By contrast, Fig. 17 indicates the balanced voltage of the integrated capacitors in both the SC cells of the proposed 17-level structure based on the experimental results. One can see that all the capacitor voltages have been fixed to 75 V with a self-charge balancing manner and there is a good agreement between the voltage ripple of capacitors in the lower and upper SC cells.

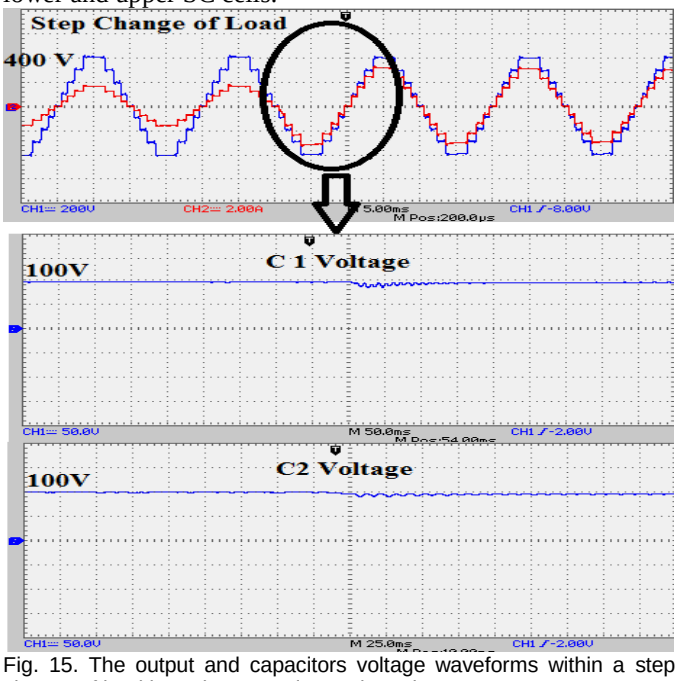

Fig. 15. The output and capacitors voltage waveforms within a step change of load based on experimental results.

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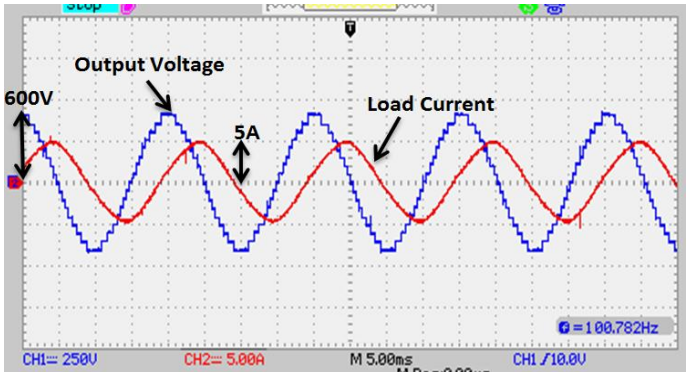

Fig. 16. Output voltage and current waveforms of the proposed symmetric 17-level structure in the experiments (250 V/div& 5 A/div).

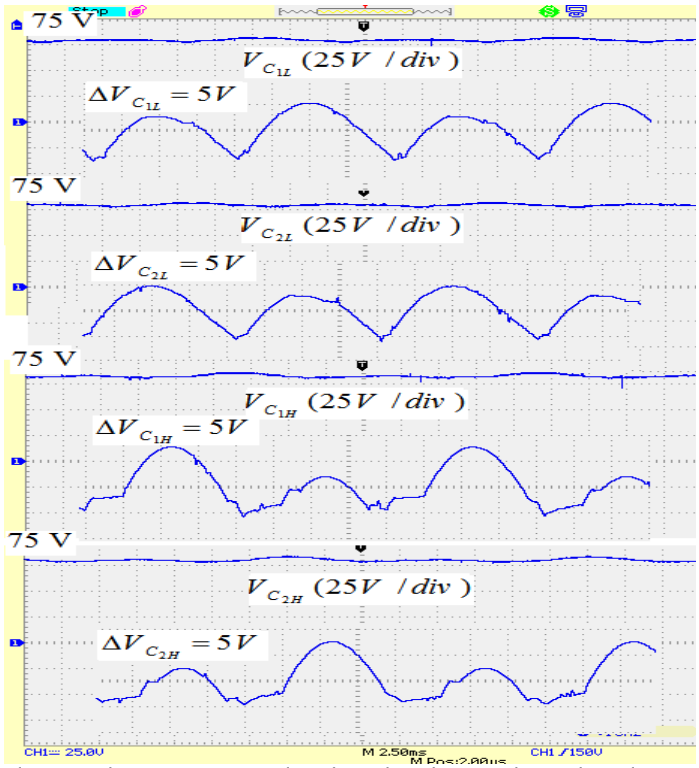

Fig. 17. Voltage across capacitors based on the experimental results (25 V/div) (Voltage ripple 2.5 V/div).

IX. Conclusion

In this study, a new basic topology of SCMLIs has been proposed which offers features like boosting capability, reduction in number of circuit components, higher efficiency and lower overall cost. The basic structure of the proposed SCMLI has only one dc source integrated into a novel SC cell. In this case, by aiming the series/parallel conversion of switches and also the redundant switching states, nine-level of the output voltage with only eight gate drivers has been obtained. Afterwards, in order to achieve further number of output voltage levels, an extended structure of the proposed SCMLI based on two isolated modules of the integrated SC cells has been presented. In respect to the proposed extended SCMLI, a generalized topology based on different numbers of involved SC cells has also been introduced. Then, determination of capacitance besides a power loss analysis is developed for the basic structure of the proposed SCMLI. A comprehensive comparison with other recently presented structures has also highlighted the potential of the proposed topologies. Finally, to demonstrate the precise performance of the proposed SCMLI configurations, various types of simulation and experimental tests under different kinds of loading conditions have been given.

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