Reduction of Capacitor Ripple Voltage and Current in Modular Multilevel Converter based Variable Speed Drives

Shambhu Sau, Saikat Karmakar, B. G. Fernandes
Department of Electrical Engineering
Indian Institute of Technology Bombay, Mumbai, India
email: shambhusau@ee.iitb.ac.in, saikatemail@ee.iitb.ac.in, bgf@ee.iitb.ac.in

***Abstract*—The major drawback of Modular Multilevel Converter (MMC) based variable speed drives is that the capacitor voltage ripple varies inversely with the output frequency. This voltage ripple can be reduced at lower operating frequency by injecting circulating current into its each arm. However, this circulating current increases the overall current rating of the converter. The voltage ripple can also be reduced by reducing the dc bus voltage when the drive is required to be operated at lower speeds. In this paper, a new configuration using multipulse diode bridge rectifier is proposed to reduce the dc bus voltage when the drive is operated at lower speeds. Therefore, the capacitor ripple voltage is reduced without injecting any circulating current. The proposed configuration is simulated in MATLAB/Simulink and the simulation results are presented to validate the proposed configuration.**

***Keywords*—Medium voltage drives, Modular multilevel converter, Multipulse rectifier, Variable Speed Drives.**

I. Introduction

Multilevel converters have gained popularity in high power applications due to their advantages such as low device switching frequency, lower voltage steps and reduced filter requirement [1]. Modular Multilevel Converter (MMC) is the most recent development in multilevel converter family which was originally proposed for high voltage dc transmission system [2]. The power circuit of a three phase MMC is shown in Fig. 1, which has three legs with two arms per leg. Each arm consists of N number of series connected submodules (SM) and an inductor. The configuration of half bridge submodule (HB-SM) and full bridge submodule (FB-SM) are shown in Figs. 1(b) and 1(c) respectively. Due to its simple and modular structure, research is being done to use it as a possible solution for medium voltage high power variable speed ac drives [3], [4]. However, the major drawback of MMC based drives is that it suffers from SM capacitor voltage fluctuation at low speeds as its peak to peak value is inversely proportional to the output frequency [3], [5]. This becomes severe particularly for constant torque loads.

The capacitor voltage ripple can be reduced by injecting higher frequency circulating current and common mode voltage into each arm of the converter [6], [7], [8]. This additional circulating current increases the current rating of the switching devices, arm inductors and capacitors [9]. The arm current rating could be as high as three times than that is required at rated torque and speed to achieve constant torque

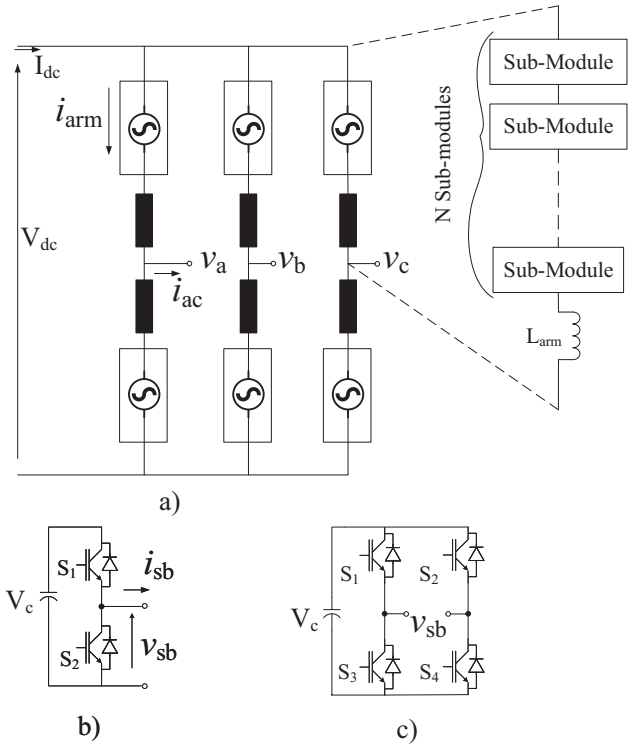

Fig. 1: Circuit configuration of a modular multilevel converter. a) Three phase converter, b) half bridge submodule, c) full bridge submodule.

over the whole speed range [6]. Various improved circulating current injection methods like square wave [8], hybrid injection method [10] are proposed in the literature to reduce the peak value of the arm current. However, the arm current is still more than that is required to produce the rated torque at rated speed. Moreover, the higher frequency common mode voltage is critical for drives system as it forces bearing current which may lead to its premature failure [5], [11]. Therefore, it remains a challenge to operate the drive at constant output torque for whole speed range [5], [6].

In [12], [13], the use of variable dc bus voltage is proposed to reduce the capacitor voltage ripple for variable speed drives. Reduction of dc bus voltage at lower output

frequency also reduces the capacitor ripple current compared to the constant dc bus voltage operation [12]. Active front end (AFE) rectifier with FB-SM based MMC [14] is one possible solution to vary the dc bus voltage [12], which has the advantage of regenerating power back to the grid. However, if the regeneration mode of operation is not required, the dc bus is normally supplied by multipulse diode bridge rectifiers along with phase shifting transformer to eliminate the lower order harmonic components from the source current [15]. In [16], the idea of buck converter is used as intermediate converter to reduce the average dc bus voltage of the MMC. However, the input side current is discontinuous, which requires additional filter circuit at the input side. Moreover, the intermediate converter reduces the overall reliability of the drive system.

In this paper, a modification of multipulse diode bridge rectifier circuit is proposed which allows to reduce the dc bus voltage while maintaining the SM capacitor voltage at its rated value. This eliminates the requirement of any additional circulating current injection into the arm. The drive with the proposed configuration is simulated in MATLAB/Simulink for variable output frequencies with constant output current and the simulation results are presented.

II. MMC IN DRIVES

In MMC, the current and voltage of each SM in the upper arm of phase-a are,

$$i_{sb} = \frac{I_{dc}}{3} + \frac{\hat{I}_{ac}}{2}\,\sin(\omega_0\, t - \phi) \tag{1}$$

$$v_{sb} = \frac{V_c}{2} - \frac{m\, V_c}{2}\,\sin(\omega_0\, t), \tag{2}$$

where, m is the output voltage modulation index. In variable speed drives with constant torque load, m varies almost linearly with the output frequency. Therefore, the modulation index and output frequency in per unit are used interchangeably in this paper.

Assuming the semiconductor devices are lossless, the peak to peak voltage ripple and rms value of the ripple current of the SM capacitor can be calculated as [2], [12],

$$\Delta V_c = \frac{2K_1}{\cos\phi}\,\frac{1}{m}\left[1 - \left(\frac{m\cos\phi}{2}\right)^2\right]^{3/2} \tag{3}$$

$$I_{crms} = \hat{I}_{ac}\frac{1}{4}\sqrt{\left(1 - \frac{m^2\,\cos^2\phi}{2}\right)}. \tag{4}$$

where K_1 is constant for constant torque output at different speeds. It is evident that both the capacitor ripple voltage and current increase when the modulation index decreases. However, with the variable dc bus voltage, these can be reduced [12] which is evident from the following equations.

$$\Delta V_c = \frac{2K_1}{\cos\phi}\,\frac{k}{m}\left[1 - \left(\frac{m\cos\phi}{2k}\right)^2\right]^{3/2} \tag{5}$$

$$I_{crms} = \hat{I}_{ac}\frac{1}{4}\sqrt{k\,\left(1 - \frac{m^2\,\cos^2\phi}{2\,k^2}\right)}. \tag{6}$$

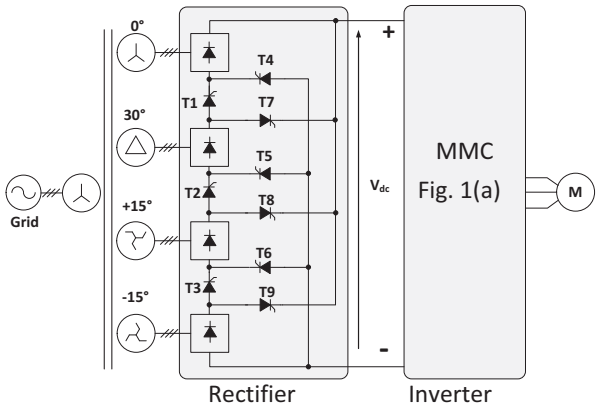

Fig. 2: Proposed configuration of the MMC based drive

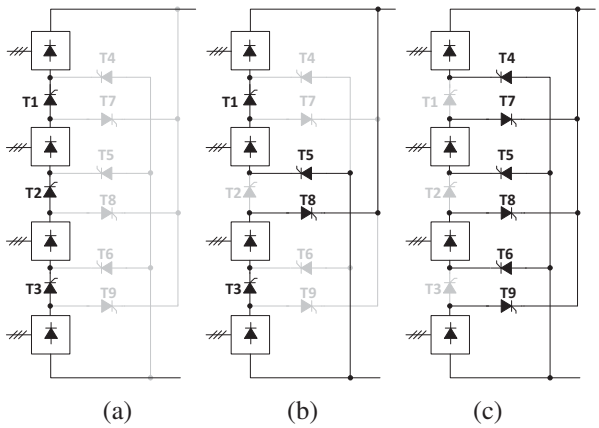

Fig. 3: Different switching states of the rectifier for : a) rated dc bus voltage, b) 50% of rated dc bus voltage, c) 25% of rated dc bus voltage.

Here, k represents the fraction of rated dc bus voltage and should always be more than or equal to modulation index in case of HB-SM based MMC. In MMC, the change of dc bus voltage is possible as RC filter with small capacitor is normally connected to the dc bus [17].

The dc bus voltage can be varied by using thyristorized bridge rectifier. However, it draws low quality input current at higher firing angle. Another possible solution is to use thyristorized tap-changing transformer with discrete level control, which makes the system bulky and costly. The use of an intermediate buck converter as proposed in [16] reduces the reliability of the overall system.

III. PROPOSED CONFIGURATION

A. Circuit configuration

The dc bus is normally supplied by multipulse diode bridge rectifiers in non-regenerative drives [15]. The multipulse rectifier operation can be achieved either by connecting the diode bridge rectifiers in series or in parallel [15]. Fig. 2 shows the proposed circuit configuration for the 24-pulse rectifier based MMC drive, which allows the diode bridges to be connected either in series or in parallel. All the diode bridges

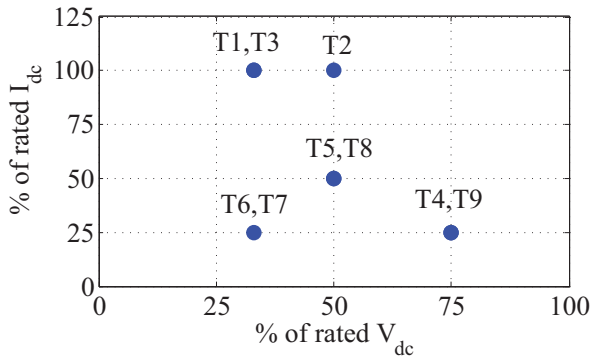

Fig. 4: Voltage and current ratings of the switching devices.

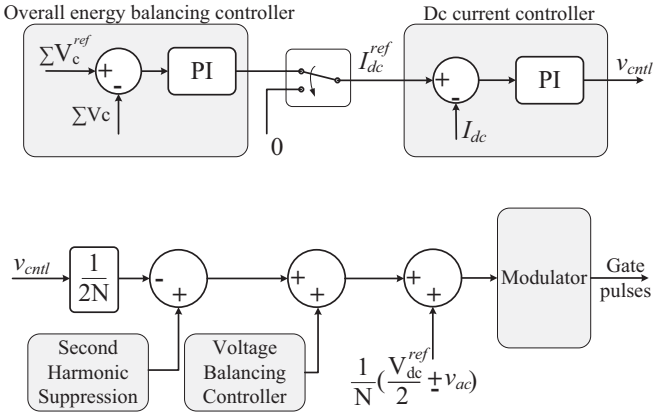

Fig. 5: Block diagram of the control scheme.

are connected in series to achieve the rated dc bus voltage, when the drive is operated near the rated output frequency. The circuit arrangement allows the diode bridges to be connected in parallel to reduce the dc bus voltage to 50% and 25% of its rated value at lower output frequency. The connection between diode bridges for three possible values of the dc bus voltages are shown in Fig 3. In case of HB-SM based MMC, the minimum dc bus voltage required is decided by the peak value of the output voltage. Therefore, to produce an output voltage higher than 0.5 pu, rated dc bus voltage is applied to the MMC. Similarly, half of the rated dc bus voltage is applied to generate output voltage between 0.25 pu to 0.50 pu. The dc bus voltage is reduced to 25% of its rated value when the output voltage is less than 0.25 pu.

Though it is possible to use either 12-pulse or 18-pulse rectifier, 24-pulse rectifier is considered in this paper as it meets the IEEE 519 standard without any additional line inductance [15]. Another advantage of this configuration is the increased reliability of the rectifier, as the drive can be operated at reduced dc bus voltage in case of fault at any of the rectifier bridges.

B. Selection of the switches

The switches T1-T3 need to block only forward voltage, whereas T4-T9 are required to block forward as well as reverse voltages. During the transition, the dc-link current is first reduced to zero to avoid the high voltage spike due to the arm inductance of MMC. Therefore, the switching losses of the devices are reduced. The voltage and current ratings of the switches (T1-T9) are given in Fig. 4. The maximum voltage rating of the switches is 75% of the rated dc bus voltage, which appears across the device T4 and T9 when the rated dc bus voltage is applied. Similarly, the current ratings of the switches T1, T2 and T3 are maximum and equal to rated dc bus current. It is to be noted that high voltage switches require lower current rating. Therefore, choice of thyristor would be suitable as switching device, since it is robust and highly reliable compared to other semiconductor switches.

C. Control scheme

Conventional control scheme [8] is used to control the voltage of all the SM capacitors. The block diagram of control technique is shown in Fig 5. The sum of all the SM capacitor voltages is maintained at its reference value by overall energy balancing controller, which generates the dc bus current reference, I_{dc}^{ref} of the MMC. The dc bus current is maintained at its reference value by dc current controller. The dc current controller generates the control voltage, v_{cntl} of each leg. This control voltage is equally divided to the $2N$ number of SM of one leg. Second harmonic suppression technique is used to reduce the second harmonic component of arm current [18]. The individual capacitor voltages are balanced by cluster voltage balancing and individual voltage balancing controller [8]. All these voltage components along with dc voltage reference, $V_{dc}^{ref}/2N$ and ac output voltage v_{ac}/N are added to generate the voltage reference for each SM. These voltage references are modulated by phase shifted PWM technique to generate the gate pulses for the switches of each SM.

D. Change of dc bus voltage

The change of dc bus voltage is performed when the output voltage reaches some predefined values. During the transition, the dc bus current is first reduced to zero to avoid high voltage spike due to the arm inductance of MMC. The advantage of MMC is that the dc bus current can be made zero momentarily as SM capacitors can supply the output power during the transition. The average value of SM capacitor voltage drops but this is not more than 10% as this whole transition takes place in less than one cycle of the grid frequency. The sequence of this process to make a smooth transition is summarized as follows:

1) The gate pulses from all the thyristors are blocked. However, to turn off the thyristor the dc bus current must be zero.
2) The dc bus current reference, I_{dc}^{ref} is made zero by bypassing the output of overall energy balance controller in Fig 5.
3) Dc bus voltage reference, V_{dc}^{ref} in Fig 5 is changed in small steps towards the next desired dc bus voltage. This change in small steps is required to avoid high dv/dt across the dc bus filter capacitor.
4) The gate pulses of the suitable thyristors are enabled depending on the desired dc bus voltage [Fig. 3].

TABLE I: Parameters for simulation

Grid line Voltage	3.3 kV	Rated power	1 MW
Load line voltage	3.0 kV	Trans. turns ratio (N_s/N_p)	1.3
Dc bus voltage, V_{dc}	5600 V	Transformer L_s	6%
Transformer R_s	1.2%	No of SM per arm	4
SM cap voltage	1400 V	SM capacitance	5 mF
Arm inductance, L_{arm}	10%	Switching frequency, f_s	1050 Hz

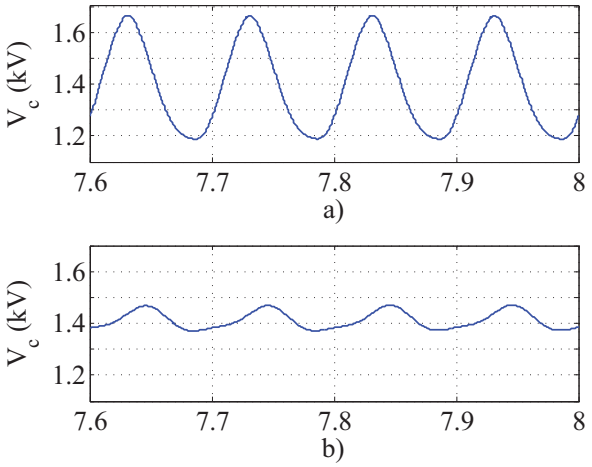

Fig. 6: SM capacitor voltage at output frequency of 0.2 pu and rated torque with a) rated dc bus voltage, b) 25% of rated dc bus voltage.

IV. Simulation Results

Simulation study on a 3.3 kV, 1 MW MMC drive system is carried out in MATLAB/Simulink with the parameters given in Table I. The rated dc bus voltage is considered as 5600 V to produce output line voltage of 3.0 kV. Considering 6% drop across the transformer leakage inductance at rated operating condition, the secondary to primary line to line voltage ratio is chosen as 1.3.

The capacitor voltage ripple at output frequency of 0.2 pu at rated torque with the rated dc bus voltage and 25% of the rated dc bus voltage are shown in Figs. 6(a) and 6(b) respectively. There is a significant reduction in capacitor ripple voltage when the dc bus voltage is reduced. It is to be noted that at lower output frequency, the fundamental frequency component in the capacitor ripple voltage is dominant compared to the second harmonic component [19]. Fig 7 shows the comparison of arm currents between hybrid circulating current injection method [10] and reduced dc bus voltage method for the same amount of SM capacitor voltage ripple at output frequency of 0.2 pu and rated torque. It can be seen that the arm current in hybrid circulating current injection method is more than twice that of the reduced dc bus voltage method. A common mode voltage of 2000 V is used in hybrid circulating current injection method. However, a common mode voltage of more than 100 V is not recommended, if the fundamental component of the applied stator voltage is low [5]. The required amount of circulating current increases further for same amount of capacitor voltage ripple, if the common mode voltage is reduced to limit the bearing leakage current, .

Fig 8(a) shows the simulation results of the drive system,

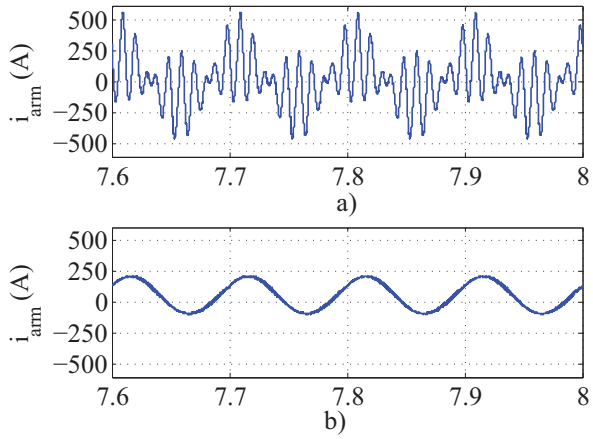

Fig. 7: The arm current at output frequency of 0.2 pu and rated torque with a) hybrid circulating current injection b) 25% of rated dc bus voltage.

when the output voltage frequency is first changed from 4 Hz to 50 Hz and then from 50 Hz to 4 Hz. The output voltage is varied proportionally to the output frequency. The output current is kept constant to emulate the constant torque load. For frequency below 12.5 Hz (0.25 pu), the dc bus voltage is maintained at 25% of its rated value by connecting all the diode bridges in parallel. The dc bus voltage is changed from 25% to 50% of its rated value by switching the proper set of thyristors when the output frequency reaches 12.5 Hz. As can be seen from the Fig 8(a) that the peak to peak voltage ripple becomes almost twice compared to that before change of dc bus voltage. The dc bus current also becomes half when the dc bus voltage is changed from 25% to 50% of its rated value. Similarly, the dc bus voltage is changed from 50% of its rated value to the rated value when the output frequency reaches 25 Hz. It can be seen that the capacitor ripple voltage remains within the desired limit over the whole speed range of operation without the need of injecting any circulating current. Although the dc bus current increases as the dc bus voltage reduces, the peak value of arm current does not exceed its rated value throughout the operating range.

The transition of dc bus voltage from 100% to 50% of its rated value is shown in Fig. 8(b). When the output frequency is reduced to 25 Hz, the gate pulses are removed from all the thyristors and the dc bus current reference, I_{dc}^{ref} is reduced to zero. To achieve this, the output of dc current controller, v_{cntl} is reduced and therefore the dc bus voltage is increased momentarily. Once the dc bus current is reduced to zero, the dc bus voltage reference, V_{dc}^{ref} is reduced slowly. The suitable set of thyristors are triggered when the dc bus voltage is near to 50% of its rated value. Although, the dc bus current is zero during the transition, the output current is maintained at its reference value as can be seen in Fig. 8(b). The average value of SM capacitor voltage drops as the output current is supplied by them during the transition. However, this drop is not more than 10% as the transition is completed within less than one cycle of the grid frequency.

The variation of input current THD for different operating speeds is shown in Fig. 9. The input current THD is slightly

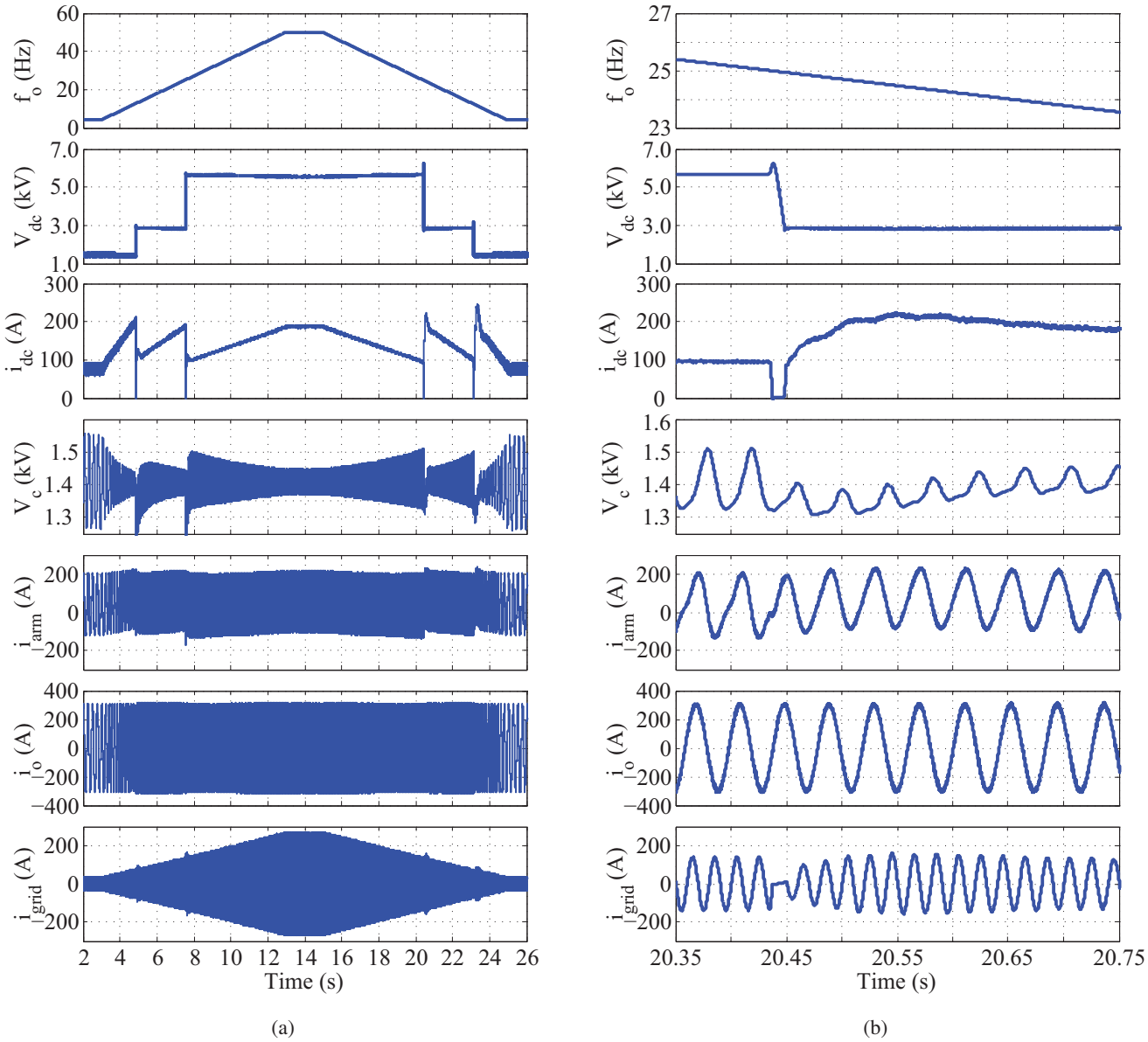

Fig. 8: Simulation Results : (a) Frequency varied from 4Hz to 50 Hz and 50 Hz to 4 Hz, (b) Zoomed at transition of dc bus voltage from 100% to 50% around 20.5 sec. From top : Output frequency, dc bus voltage, dc bus current, SM capacitor voltage, arm current, output current, grid current.

lower when the diode bridges are connected in parallel compared to that when those are connected in series particularly at lower output frequency. This is due to different harmonic distribution of the transformer secondary currents for series and parallel connection of diode bridges. However, the THD of the input current is within the IEEE 519 standard upto the output frequency of 7.5 Hz(0.15 pu).

Capacitor ripple current is one of the important factors for the capacitor selection in high power drives [20]. Fig. 10 shows that the rms value of the capacitor ripple current is also reduced when the dc bus voltage is reduced. With constant dc bus voltage, capacitor ripple current increases further due to the circulating current injection [12] into each arm. It can be seen from Fig. 10 that the capacitor ripple current for whole speed range of operation is within its allowable limit.

V. Conclusion

The SM capacitor voltage and current ripple are the main drawbacks of MMC based drives when operated at low speed. These ripple can be reduced if the dc bus voltage is reduced at low speed. In this paper, a simple method is proposed to reduce the dc bus voltage in MMC based drives, which is fed from multipulse diode bridge rectifiers. The proposed configuration allows the diode bridge rectifiers to be connected in series when the output voltage frequency of the drive is above 50% of the rated frequency. The diode bridge rectifiers are connected

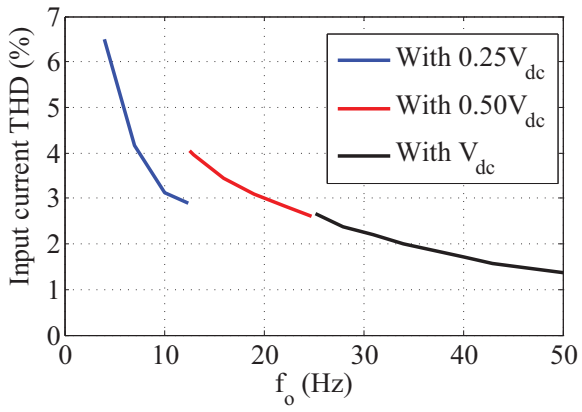

Fig. 9: Input current THD for different output frequency at constant torque output.

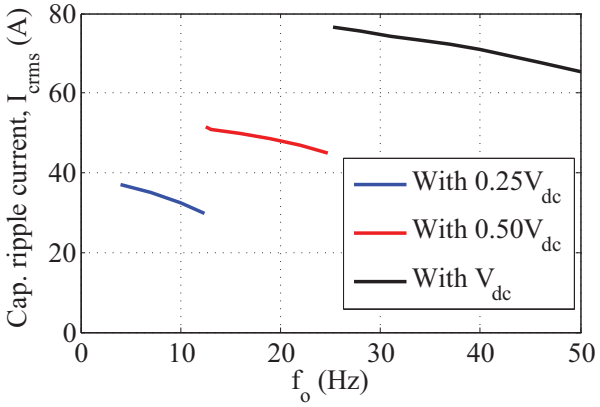

Fig. 10: Rms value of capacitor ripple current for different output frequency at constant torque output.

in parallel when the drive is operated at low frequency. The thyristors are switched at zero current only when the dc bus voltage is changed from one level to another level. Another benefit of the proposed configuration is that even if a diode bridge fails, the drive can be operated at reduced power with lower dc bus voltage. This makes the proposed MMC based drive more reliable. Although additional circuitry is required to vary the dc bus voltage, the overall cost of the converter is comparable to that of the existing solutions considering the rating of the components due to additional circulating current. Therefore, it can be an effective solution for high power medium voltage variable speed drives.

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