Research of the Electrical Characteristics Polysilicon on Insulator Thin Films

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***Abstract* – The electrical properties of polysilicon on insulator thin films (with a thickness 30-100 nm), which define a wide range of applications in electronic devices, were studied. Polysilicon thin film transistors are manufactured by a standard cheap technology that makes possible a mass production of semiconductor devices. The effective carrier mobility and state density in polysilicon thin film grown by CVD on SiO_2/Si substrate and their dependence on the conditions of fabrication of PolySi/SiO_2 heterointerfaces and on the film thickness were determined. It is shown that transistors fabricated using test films provide low leakage current and high I_{ON}/I_{OFF} ratio.**

***Index Terms* – Polysilicon, thin films, MOSFET.**

I. INTRODUCTION

AT THE PRESENT time, thin films of polysilicon and polysilicon thin film transistors have a wide usage in electronics - flexible electronic devices [1], organic light-emitting diode displays (OLED), active matrix liquid crystals displays (AMLCD) and large displays [2], solar cells [3], logical elements [4] and, recently, biosensors [5]. What is the reason of wide use of such transistors? First, they are manufactured by a standard silicon technology that makes possible a mass production of such devices. Furthermore, the process of deposition of polysilicon on Si, Si/SiO_2 substrates and flexible substrates (such as glass, plastic, or polymers [6]) is extremely cheap.

Along with the advantages of polysilicon thin film transistors, there are some drawbacks. The most important drawback is presence of a grain boundary in polysilicon (GB, the interface between differently oriented crystallites). The presence of potential barrier on GB (ΔE_C) leads to decrease in polysilicon film conductivity σ with exponential dependence on ΔE_C. , Besides, the conductivity linearly depends on the grain size L_{GR} in polysilicon [7]. So we get:

$$\sigma \sim L_{GR} exp\left(-\frac{\Delta E_C}{kT}\right) \quad (1)$$

The presence of the potential barrier and a high interface state density on GB in polysilicon films lead to a degradation of charge carrier mobility and conductivity of the films.

As is known, the parameters of MOSFET (metal-oxide-semiconductor field effect transistors)such as threshold voltage V_T, flat band voltage V_{FB}, subthreshold slope S, leakage current I_{LK}, etc. can be extracted from their current-voltage characteristics. Parameters of the Si/SiO_2 system such as charge carrier mobility μ, concentration of dopant N_D, interface state density D_{IT} and charge in the dielectric Q_{BOX} [8] can be extracted from parameters of the transistors . A fundamental feature of transistors on fully depleted silicon films is an interrelation of potential on opposite SiO_2 /Si/ SiO_2 interfaces [9]. Because of this effect, it is impossible to determine the parameters of a single interface not knowing the parameters of the second interface and not minimizing the contribution of the second interface. This problem is also typical for polysilicon thin film transistors. The solution of this problem is the creation of a certain controlled state of one of the Si/SiO_2 heterointerfaces using double-gate transistors. The double-gate transistors based on not depleting films allow to determine parameters of polysilicon films on both of the film/dielectric heterointerfaces independently.

Typically, the process technology of polysilicon thin film transistors begins with the deposition of amorphous silicon, in particular by chemical vapor deposition (a-Si, CVD, 580 °C), on various substrates. Different techniques like high temperature annealing, plasma annealing with different plasma composition (H_2 [10], NH_3, [4] et. al), ion implantation [11], excimer laser annealing [12], copper vapor laser annealing [13] etc. are used in fabrication of polysilicon films. The laser crystallization increases the grain size, and hence the carrier mobility and conductivity of films. It should be noted that high mobility and conductivity do not determine the performance of the most above listed devices. The most critical for the device performance parameters are low leakage currents and a high current ratio of the opened/closed state I_{ON}/I_{OFF} (the transistor's switching ability).

The purpose of this work is to study the polysilicon thin films properties with a thickness of less than 100 nm obtained by CVD and thermal annealing.

II. PROBLEM DEFINITION

The tasks of this paper were to determine the electrical properties of polycrystalline silicon films:

1) near heterointerfaces obtained at different conditions of growth of the polysilicon on the oxidized substrate and of thermal oxidation of polysilicon;

2) depending on the polysilicon film's thickness – 27 nm, 47 nm, 100 nm.

3) depending on dopant concentration in range $2*10^{16}$ - $1*10^{17}$ cm^{-3};

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4) comparing parameters of polysilicon on insulator films and silicon-on-insulator (SOI) films.

The initial amorphous silicon films were obtained by CVD process with thermal decomposition of monosilane SiH_4 at T =580 °C. Then, high temperature annealing was performed in an argon atmosphere at T = 900 °C for 20 minutes. Then, the n-channel transistors on the a-Si/SiO_2/Si-sub structure were formed:

- with the top gate, TG (fig.1,a);
- with the free surface of the film (fig.1,b).

For comparison, the transistors based on silicon-on-insulator (SOI, fig. 1, c) were used. All transistors used the silicon substrate as the bottom gate BG.

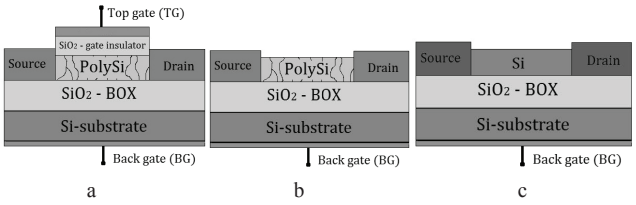

Fig.1. Schematic image of a top gate transistor based on polysilicon on insulator (a) and an open surface transistor based on polysilicon on insulator (b) and SOI (c).

The design parameters of these transistors are given in table I. t_{OX} is the gate insulator thickness and t_{BOX} is the thickness of buried oxide.

TABLE I
PARAMETERS OF STUDIED STRUCTURES

Parameters	Transistors with TG based on polysilicon	Transistor with open surface based on polysilicon on insulator	Transistor with open surface based on SOI
t_{film}, nm	100	27 / 47	30
t_{BOX}, nm	280	310 / 210	300
t_{OX}, nm	76	-	-
L/W, μm/μm	100 / 100	10 / 10	10 / 3

Based on the $I_{DS}(V_{BG})$ characteristics the following parameters of transistors have been defined:

- interface state density D_{IT} ($eV^{-1}cm^{-2}$);
- effective carrier mobility μ ($cm^2/V*s$).

The mobility value was calculated from the expression for $I_{DS}(V_{BG})$ dependence (2):

$$I_{DS} = \frac{W}{L}\mu_e C_{OX}\left(V_{BG} - V_{TH}\right)V_{DS} exp\left(-\frac{\Delta E_C}{kT}\right), \qquad (2)$$

where W is the width and L is the length of gate, C_{OX} is the capacity of dielectric, V_{TH} is threshold voltage, V_{DS} is pulling source-drain voltage, *k* is Boltzmann's constant and T is temperature.

The interface state density was calculated from the expression for the subthreshold slope S of $I_{DS}(V_{BG})$ (3):

$$S = ln10 \cdot \frac{kT}{q}\left(\frac{C_{IT} + C_{OX} + C_{Si}}{C_{OX}}\right), \qquad (3)$$

$$D_{IT} = qC_{IT.} \qquad (4)$$

where C_{IT} is the interface state's capacity, C_{Si} is the silicon film capacity and q is the electron charge.

III. RESULTS AND DISCUSSION

Fig. 2 shows the $I_{DS}(V_{BG})$ characteristics of transistors based on undoped polysilicon film with thickness of 100 nm measured at different top gate voltages . It can be seen that:

1) leakage current I_{LK} of transistors at $V_{TG} = 0$ is less than $1*10^{-11}$ A;

2) $I_{ON}/I_{OFF} > 10^5$;

3) at higher V_{TG} values there is an additional constant current component in the V_{BG} voltage range of 0-80 V;

4) there is no shift characteristic on the voltages axis depending V_{TG}.

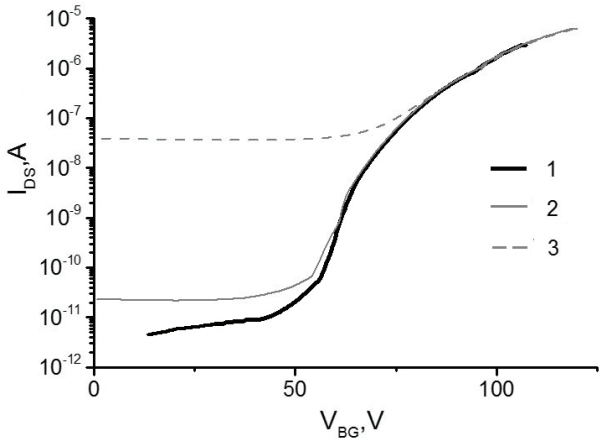

Fig. 2. $I_{DS}(V_{BG})$ curves for polysilicon transistors with constant V_{TG} voltage: 0 V (1) ; -5 V (2); 10 V (3). V_{DS} = 1 V.

Fig. 3 shows the $I_{DS}(V_{BG})$ characteristics for transistors based on polysilicon film with thickness of 47 nm doped with arsenic at concentration in the range of $2*10^{16}$ - $1*10^{17}$ cm^{-3}. It can be seen that high I_{ON}/I_{OFF} values remain unchanged and leakage current I_{LK} is less than $1*10^{-11}$ A. The doping of films has little effect on characteristics. The shift of $I_{DS}(V_{BG})$ characteristics along the voltage axis (ΔV_T threshold voltage shift) is not more than 3 V. Note that the doping of monocrystalline silicon in such concentration range provides $\Delta V_T \sim 6$ V.

Fig 4. shows the $I_{DS}(V_{BG})$ characteristics for transistors based on polysilicon film with thickness of 27 nm and on SOI with thickness of 30 nm. It can be seen that the films have similar leakage currents. Comparable I_{ON}/I_{OFF} values are observed at high V_{DS} voltage.

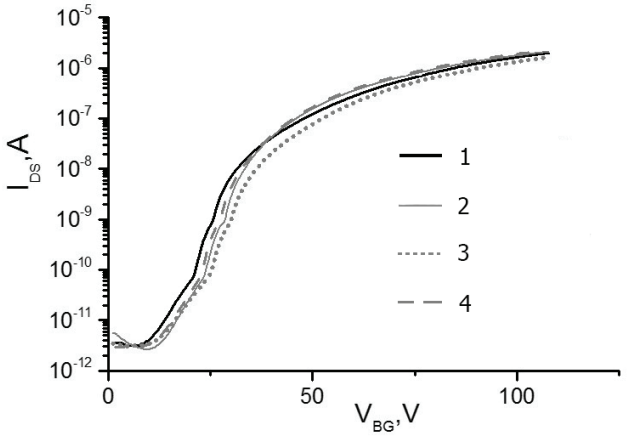

Fig. 3. I_{DS} (V_{BG}) curves for polysilicon transistor with different doping concentration N_D (cm^{-3}): $2*10^{16}$ (1); $4*10^{16}$ (2); $8*10^{16}$ (3); $1*10^{17}$ (4). V_{DS} = 1 V.

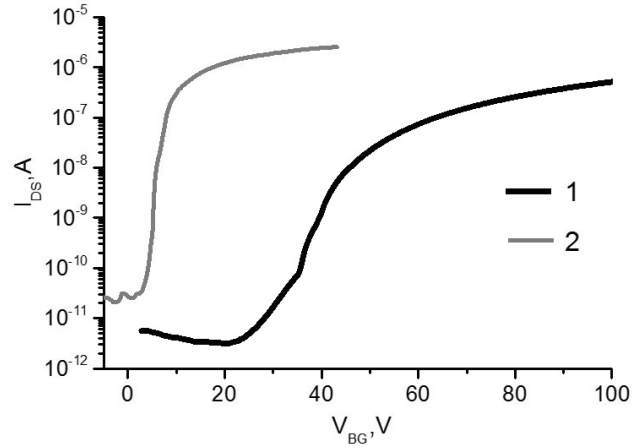

Fig. 4. I_{DS} (V_{BG}) curves for polysilicon thin film transistor with V_{DS} = 1 V (1) and SOI-transistors with V_{DS} = 0.1 V (2).

The appearance of the constant current component at higher V_{TG} values for the polysilicon film thickness of 100 nm (fig. 2) indicates that a conduction channel in film near the TG is formed. The absence of shift of characteristics on the V_{BG} voltage axis suggests that the potentials at the opposite interfaces are not related, i.e. undoped polysilicon film thickness of 100 nm is not depleting (film thickness t_{film} is greater than depletion region thickness t_{SC}). The Debye length ($L_D = \sqrt{\frac{kT\varepsilon\varepsilon_0}{q^2 N_D}}$) is less than 30 nm in such films because $t_{film} > t_{SC} \sim 3L_D$. It is clear that the doping concentration N_D of the film is greater than $2*10^{16}$ cm^{-3}. The doping concentration in the range of $2*10^{16}$ - $1*10^{17}$ cm^{-3} (fig. 3) does not significantly change the conductivity of the film. This means that polysilicon film has many acceptor type interface states (more than $1*10^{17}cm^{-3}$) which can compensate donor impurities. Thus, the acceptor type interface state density is not less than $1*10^{17}$ cm^{-3} in the studied undoped polysilicon films.

Since the 100 nm thickness films are not depleting, we can determine the parameters of the film with the surrounding dielectrics independently. Note that it is possible to determine the carrier mobility in polysilicon films using equation (2) if the height of potential barrier at the GB is considerably (1-2 order of magnitude) less than heat potential kT (exponent tends to unity). The height of the barrier at GB decreases with increasing the gate voltage V_{BG} and pulling voltage V_{DS} [14]. As follows from fig. 4, comparable values in the open state I_{ON} for transistors on the polysilicon and SOI (i.e. condition when the potential barrier on the GB can be neglected) are observed for transistors on polysilicon at V_{DS} no less than 1 V. Therefore, the effective low field carrier mobility in polysilicon films was estimated at V_{DS}=1 V.

Table II presents the values of the effective state density and low field carrier mobility for the polysilicon films thickness of 30-100 nm. For comparison, the table II also gives the parameters for SOI film thickness of 30 nm.

TABLE II
PARAMETERS OF POLYSILICON FILMS AND SOI

Film's thickness, nm		D_{IT}, $eV^{-1}cm^{-2}$	μ_e, $cm^2/V*s$
27		$3.72*10^{12}$	2.1
47		$7*10^{12}$	2
100	PolySi/Ox (interface with TG)	$2.4*10^{12}$	3
	PolySi/BOX (interface with BG)	$4.7*10^{12}$	3.1
30 (SOI)		$1*10^{12}$	900

It can be seen that the value of effective low field mobility is almost independent of the film thickness, and is about ~2-3 $cm^2/V*s$. The effective interfaces state density for film thickness of 27 nm and 47 nm is $3.7*10^{12}$ $eV^{-1}cm^{-2}$ and $7*10^{12}$ $eV^{-1}cm^{-2}$, respectively. It should be noted that the interface state density in polysilicon is an effective value and is determined by the states on the PolySi/SiO_2 heterointerface and the states at the GB. Large values of D_{IT} for this film may be associated with the open surface. The transistors based on 100 nm polysilicon films are protected by a gate dielectric. The PolySi/Ox interface was formed during thermal oxidation of polysilicon, while the PolySi/BOX interface was formed by deposition of polysilicon on oxidized substrate. As can be seen from Table II, D_{IT} value for PolySi/Ox interface is almost 2 times less than for PolySi/BOX interface.

IV. CONCLUSION

The electrical properties of polysilicon thin films with thickness of 27, 47, and 100 nm grown by CVD process on SiO_2/Si substrates were investigated. It is shown that the

effective state density at the interfaces with dielectric and grain boundaries of film is equal to $2.4*10^{12}$ $eV^{-1}cm^{-2}$ and $4.7*10^{12}$ $eV^{-1}cm^{-2}$ for heterointerfaces, fabricated by thermal oxidation of polysilicon and by deposition of polysilicon on oxidized substrate, respectively. The value of effective low-field carrier mobility does not depend on film thickness and is about 2-3 $cm^2/V*s$. However, transistors based on such polysilicon films have low leakage currents ($I_{LK} < 1*10^{-11}$ A) and a high switching ability ($I_{ON}/I_{OFF} > 10^5$) that define their usage in many electronic devices.

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