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Analytical Model for Inverter Design using Floating Gate Graphene Field Effect Transistors

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***Abstract*— With device dimensions reaching their physical limits, there has been a tremendous focus on development of post CMOS technologies. Carbon based transistors, including graphene and carbon nanotubes, are seen as potential candidates to replace traditional CMOS devices. In that, floating gate graphene field effect transistors (F-GFETs) are preferred over dual gate graphene field effect transistors (D-GFETs) due to their ability to provide variable threshold voltage using a single power supply. In this paper, we present a novel analytical model for the design of a complementary inverter using floating gate bilayer graphene field-effect transistors (F-GFETs). Our proposed model describes the *i-v* characteristics of the F-GFET for all the regions of operation considering both hole and electron conduction. The *i-v* characteristics obtained using our model are compared with that of D-GFETs . Based on our proposed model, we obtain the transfer characteristics of a complementary inverter using F-GFETs. Our proposed inverter gives better transfer characteristics when compared with previously reported inverters using either F-GFET or chemically doped D-GFETs.**

***Keywords*— Bilayer graphene, graphene field effect transistors, complementary inverter, i-v characteristics, transfer characteristics.**

I. INTRODUCTION

Current CMOS technology cannot meet the challenges placed by the International Technology Semiconductor Roadmap [1], due to device dimensions reaching their physical limits. In the sub-10 nm scale, silicon MOSFETs face the problems of quantum effects and the effects associated with long range Coulomb potential [2]. To meet these challenges we need to look for new architectures [3] and novel materials for the channel, the gate stack and the contacts. Carbon allotropes, like carbon nanotubes [4] and graphene nanoribbons (GNRs) [5] have attracted the attention of scientific community in the last decade. Carbon nanotubes face the problem of compatibility with the current CMOS lithographic processes due to their non-planar structures. On the other hand, GNRs offer superior electrical characteristics along with ease of fabrication including higher career mobility [6], high cutoff frequencies in the order of 100 GHz [7-8] and compatibility with the current CMOS lithographic processes due to its 2-D structure [9]. Bulk graphene is zero band gap material, thereby offering metallic properties. However, cutting graphene in planar ribbon like structures called graphene nanoribbons (GNRs) increases the bandgap, thus making it suitable for transistor applications [10].

Recently, there have been various successful attempts at fabricating GNR based field-effect transistors (GNRFETs). In that, *p*-type and *n*-type GNRFETs are used for construction of functional devices, such as complementary inverters. Here threshold voltage (Dirac point) is kept variable [11]. Initially, top-gate GNRFETs were fabricated, but they suffered from lower on/off current ratio (typically around 5). On the other hand, dual gate GNRFETs (D-GFETs) offer superior on/off current ratio (typically 100 at room temperature and 2000 at 20 K) [12]. The Dirac point in D-GFETs is set by the applying suitable back gate voltage. Therefore, in case of a complementary inverter, one would need separate back gate voltages and to set the Dirac points for achieving the p-type and n-type behavior. We would need three different voltage sources (one as power supply and two for back-gate voltages) for proper functioning of the inverter. However, use of separate back gate voltage results in complex routing and an additional power supply for each transistor. Surface chemical-molecular doping as proposed by authors in [11] can be used to achieve a common back-gate voltage for all transistors. However, one still requires two voltage sources. Additionally, a very high common back gate voltage is required to achieve reasonable on/off current ratio. Therefore, we need a alternate approach to Graphene FET-based inverter design where the requirements of tunable threshold voltage and high on/off current ratio can be achieved using a single power supply.

Authors in [13] proposed an FET in which semi-permanent charge storage was possible using a floating gate. The concept of floating gate is used to achieve tunable threshold voltage in silicon-on-insulator CMOS as reported by authors in [14]. Similarly, floating gate can also be used in Graphene FETs to achieve the necessary threshold voltage as shown in [15]. The threshold voltage of the channel is controlled using charge injection into the floating gate. The aim of this paper is to contribute to the design and analysis of F-GFET based complementary inverter by formulating an accurate analytical model. In that, we report analytical model for the i-v characteristics of the F-GFET and the transfer characteristics of inverter designed using F-GFETs. The analytical model is preferred over Monte Carlo simulations and master equation methods [16-17] due to lesser computation time. Authors in [8] have proposed the channel resistance equation for F-GFETs. However, the proposed equations are valid only for the linear region of operation. On the contrary, our analytical model computes the drain current that is valid over all regions of the transistor operation. In our analysis, we have used voltage dependent equivalent resistor model for designing a complementary inverter and obtaining its voltage transfer characteristics. When compared with a F-GFET [18] and a chemically doped D-GFET [11], we obtain better transfer characteristics without additional processing steps or supply voltage requirements . Our proposed model provides physical insights into the factors that control the behavior of G-FETs. It is seen that the charge present on the floating gate and its position from the graphene channel can be used to optimize the *i-v* characteristics and voltage transfer characteristics of the F-GFET.

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The remainder of the paper is organized as follows: In Section II, the closed form analytical model for the *i-v* characteristics of F-GFETs has been proposed. Based on our analytical model for F-GFETs, we present the design of a complementary inverter. The effect of floating gate charge on the resistance of F-GFET and the transfer characteristics of complementary inverter is presented. Analysis of our model is shown in Section III. The theoretical results obtained using our model are compared with previously reported literature here. The paper concludes in Section IV.

II. PROPOSED MODEL

The schematic of a F-GFET is shown in Fig. 1. A floating gate is placed in SiO_2 substrate between the graphene channel and back gate. There are mainly three capacitances present in the F-GFET. C_g is the capacitance between top-gate and the graphene channel, C_{fch} is the capacitance between the graphene channel and the floating gate while a capacitance, C_{fb}, exists between the floating gate and the back-gate. Here, V_f and V_b are the potentials of the floating gate and back-gate, respectively while V_s and V_d represent the source and drain potentials respectively.

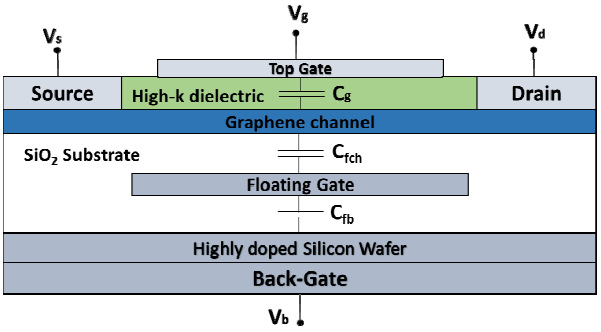


Fig. 1 Schematic of a floating gate Graphene NanoRibbon Field Effect Transistor (GNRFET).

Due to the graphene channel, an additional quantum capacitance, C_q, will be added in series with the two capacitances, C_g and C_{fch}. Therefore, the equivalent top-gated capacitance, C_{top}, will be $C_g . C_q /(C_g + C_q)$ and the equivalent back-gate capacitance, C_{back}, will be $C_{fch} . C_q /(C_{fch} + C_q)$. The threshold voltage (V_0) and floating gate potential (V_f) can be computed using the capacitances, C_{top} and C_{back}, as given by [18] as:

$$V_0 = V_{gs}^0 + \frac{C_{back}}{C_{top}}(V_{fs}^0 - V_{fs}) \tag{1}$$

Here, V_{gs}^0 is the top gate-source voltage at the Dirac point, V_{gs} is the top gate-source voltage, V_{fs} is the floating gate–source voltage, and V_{fs}^0 is the floating gate-source voltage at the Dirac point.

$$V_f = \frac{Q_{fb} - C_{top}(V_{gs} - V_{gs}^0)}{C_{back} + C_{fb}} + \frac{C_{back}(V_s + V_{fs}^0) + C_{fb} V_b}{C_{back} + C_{fb}} \tag{2}$$

where, Q_{fb} is the charge density on the floating gate.

Fig. 2 shows the typical current voltage characteristics of graphene FETs. The *i-v* characteristic of a floating gate bilayer graphene FET is divided into three regions: triode region, unipolar saturation region and ambipolar saturation region. In the triode and unipolar saturation regions, carrier transport is either due to holes or electrons, while in the ambipolar saturation region, the carrier transport is due to both electrons and holes. Therefore, there is need to develop an analytical model that gives the drain current expressions for each of these three regions. We have used the characteristics equation given by authors in [19] to derive the drain current equation for F-GFETs.

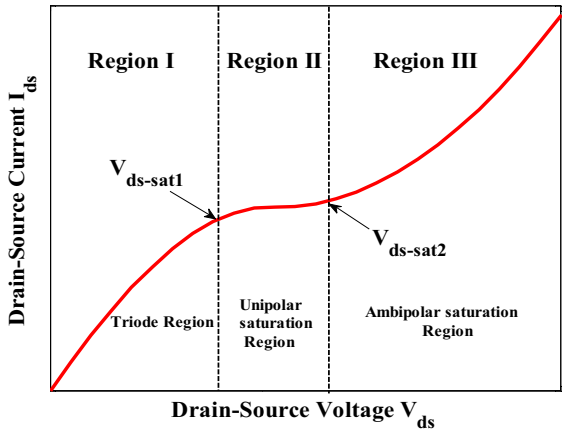


Fig. 2. Typical current-voltage characteristics of Graphene Field Effect Transistors (GFETs)

In that, the threshold voltage, V_0 obtained using (1) is substituted in the current equations. Current is calculated in terms of charge density at a given point of channel. It is then integrated over entire channel to get the drain source current expressions for various regions of operation in F-GFET as given below.

A. *Hole conduction*

***1) Triode region*:** The drain-source current is expressed as:

$$I_{ds} = \frac{-1}{4R_c}\left[\frac{Lv_{sat}}{\mu} - V_{ds} + 2Wv_{sat}C_{top}R_c\left(\frac{V_{ds}}{2} - V_{ov}\right) - \sqrt{\left(\frac{Lv_{sat}}{\mu} + V_{ds} + 2Wv_{sat}C_{top}R_c\left(\frac{V_{ds}}{2} - V_{ov}\right)\right)^2 - 4\frac{Lv_{sat}}{\mu}V_{ds}}\right] \tag{3}$$

where, $V_{ov} = V_{gs} - V_o$ is the overvoltage and R_c is the series resistance at both the drain and source terminals, V_{ds} is the drain-source voltage, L is the length of the graphene channel, v_{sat} is the saturation velocity.

***2) Unipolar Saturation Region*:** $V_{ds-sat1}$ is the value of drain-source voltage where the F-GFET moves from the triode region to the unipolar saturation region and is given by:

$$V_{ds-sat1} = \frac{1}{(1+\mathrm{Wv}_{sat} C_{top} R_c)^2}\Big[2V_{ov}\,\mathrm{Wv}_{sat} C_{top} R_c (1+\mathrm{Wv}_{sat} C_{top} R_c) + (1-\mathrm{Wv}_{sat} C_{top} R_c)\left(\frac{Lv_{sat}}{\mu} - \sqrt{\left(\frac{Lv_{sat}}{\mu}\right)^2 - 2\frac{Lv_{sat}}{\mu}V_{ov}(\mathrm{Wv}_{sat} C_{top} R_c + 1)}\right)\Big] \tag{4}$$

The saturation current in this regions is given by:

$$I_{ds-sat} = \frac{Wv_{sat} C_{top} R_c}{R_c (1+Wv_{sat} C_{top} R_c)^2}\left[-\frac{Lv_{sat}}{\mu} + (1+Wv_{sat} C_{top} R_c)V_{ov} + \sqrt{\left(\frac{Lv_{sat}}{\mu}\right)^2 - 2(1+Wv_{sat} C_{top} R_c)\frac{Lv_{sat}}{\mu}V_{ov}}\right] \tag{5}$$

***3) Ambipolar Saturation Region*:** The ambipolar region exhibits an additional displacement current that is given by:

$$I_{disp} = -\frac{W}{2L}\mu_n(\mathrm{C}_{top})V_{ds-sat2}^2\left(\frac{V_{ds}}{V_{ds-sat2}} - 1\right)^2 \tag{6}$$

where, μ_n is the mobility of minority charge carriers, W is the channel width and $V_{ds-sat2}$ is the drain-source voltage when the F-GFET moves from unipolar saturation region to ambipolar saturation region. The drain-source voltage, $V_{ds-sat2}$, is given by:

$$V_{ds-sat2} = V_{ds-sat1} - \frac{1}{2}\left(|V_{ov} - V_{ds-sat1}|\right) \tag{7}$$

In the ambipolar saturation region, current increases due to the flow of minority charge carriers. These minority charge carriers arise due to kink effect [19-20] and can be modeled by adding displacement current, I_{disp}, in the existing drain current expression for the unipolar saturation region. The drain-source current in this region is therefore given by:

$$I_{ds} = I_{ds-sat} + I_{disp} \tag{8}$$

B. Electron conduction

Based on the above discussion, we now obtain the analytical expressions for the case of electron conduction.

1) Triode region: The drain-source current is expressed as:

$$I_{ds} = \frac{1}{4R_c}\left[\frac{Lv_{sat}}{\mu} + V_{ds} - 2Wv_{sat} C_{top} R_c\left(\frac{V_{ds}}{2} - V_{ov}\right) - \sqrt{\left(-\frac{Lv_{sat}}{\mu} + V_{ds} + 2Wv_{sat} C_{top} R_c\left(\frac{V_{ds}}{2} - V_{ov}\right)\right)^2 + 4\frac{Lv_{sat}}{\mu}V_{ds}}\right] \tag{9}$$

2) Unipolar Saturation Region: Similar to hole conduction, $V_{ds-sat1}$ can be expressed as:

$$V_{ds-sat1} = \frac{1}{(1+\mathrm{Wv}_{sat} C_{top} R_c)^2}\Big[2V_{ov}\,\mathrm{Wv}_{sat} C_{top} R_c (1+\mathrm{Wv}_{sat} C_{top} R_c) + (\mathrm{Wv}_{sat} C_{top} R_c - 1)\left(\frac{Lv_{sat}}{\mu} - \sqrt{\left(\frac{Lv_{sat}}{\mu}\right)^2 + 2\frac{Lv_{sat}}{\mu}V_{ov}(\mathrm{Wv}_{sat} C_{top} R_c + 1)}\right)\Big] \tag{10}$$

The saturation current, I_{ds-sat}, is expressed as:

$$I_{ds-sat} = \frac{Wv_{sat} C_{top} R_c}{R_c (1+Wv_{sat} C_{top} R_c)^2}\left[\frac{Lv_{sat}}{\mu} + (1+Wv_{sat} C_{top} R_c)V_{ov} - \sqrt{\left(\frac{Lv_{sat}}{\mu}\right)^2 + 2(1+Wv_{sat} C_{top} R_c)\frac{Lv_{sat}}{\mu}V_{ov}}\right] \tag{11}$$

3) Ambipolar Saturation Region: The displacement current is given by:

$$I_{disp} = \frac{W}{2L}\mu_n(\mathrm{C}_{top})V_{ds-sat2}^2\left(\frac{V_{ds}}{V_{ds-sat2}} - 1\right)^2 \tag{12}$$

where, $V_{ds-sat2}$ is given by:

$$V_{ds-sat2} = V_{ds-sat1} + \frac{1}{2}\left(|V_{ov} - V_{ds-sat1}|\right) \tag{13}$$

Similar to the case of hole conduction, the drain-source current can be obtained using (8) for the case of electron conduction also.

It is a well known fact that FETs act as voltage dependent resistors. This assumption is being used in our work to obtain the transfer characteristics of the complementary inverter. Till now, we have developed the current equations for each region of operation of a single F-GFET. Equations (1)-(13) are now used to compute the channel resistance that is seen to be dependent on the biasing conditions. Expression for the channel resistance has been obtained by differentiating drain-source current with respect to the drain-source voltage for varying values of gate-source voltage, V_{gs}. The proposed F-GFET can be made to work as a *p*-FET and *n*-FET device by adjusting the threshold voltage, V_0, which is dependent on the charge present on the floating gate. The amount of charge on the floating gate is preset at the time of fabrication. The equivalent voltage dependent resistor model of a F-GFET based complementary inverter is given in Fig. 3. In Fig. 3, the output voltage, V_{out} is given by:

$$V_{out} = \left(\frac{R_n(\mathrm{V}_{gs})}{R_p(\mathrm{V}_{gs}) + R_n(\mathrm{V}_{gs})}\right)V_{DD} \tag{15}$$

The resultant transfer characteristics for the F-GFET based inverter can now be obtained using the expression given in (15). Based on the above expressions, we are now in a position to obtain the *i-v* characteristics of an F-GFET using our analysis and design a complementary inverter circuit. We now present the analysis of F-GFET and floating gate GNRFET

based inverter using on our proposed model in the following section.

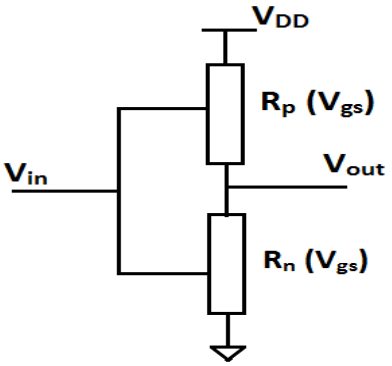


Fig. 3. Voltage dependent equivalent resistor model of a complementary inverter.

III. Results and Discussion

Table 1 summarizes the design parameters that are being used in our proposed model. For performance comparison between our results and existing data, we have used typical design parameters that have used for both floating and dual gate GFETs, as given in [18-19].

Table 1: Design parameters for our proposed model

Model parameters	Value	Description
L(μm)	1	Channel length
W(μm)	2.1	Channel Width
t_{ox} (nm)	15	Hafnium Oxide Thickness
C_q (μFcm^{-2})	2	Quantum capacitance
k_1	16	Hafnium oxide relative dielectric
k_2	3.9	Silicon oxide relative dielectric
V_{gs}^0 (V)	1.45	Top-Gate to source Dirac Voltage
V_{bs}^0 (V)	2.7	Back-Gate to source Dirac Voltage
R_s (Ω)	1000	Series resistance
μ(cm^2/Vs)	300	Mobility
H_{sub} (nm)	285	Floating gate to channel thickness
X_{fg} (nm)	285	Floating gate to back gate thickness

Figs. 4 and 5 show the current voltage characteristics for hole conduction and electron conduction for a F-GFET, respectively. The value of V_{ds} varies from 0 to $V_{ds-sat1}$ in the triode region, from $V_{ds-sat1}$ to $V_{ds-sat2}$ in the unipolar saturation region and from $V_{ds-sat2}$ to V_{DD} in the ambipolar saturation region. In first two regions, source-drain current, I_{ds} increases with increasing V_{gs} while in the ambipolar saturation region this trend is reversed. The occurrence of ambipolar saturation region is dependent on the overvoltage parameter, V_{ov}.

Fig. 6 shows the *i-v* characteristics for the F-GFET and D-GFET [21]. For comparison with our results, the drain-source currents for the D-GFET have been plotted for a back gate voltage of zero volts. It is seen that the current in our proposed model is higher than that of a D-GFET. This difference is attributed to increased capacitance due to the presence of a floating gate. As explained earlier the voltage transfer characteristics depends on the value of the charge present on floating gate. The F-GFET with higher charge depicts *p*-type behavior while that with lower charge depicts *n*-type behavior.

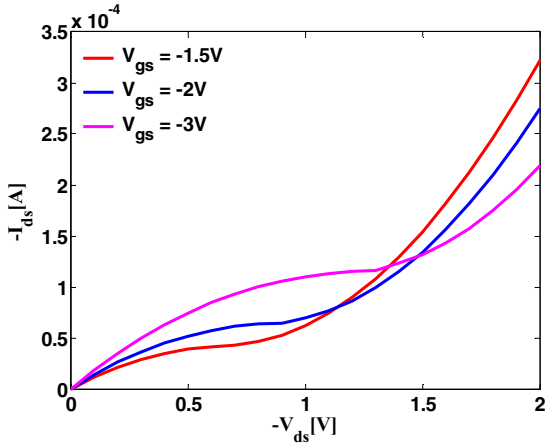


Fig. 4. *i-v* characteristics for the hole conduction in F-GFET with V_{bs} = -2 V. V_{ds} is varied from 0 to -3 V for top gate voltages of -1.5 V, -2 V and -3 V.

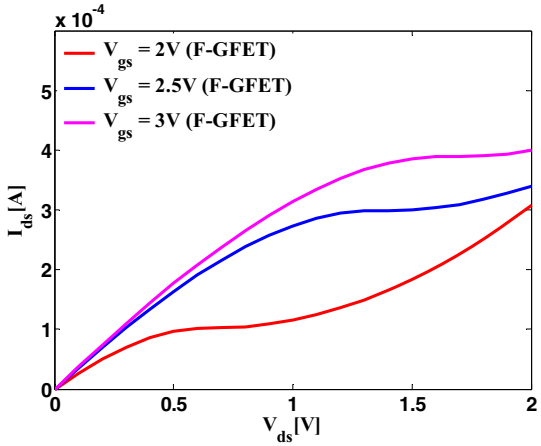


Fig. 5. *i-v* characteristics for the electron conduction in F-GFET with V_{bs} = 0 V. V_{ds} is varied from 0 to 3 V for top gate voltages of 2 V, 2.5 V and 3 V.

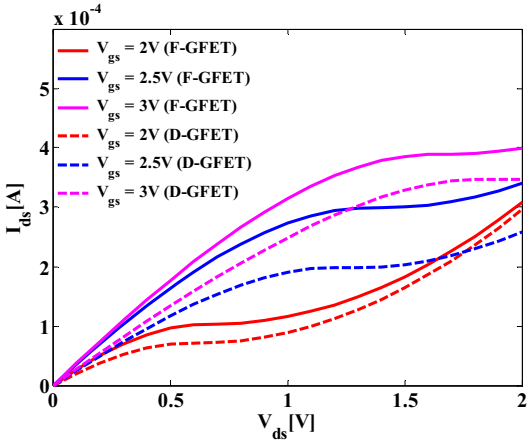
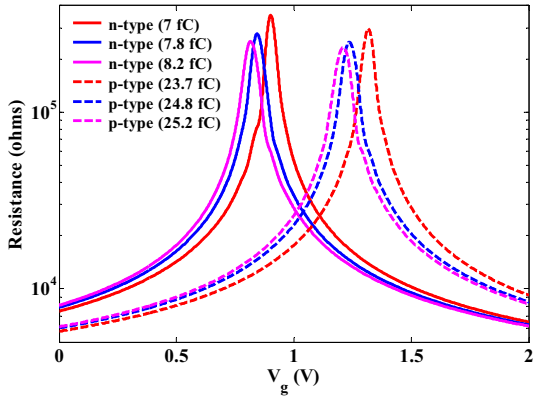


Fig. 6. I_{ds} versus V_{ds}. Comparison between analytical results obtained for F-GFET with D-GFET experimental data [21].

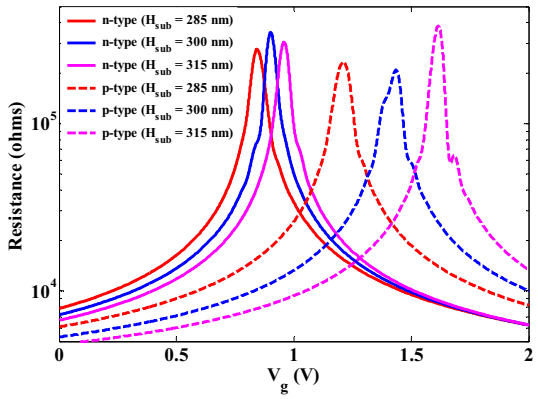
Figs. 7a and 7b show the channel resistance versus gate voltage and distance between channel and floating gate,

respectively, for both *n*-type and *p*-type F-GFETs. The gate voltage at which the peak of the channel resistance is obtained is the threshold voltage of the F-GFET. In Fig. 7a, the effect of floating gate charge on the channel resistance is shown. It is seen that the threshold voltage of the F-GFET depends on the value of gate charge. Also, by varying the gate charge, the same device can be made to work either as a p-type or an n-type transistor. The distance between the floating gate and the graphene channel can also be used to operate the device either as a p-type or an n-type transistor and change the threshold voltage of the F-GFET, as shown in Fig. 7b.

Fig. 8 shows the variation in the voltage transfer characteristics for different value of floating gate charge. In that, we have obtained transfer curve with increasing floating charge value for both n-type and p-type GFETs. We can conclude that the transition point from high to low logic shifts towards the left with increasing floating gate charge. In this process, the switching speed of the complementary inverter remains constant. It is also seen that the transfer characteristics obtained using our model is similar to the one obtained from a chemically doped D-GFET reported in [11], which is shown in the inset. Here, we obtain better voltage swing in our F-GFET based complementary inverter model than that reported in [11] with no additional processing steps or back-gate voltage.



(a)



(b)

Fig. 7. Variation of resistance of F-GFETs with gate potential (a) for different value of floating gate charge (H_{sub} is 285 nm is assumed), (b) for different floating gate position from graphene channel (Q_n and Q_p are assumed as 7.8 fC and 25.2 fC respectively). The solid line represents the n-type behavior showing F-GFET while dashed line represent p-type behavior.

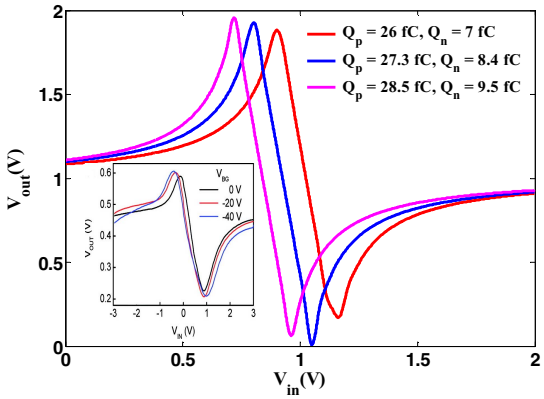
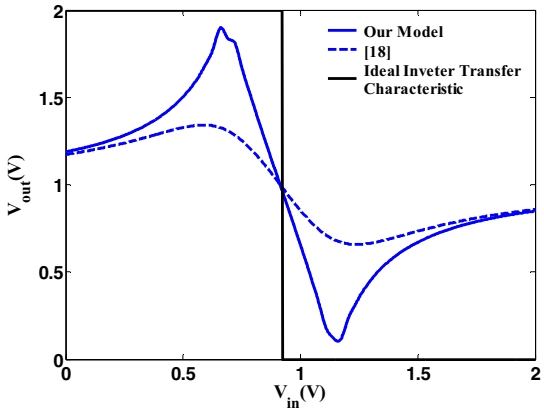
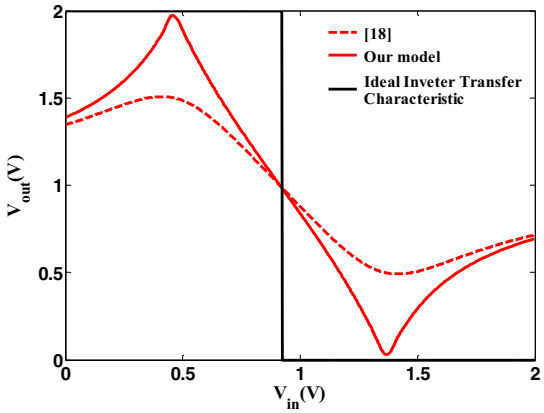


Fig. 8. Variation of voltage transfer characteristics for different values of floating gate charge. Transfer characteristics of a chemically doped D-GFET is shown in the inset [11].

In Figs. 9a, 9b and 9c, voltage transfer characteristics obtained using our analysis is compared with that reported in [18]. In this figure, floating gate charge on one of the F-GFETs is increased while it is decreased on the other. When we increase charge on the GFET, it behaves as p-type; on the other hand when we decrease the charge on the GFET it behaves as n-type. Thus, we can get faster switching from high to low logic at the same transition point.



(a)



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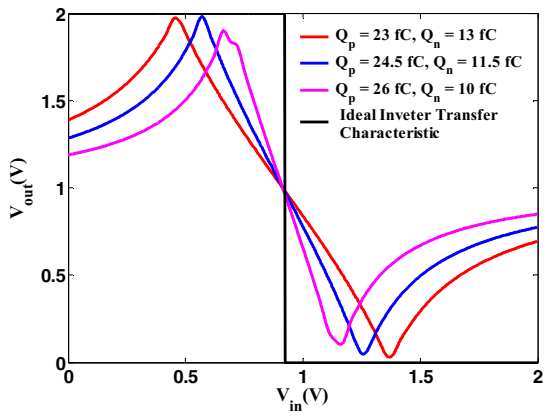

(c)

Fig. 9. Variation of voltage transfer characteristics (a) compared with [18] for value of floating charge Q_n = 10 fC, Q_p = 26 fC, (b) compared with [18] for value of floating charge Q_n = 13 fC and Q_p = 23 fC. (c) for different value of floating gate charge.

From above discussion, it is clearly seen that the charge on floating gate and the distance between the floating gate and channel are the major design parameters to optimize the behavior of the F-GFET. Additionally, floating gate GFETs are easy to fabricate when compared to D-GFETs that require extra processing steps for doping. Also, the F-GFETs do not require extra power supply for providing back-gate voltage, which happens to be another advantage over D-GFETs.

IV. Conclusion

In this paper, we have presented a novel analytical model for the design of a complementary inverter using floating gate bilayer graphene field-effect transistors. Our proposed model describes the *i-v* characteristics of an F-GFET for all the regions of operation considering both hole and electron conduction. Based on our proposed model, we have been obtained the transfer characteristics of a complementary inverter using F-GFETs. The *i-v* characteristics obtained using our model has been compared with that of D-GFETs. Based on our analysis, desired transfer characteristics for the complementary inverter can be achieved by either adjusting the charge at the floating gate or its position with respect to the graphene channel. Our proposed inverter gives better transfer characteristics when compared with previously reported inverters using either F-GFET or chemically doped D-GFETs. In addition, our proposed inverter requires a single supply voltage instead of three supply voltages as in case of D-GFETs. Therefore, F-GFETs can be seen as potential candidate used as transistors in future circuits. It is felt by the authors that complex circuits can also be realized using the proposed complementary inverter model.

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