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A Fault Tolerant 3-phase Adjustable Speed Drive Topology with Active Common Mode Voltage Suppression

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***Abstract*— A fault tolerant adjustable speed drive (ASD) topology is introduced in this paper. A conventional ASD topology is modified to address: a) drive vulnerability to semiconductor device faults b) input voltage sags c) motor vulnerability to effects of long leads and d) achieve active minimization of common mode (CM) voltage applied to the motor terminals. These objectives are attained by inclusion of an auxiliary IGBT inverter leg, three auxiliary diodes, and isolation - reconfiguration circuit. The design and operation of the proposed topology modifications are described for different modes; (A) Fault mode, (B) Active Common Mode Suppression mode and (C) Auxiliary Sag Compensation (ASC) mode. In case of fault and sag, the isolation and hardware reconfiguration are performed in a controlled manner using triacs/anti-parallel thyristors. In normal operation, the auxiliary leg is controlled to actively suppress CM voltage. For inverter IGBT failures (short circuit and open circuit), the auxiliary leg is used as a redundant leg. During voltage sags, the auxiliary leg along with auxiliary diodes is operated as a boost converter. A current shaping control strategy is proposed for the ASC mode. A detailed analysis of CM performance of the proposed topology is provided and a new figure of merit, Common Mode Distortion Ratio (CMDR) is introduced to compare the attenuation of CM voltage with that of a conventional ASD topology. The output filter design procedure is outlined. A design example is presented for an 80 kW ASD system and simulation results validate the proposed auxiliary leg based fault tolerant scheme. Experimental results from a scaled prototype rated at 1 hp are discussed in this paper.**

***Index Terms*— adjustable speed drive, fault tolerant, common mode suppression, voltage sag compensation, common mode distortion ratio**

I. INTRODUCTION

A Motor Drive System (MDS) consists of an adjustable speed drive (ASD), a motor and the grid supply. The use of MDS is widespread in applications like water pumping stations, compressor, crusher and steel rolling mills in petrochemical, cement and steel industry [1]. In a number of these applications, MDS is integral part of a continuous process [2]. Any interruption of the manufacturing process is expensive because of production loss and follow-up costs [3,4]. Therefore the availability of MDS in such applications has an immense financial impact. This has triggered interest in failure modes of both ASDs and motors [1, 5-8]. Other power interruption phenomena like voltage sag/ swells have also been studied extensively [9-11]. These and other factors which affect the reliability of individual subsystems of an MDS are summarized in Figure 1. A detailed review of these issues and existing solutions has been presented in this section.

A. ASD failure modes

A conventional ASD topology is shown in Figure 2. The failure modes of ASD have been studied in various surveys. According to [12], power semiconductor device faults account for about 35% of all ASD faults. In [13], up to 40% of the 3-phase inverter failures in the field are attributed to power transistor failures. Other surveys have estimated that, of all components, power semiconductor device failures cause the most number of ASD failures [13].

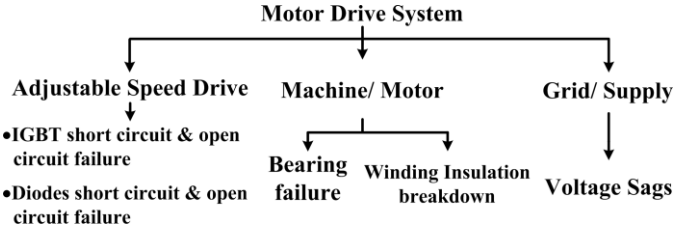

Figure 1. Issues affecting Motor Drive System availability and reliability

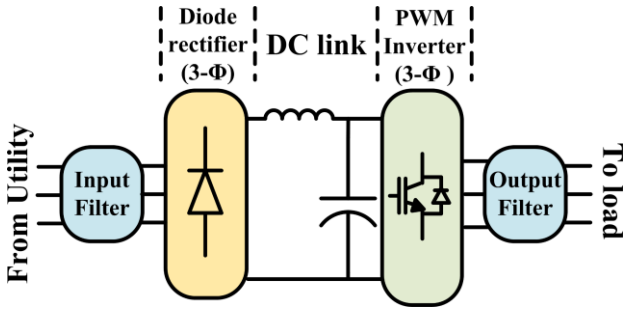

Figure 2. Conventional ASD topology with input and output filter

Semiconductor devices: Modern drives use highly integrated power modules which utilize different materials in their construction [14]. This leads to non-uniform thermo-mechanical stresses and consequently fatigue induced failures [15]. Other failure mechanisms for IGBT due parasitic BJT latch up, V_{CE} overvoltage breakdown due to high dV/dt spikes during turn off, and thermal breakdown have been discussed in [16].

Existing solutions: A number of techniques have been proposed to detect [17-19] and mitigate effects of semiconductor device failures [20, 21] in voltage source inverters. A detailed review of published fault detection techniques is provided in [22] and fault tolerant inverter topologies have been presented in [6] and [23]. Fault tolerance is typically achieved by introducing redundancy or added complexity. Amongst them three techniques are popular. First approach is to connect the faulty phase to DC link mid-point using triacs [24]. Second approach is to isolate the faulty phase and connect the motor neutral to the DC link mid-point [25]. A third approach is to introduce an additional leg which is connected to the motor neutral [26]. In all these cases, the semiconductor devices are oversized and the inverter output power during fault mode operation is limited and the DC bus capacitors need to be oversized. In the first and second approaches, access to DC bus mid-point is required whereas the third approach handles only open circuit faults and a fourth

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wire is needed which adds to the cost. More recently, phase redundant approaches [13, 27-29] have gained popularity due to 100% post fault output capabilities without drive overrating. A detailed cost and feature comparison of different fault tolerant topologies is presented in [5].

B. Motor failure modes

Motor failures also affect the availability of a motor drive system. According to the data from commercial installations [8], bearing and winding failures together account for 70% of machine failures. High frequency bearing currents contribute to bearing failures and large voltage overshoots result in winding insulation breakdown.

1. Motor bearing failures

A modern motor drive uses high frequency PWM which results in high frequency common mode neutral-ground voltage. This voltage induces high frequency motor bearing currents [30, 31] which gradually erode the bearing races [8, 32] and lead to early mechanical failures. Electrical grounding also plays a vital role in determining the magnitude and generation mechanism of bearing currents [33, 34].

Existing solutions: The existing solutions to the problems of bearing currents and common mode voltage fall under one of the following two categories. Firstly, the motor installation could feature: insulated or ceramic bearings, grounding brush contact and insulated coupling methods [34]. Additional filter components (dV/dt or sinusoidal output filters) can also be installed to modify the shape of inverter output. Secondly, modification to the inverter could be made, such as: a dual inverter bridge approach open winding [35, 36] and double winding machines [37]. Alternative approaches involving auxiliary inverter have been illustrated in [38, 39]. Another method proposed in [40] involves the use of an additional half bridge to actively cancel common mode voltage.

2. Motor winding

High frequency PWM inverters with long lead cables can cause large voltage overshoots at the motor terminals. Magnetic wire insulation life curves shown in [41] illustrate the effect of increasing cable length and switching frequency. Prolonged voltage stresses lead to gradual deterioration of the insulation material and ultimately result in catastrophic failures.

Existing solutions: Three methods are widely used to mitigate the effect of high voltage stresses- inverter output reactors, inverter output filters [42-44] and cable termination filters [45]. The dV/dt limit is dependent on the length and electrical properties of the cable and reflection coefficient of the load. For instance, in [37] critical rise time is restricted to 2.5μs for a 30m cable. A review of different mitigation techniques has been presented in [46].

C. Grid Power Interruption

Voltage sag: Based on power quality surveys [11] and standards [47-49], an input voltage drop by more than 13% and longer than one half cycle can lead to MDS trips. Although a trip protects the power electronic components during sag, it can lead to production loss [3, 4, 47, 49]. In continuous process industry applications, this could have a significant financial impact.

Existing solutions: An overview of voltage sag compensation techniques has been presented in [50]. Hardware intensive techniques such as auxiliary boost converter, a two stage AC-DC conversion (diode rectifier followed by boost converter), PWM rectifier front end and energy storage based topologies use additional components [4, 50]. At the distribution level, Dynamic Voltage Restorer (DVR) compensates for upstream disturbances using energy storage [51].

As discussed above, the factors affecting MDS failure modes (Figure 1) have been studied rigorously in the literature. Though a number of different solutions exist which address these problems separately, none of the discussed approaches tackle all these issues with a single solution. In order to simultaneously address the issues of fault tolerance, common mode voltage, overvoltage at motor terminal and grid voltage sags, a combination of approaches discussed in section (I.A), (I.B) and (I.C) is required, which makes the system design complex. This paper develops a single approach to mitigate all these factors by modifying a conventional drive topology.

The fault tolerant non-regenerative AC motor drive system proposed in this work is shown in Figure 3. The topology consists of a three phase diode rectifier (*D1-D6*) and auxiliary diodes (*D7-D9*) followed by a 4-leg inverter ($S_{1A\text{-}D}$ and $S_{4A\text{-}D}$) along with isolation (T_{si} and $T_{fia\text{-}d}$) and reconfiguration (T_{sr} and $T_{fra\text{-}d}$) circuits for sag and fault mode operations. During normal operation the 4th leg, hereby known as auxiliary leg (S_{1D} and S_{4D}), is coupled to the conventional 3 phase inverter topology using the output filter. This auxiliary leg enables active common mode suppression by imposing a voltage at the inverter output which is equal but opposite to the common mode voltage magnitude. In grid phase voltage sag scenario, this auxiliary leg (S_{1D} and S_{4D}) and diodes (*D7-D9*) form a boost converter to achieve sag compensation. For fault mode operation, this auxiliary leg replaces the faulty leg after hardware reconfiguration. The output filter on the inverter side smoothens out dV/dt transitions which reduces voltage overshoots at motor terminals. Thus, the proposed system reduces vulnerability to device faults, bearing currents, winding breakdown and voltage sag. This system has various advantages:

- A single auxiliary half bridge (S_{1D} and S_{4D}) performs multiple tasks: (a) fault tolerance capability during open and short circuit device faults, i.e. S_{1D} and S_{4D} along with T_{si}, T_{fib}, T_{fic}, T_{fra} (all on assuming inverter phase A is faulty); (b) active common mode suppression during normal operation: i.e. with S_{1D} and S_{4D} along with T_{fia}, T_{fib}, T_{fic} and T_{si} (all on) and (c) sag compensation during voltage sags: i.e. with S_{1D} and S_{4D} along with T_{sr}, T_{fia}, T_{fib}, T_{fic} (all on).
- Modular design of proposed fault tolerant modifications and simple control strategy enables retro-fit capability.
- Active common mode suppression reduces the size of the common mode filters.

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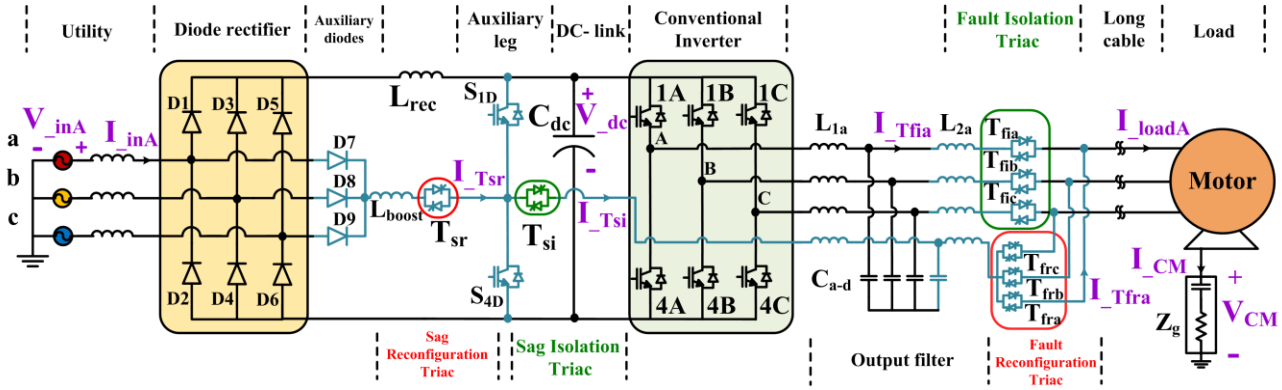

Figure 3. Proposed fault tolerant ASD topology with Auxiliary leg (S_{1D},S_{4D}) and diodes (*D7*, *D8*, *D9*), Isolation (T_{si}, T_{fia}, T_{fib}, T_{fic}) and Reconfiguration (T_{sr}, T_{fra}, T_{frb}, T_{frc}) circuit

- Operation at full load even under fault conditions.
- The inverter output filter reduces dV/dt at motor terminals for long motor leads.
- Use of anti-parallel thyristors/ triacs/ solid state relays allow fast and controlled system reconfiguration in case of faults and minimize conduction losses [52]. The choice of an appropriate device will depend on the power ratings and conduction loss performances of available options. Recently, reverse blocking bidirectional IGBTs were integrated into an IGBT module which could also be an option in the future. Henceforth, the term "Triac" has been used for the sake of simplicity.

II. Proposed Topology

The design and operation of the proposed fault tolerant ASD topology in Figure 3 is covered in this section, and may be best understood by studying it in four detailed sub-sections: (A) Fault mode operation, (B) Active Common Mode Suppression (ACMS) operation with modulation strategy and filter design, (C) Auxiliary Sag Compensation (ASC) operation with current shaping control strategy, (D) Comparative common mode voltage analysis for 3-leg and 4-leg modulation strategies. The state transition diagram for handover between different operating modes is shown in Figure 4. It is noted that in post fault or ASC operation, ACMS is unavailable. The simulation and experimental results are discussed in the following sections.

A. *Fault mode operation*

Fault tolerant capability is added to a conventional ASD topology by introducing a redundant auxiliary leg (S_{1A} and S_{1D}). This provides fault tolerance in case of open and short circuit failures of inverter IGBTs and anti-parallel diodes. However, failures in the inverter IGBTs and anti-parallel diodes - hereby called devices - are treated as the same in this discussion as they have similar effects on the inverter operation. Fault tolerant operation includes three distinct steps: (i) Fault isolation, (ii) Hardware reconfiguration, and (iii) Post fault control. The proposed topology implements these steps for both open and short circuit device failures.

Typical device open circuit fault detection time for a 3 phase inverter is in the order of milliseconds [22]. Most of the published methods rely on sensing inverter phase currents and their deviation from normal operation to detect open circuit faults. Recently, faster methods have been published which use V_{CE} voltage of the low side device to detect open circuit fault [53]. Since the focus of this work is not fault diagnosis, the detection time for open circuit fault is taken to be 2 ms. For short circuit failure a detection time of 4 µs is used, as modern gate drives employ schemes such as de-saturation protection which can complete fault detection in less than 5 µs [54]. Also, the open circuit and short circuit faults are discussed for IGBT S_{1A} only, however the same discussion is applicable in case of failures in other devices.

The topology schematic in Figure 3 has been simplified (Figure 5) for better understanding of failure mode operation for IGBT S_{1A}. First the open circuit device failure is discussed. During normal operation, triac T_{fia} (fault isolation triac for phase A) is turned on while T_{fra} (fault reconfiguration triac for phase A) is off. When a fault is detected, T_{fia}, T_{fra} and all the inverter switches are turned off. This is done to avoid any catastrophic transients. After a preset wait time of a few hundred microseconds T_{fra} is turned on, and the gating signals of S_{1A} and S_{4A} are applied to S_{1D} and S_{4D} respectively. This completes reconfiguration and update of control strategy. The control of healthy legs (B and C) in post fault operation is unaltered.

The operation under short circuit failure is similar to the above discussion, except for the fault detection time. As discussed before, the detection time for short circuit faults is 4 µs. Once a short circuit failure is detected, the de-saturation protection turns off S_{4A} immediately, and controller temporarily turns off all other switches. The reconfiguration and post fault control strategy is same as the open circuit failure case.

B. *Active Common Mode Suppression operation*

In a conventional 3 phase sinusoidal PWM inverter, three switches are on at any time. This leads to a common mode voltage on the output terminals at each time instant. With an even number of legs and with an appropriate switching strategy, it is possible to ensure that an equal number of output terminals are connected to positive and negative of the DC bus. So if higher order effects like dead-time and DC ripple are neglected, the common mode voltage on the output terminals is zero at each instant. The common mode suppression scheme proposed in [40] is based on this principle. This modulation strategy is used in the proposed topology.

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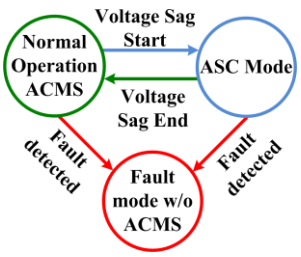

Figure 4. State Transition Diagram for different operating modes

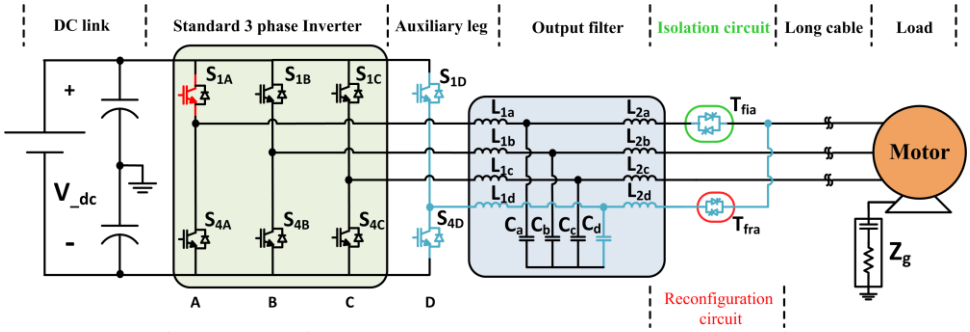

Figure 5. Simplified schematic of the proposed topology to illustrate inverter switch S_{1A} failure ride-through

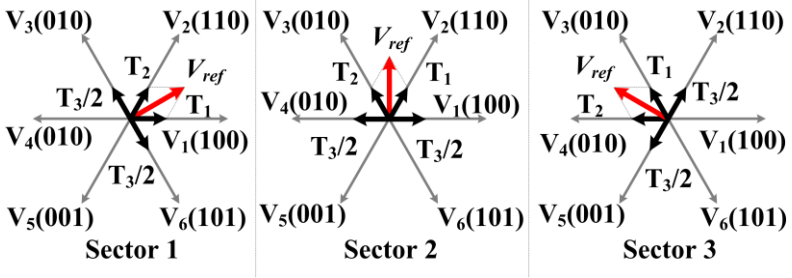

Figure 6. Modulation strategy (AZSPWM) in sector 1-3 (Sectors 4,5 and 6 are not shown)

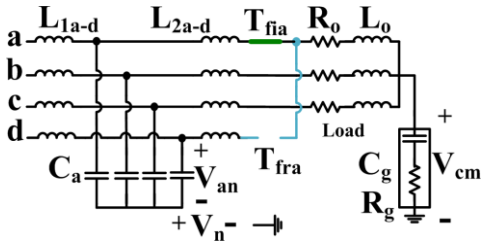

Figure 7. Inverter output filter structure

1. *Modulation strategy*

Different modulation schemes have been proposed to improve the common mode performance of 3 phase voltage source inverters [55-58]. The modulation strategy used in this paper is referred to as Active Zero State PWM (AZSPWM). In AZSPWM strategy zero states of a conventional space vector PWM are replaced with the non-adjacent non zero vectors [59, 60]. This is illustrated in Figure 6. AZSPWM contains third harmonic component which introduces common mode voltage on the output terminals, however this low frequency component has minimal effect on common mode current. This generates the gating signals for three inverter legs. The gating signals for S_{1D} and S_{4D} are generated using logic equation given in (1)

$$S_{1D} = S_{1A} \oplus S_{1B} \oplus S_{1C} \tag{1}$$

2. *Inverter Output Filter*

The auxiliary leg is coupled to the 3 phase inverter by using an output filter shown in Figure 7. The output filter has two functions. Primary function of $L_{1a\text{-}d}$ and $C_{a\text{-}d}$ is to attenuate the switching frequency (f_{sw}) harmonics and suppress common mode voltage. As the higher frequency components are significantly attenuated, the effect of dV/dt on motor terminals is minimized [44]. If all the inductors $L_{1a\text{-}d}$ (L_f) and capacitors $C_{a\text{-}d}$ (C_f) are identical, It can be shown by mathematical analysis that common mode voltages at the load neutral (V_{cm}) and is related to the filtered phase voltages. The transfer function is given in (2).

$$V_{cm} = \frac{4 \cdot (V_{an} + V_{bn} + V_{cn})}{3s^2 L_f C_g + 4(s^2 L_o C_g + s R_o C_g + 3)} \tag{2}$$

From (2), V_{cm} decreases when (V_{an} + V_{bn} + V_{cn}) is reduced. As the sum of filtered phase voltages tends to zero, the common mode voltage will tend to zero. This can be achieved by balancing the phase voltage at fundamental frequency and filtering higher frequency switching harmonics.

The modulation scheme has been analyzed for calculating ripple current (Figure 8). The $I_{pk\text{-}pk}$ ripple is maximum when the volt-sec applied across the inductor L_f is maximum [61]. This occurs when reference vector (V_{ref}) is aligned with V_1, i.e. T_2=0. Using the volt-sec balance principle, the peak to peak ripple current at switching frequency is given by (3).

$$I_{pk-pk} = \frac{d_0 \, d_1 \, V_{dc}}{2 L_f \, f_{sw}} \tag{3}$$

When the reference vector is aligned with V_1 and modulation index is maximum i.e. 1.15, then d_0 and d_1 are given by (4) and (5).

$$d_1 = 2 * \left(\frac{0.866}{2} * \frac{\sin(60° - 0°)}{\sin 60°} \right) + \left(\frac{1}{2} - \frac{0.866}{2} * \frac{\sin(60° - 0°)}{\sin 60°} \right) \tag{4}$$

$$d_0 = \left(\frac{1}{2} - \frac{0.866}{2} * \frac{\sin(60° - 0°)}{\sin 60°} \right) \tag{5}$$

In order to remove switching frequency (f_{sw}) harmonics, the value of filter components are chosen using (6).

$$\frac{1}{2\pi\sqrt{L_f C_f}} \le \frac{f_{sw}}{3} \tag{6}$$

Another factor to consider while designing the filter is the damping coefficient. The damping coefficient for series RLC circuit is given by (7). The value of R_{damp} is chosen to minimize overshoot and power loss.

$$\zeta = \frac{R_{damp}}{2} \sqrt{\frac{C_f}{L_f}} \tag{7}$$

The second function of the filter is to limit the current flow between two filter capacitors during transients. In case of a fault in S_{1A}, during reconfiguration T_{fia} and T_{fra} are both ON for a brief period. Charge exchange between the faulty phase capacitor (C_a) and healthy auxiliary phase capacitor (C_d) takes place and inductors L_{2a}, L_{2d} limit this current transient. The worst case voltage difference between the two filter capacitors (V_{dc}) is used to choose the inductor value (L_2) for limiting this current di/dt transient (8).

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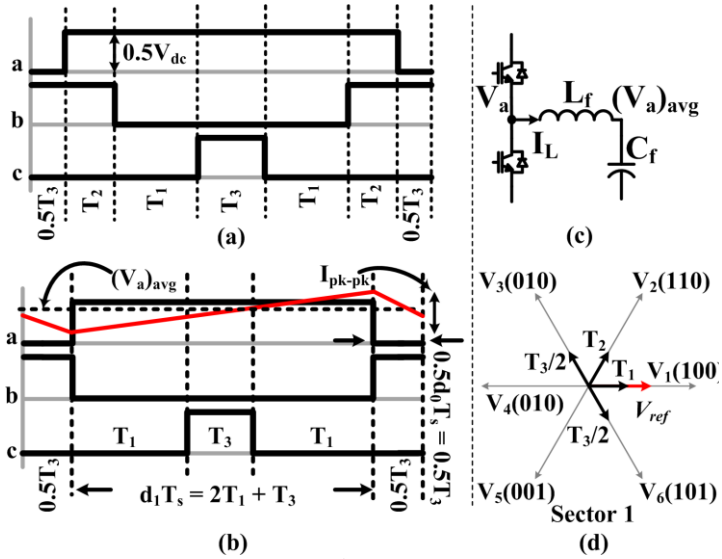

Figure 8. Ripple current analysis for AZSPWM modulation scheme (a) Switching in sector 1, (b) Switching sequence when reference vector is aligned to V_1, (c) Half-bridge representation with filter components (d) Reference vector (V_{ref}) aligned to V_1

$$L_2 \frac{\Delta i}{\Delta t} = V_{dc} \qquad (8)$$

C. Auxiliary Sag Compensation operation

In the proposed topology, sag ride through is achieved by integrating a boost converter in a typical ASD topology [9]. For better understanding of ASC operation, the proposed topology is simplified (Figure 9) to illustrate sag compensation. The components (in blue) added to implement ride through are 3 auxiliary diodes (*D7*, *D8*, *D9*), 2 triacs (T_{si} and T_{sr}) and boost inductor. The sag isolation triac (T_{si}) disconnects the auxiliary leg from output filter. Sag reconfiguration triac (T_{sr}) enables boost converter operation by connecting the auxiliary diodes to the mid-point of the auxiliary leg.

Input line voltages are continuously monitored for detecting voltage sag. When a voltage sag is detected, T_{si} is turned off and T_{sr} is turned on. The front end circuit is now reconfigured with two possible paths. In addition to the regular path through *D1*, *D3* and *D5*, a secondary path is established through the integrated boost converter consisting of *D7*, *D8*, *D9*, boost inductor (L_{boost}), T_{sr}, S_{1D} and S_{4D}.

A current shaping control strategy (Figure 10) is proposed for the ASC mode operation. The conventional voltage and current control loops with PI controller are used. The reference dc bus voltage ($V_{\_dcref}$) is compared with the sensed dc bus voltage ($V_{\_dc}$). This error is the input to a PI controller which generates a scaling factor. The reference current shape V_{rect}' is obtained from the ASC rectified voltage (V_{rect}) as shown in Figure 10.

The LPF block in Figure 10 extracts the DC component of V_{rect}. This shape (V_{rect}') provides a current reference with a DC value superimposed on a low frequency AC component. A factor of 2 allows this shape (V_{rect}') to represent an inverse of V_{rect} or the required boost inductor current shape behavior, i.e. when the voltage is low the boost current should be higher and vice-versa. The boost inductor operates in continuous conduction mode. This shape is scaled to obtain the reference current. This reference is compared with I_{boost} to generate the error signal which is the input to a PI controller. The output of the PI controller is the duty cycle of S_{4D}. The voltage $V_{\_dcref}$ is chosen to be higher than dc bus voltage under normal operation. This helps to reduce the input currents during transients as well as during ASC mode operation and enables lower device ratings.

D. Common mode voltage analysis for 3 leg and 4 leg modulation strategies

The AZSPWM strategy used in the proposed topology reduces common mode voltage significantly. Sinusoidal PWM with conventional 3 leg inverter, AZPWM with conventional 3-leg inverter and AZPWM with 4 leg inverter are simulated to compare the common mode performance of these topologies. The system parameters are summarized in Table 1. The filter parameters are chosen to achieve output power and line to line voltage of 1.p.u.

For modulation index=1, the common voltages of three modulation strategies for the two studied topologies are shown in Figure 11. It is evident that common mode voltage is significantly reduced in case of AZSPWM (4-leg). It is also observed that the higher frequency content of the common mode voltage is reduced. The frequency spectra of the three waveforms shown in Figure 12 clearly illustrate this. A new figure of merit called Common Mode Distortion Ratio (CMDR) is introduced to compare the common mode performance of these three strategies. CMDR defined in (9) is the square root of weighted sum of square of common mode voltage, normalized to fundamental component of differential mode phase voltage.

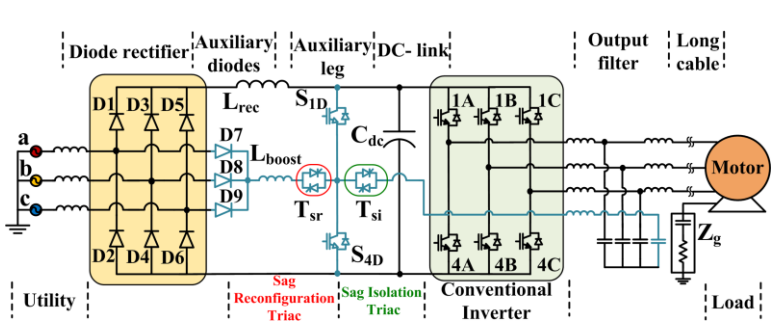

Figure 9. Proposed topology simplified to emphasize sag compensation mode of operation. Components added for sag mode operation are highlighted in blue

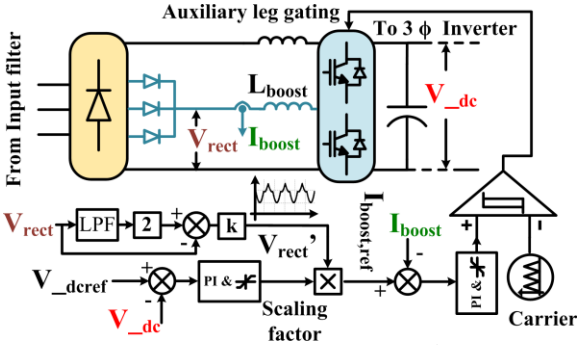

Figure 10. Current shaping based control strategy for Auxiliary Sag Compensation mode operation

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Table 1. Simulation parameters for comparison of Sine PWM and AZSPWM strategies

Simulation Parameter	Value	Simulation Parameter	Value
Output Power	1 p.u.	Load	0.81Ω, 1.04mH
Output Line-Line voltage	1 p.u.	L_f, C_f	7μH,580μF
Load power factor	0.9	V_{dc}	1.633 (p.u.)

$$CMDR = \frac{1}{V_{dm,1}} \sqrt{\sum_{h=1}^{\infty} (h \cdot V_{cm,h})^2} \quad (9)$$

Table 2. A 100 hp 3-phase induction machine parameters

Motor Parameter	Value	Motor Parameter	Value
Power (in hp)	100	r_r (p.u.)	0.015
Stator Line-Line voltage	460 Vrms	X_{ls}	0.10 (p.u.)
Poles	4	X_{lr}	0.10 (p.u.)
Rated slip	0.0175	X_m	3.0 (p.u.)
r_s (p.u.)	0.010		

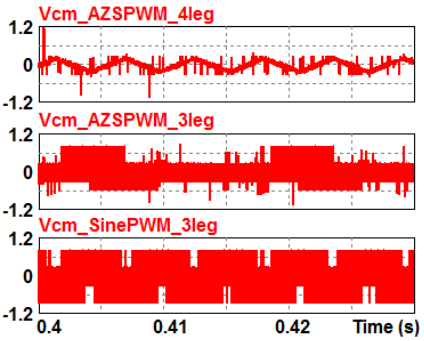

Figure 11. Comparison of common mode voltage for AZSPWM in 4-leg and 3-leg inverter and Sine PWM in 3-leg inverter

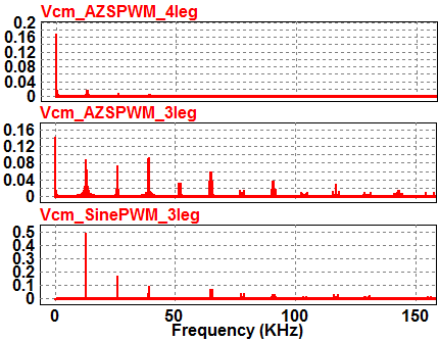

Figure 12. FFT of common mode voltage for AZSPWM in 4-leg and 3-leg inverter and Sine PWM in 3-leg inverter

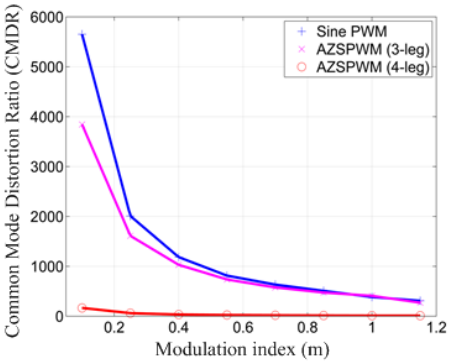

Figure 13. Variation of CMDR with modulation index for Sine PWM (3-leg) and AZSPWM (3-leg and 4-leg) strategies

The variation of CMDR is plotted (Figure 13) with varying modulation index for sinusoidal PWM strategy in 3 leg inverter and AZSPWM strategy in 4 leg and 3-leg inverter. The figure of merit CMDR is helpful to compare the performances of different modulation strategies and their effects on common mode currents. For better common mode voltage performance, a lower CMDR value is desirable.

III. Design Example and Simulation Results

A. Design example and Component sizing

An 80 kW ASD system is designed for a 100 hp 3-phase induction machine. The motor parameters are summarized in Table 2.

The under-voltage lock out condition for the drive has been assumed to be 87% of the nominal dc bus voltage. The drive input overcurrent limit has been taken to be 2 times the peak unfiltered input current ($I_{\_inA}$) under regular operation. For the output current ($I_{\_loadA}$), an instantaneous overcurrent limit of 2 times the peak load current is set to avoid nuisance tripping during fault transients. The input voltage to the drive is 480 V (line-line rms) and dc link voltage ($V_{\_dc}$) is 650V. The values of different passive components are tabulated in Table 3. The DC bus capacitor (C_{dc}) has been overrated to limit the input and output currents during faults. For Z_g, C_g has been calculated from the graph given in [31] and R_g is deduced from impedance measurements between shaft and frame on a motor using LCR meter.

Table 3. Passive component values selected for system simulation

Line side	Value	DC bus	Value	Motor side	Value
Z_{base}	3.1 Ω	Z_{base}	5.6 Ω	Z_{base}	2.8 Ω
L_{in}(60Hz)	0.25 mH (3%)	L_{rec}	220 μH	$L_{1a\text{-}d}$ (60Hz)	40 μH (0.5%)
		C_{dc}	15 mF	$C_{f\,a\text{-}d}$(60Hz)	40 μF
		L_{boost}	250 μH	$L_{2a\text{-}d}$	160 μH (2%)
				C_g, R_g	1 nF, 200 Ω

The ratings for various devices are summarized in Table 4. All the ratings are based on $I_{base,\,rms}$ = 90 A and V_{base} = 480 V. All devices have been de-rated accounting for increased current during full load operation under sag condition. It is noted that if L_{rec} is split between the positive and negative buses, the required L_{boost} value is effectively reduced by $L_{rec}/2$.

Table 4. Summary of component voltage and current ratings

Device	Rating	Device	Rating	Device	Rating
Rectifier diode ($D1$-$D6$)	180Arms (2 p.u.) 1200V(4.33 p.u.)	C_{dc}	1200V (4.33 p.u.)	IGBT ($S_{1A\text{-}D}$ to $S_{4A\text{-}D}$)	1200 V (4.33 p.u.) 200Arms (2.22 p.u.)
Auxiliary diodes ($D7$-$D9$)	180Arms (2p.u.), 1200V (4.33 p.u.)	T_{si}	200Arms (2.22 p.u.) 600V (2.22 p.u.)	L_{1a} to L_{1d}	200Arms (2.22 p.u.)
L_{boost}	180Arms (2 p.u.)	T_{sr}	180Arms (2 p.u.) 600V (2.16 p.u.)	L_{2a} to L_{2d}	200Arms (2.22 p.u.)
T_{fia} to T_{fid}	1200V (4.33 p.u.) 200Arms (2.22 p.u.)	T_{fra} to T_{frd}	1200V (4.33 p.u.) 200Arms (2.22 p.u.)	C_{fa} to C_{fd}	≥600V(2.16 p.u.) 100Arms (1.11 p.u.)
f_{sw_inv}	13 kHz	f_{sw_boost}	10 kHz		

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B. Simulation Results

The proposed topology was simulated for 80 kW ASD system with the parameters in Table 2 and Table 3. This discussion is divided into three parts – (1) Fault mode operation, (2) Sag mode operation, (3) Common Mode Performance. A description of current and voltage parameters, and device labels can be found in Figure 3.

1. Fault Mode operation

The operation of the topology in fault mode was verified for the cases of open circuit fault in S_{1A} (Figure 14 and Figure 15) and short circuit fault in S_{1A} (Figure 16 and Figure 17). The rising edge of the "Fault" pulse in Figure 14 to Figure 17 indicates the start of fault. The falling edge shows the completion of detection. The transient waveforms illustrate that the overcurrent and under-voltage performance of the topology are well within the defined specifications.

The detection times for open circuit and short circuit faults are 2ms and 4µs respectively. It is observed in Figure 16 that the DC bus voltage ($V_{\_dc}$) falls below the under-voltage limit during a short circuit fault transient. When the fault is detected, the gating signals to all the devices are turned off for a period of 10-20 µs. This period ensures that the controller can complete all diagnostic checks before returning to normal operation. It may be seen from Figure 15 and Figure 17 that following a fault, the ASD supplies nominal load current within two cycles (60Hz).

2. ASC operation

The auxiliary sag compensation operation is studied for a phase to neutral sag to 50% and 500 ms long. When a voltage sag is detected, the auxiliary leg and auxiliary diodes are reconfigured to form a boost converter which supplies the DC link capacitor. The boost converter operates at a switching frequency of 10 kHz. The transient performance in ASC operation are shown in Figure 18 to Figure 21.

At t= 0.4 s, input phase C-to-neutral voltage sags to 50% of nominal value and at t=0.9 s returns to nominal value. In sag compensation operation, the DC bus is regulated at 690 V, i.e. approximately 7% higher than regular operation. This restricts the input and output current transients to within the overcurrent limit specified. It can be observed that the input current quality degrades during sag operation, but returns to normal under regular operation. It is to be noted that these currents discussed are un-filtered input currents and the grid-side filtered currents are expected to be of much better quality.

3. ACMS mode operation

The state transition diagram discussed in Figure 4 illustrated that the ACMS mode is the normal mode of operation in the absence of sags and faults. Figure 22 shows the common mode current and voltage in normal and fault mode operations. It may be seen from the voltage waveform that ACMS system, under normal operation, attenuates switching frequency harmonics in the common mode voltage. The normal and post fault common mode current and voltage performances may be compared in Figure 23 and Figure 24. It is observed that high frequency switching harmonics play a great role in determining the common mode current magnitude.

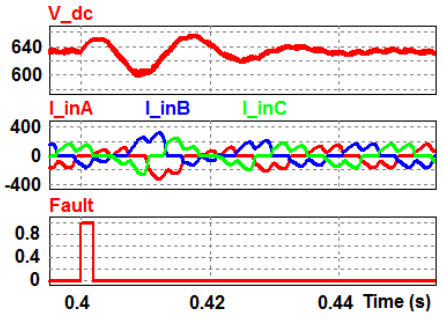

Figure 14. Fault mode operation under open circuit fault introduced at t = 0.4 s. DC bus voltage (volts), unfiltered input currents (amperes) and fault signal are shown

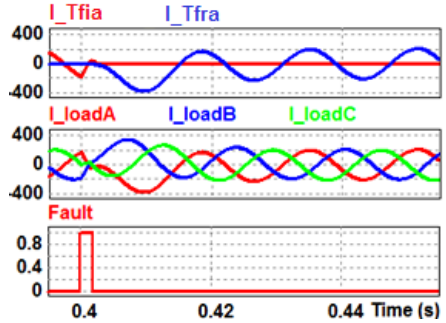

Figure 15. Fault mode operation under open circuit fault introduced at t=0.4 s. Isolation (T_{fia}) and reconfiguration (T_{fra}) triac currents (amperes), load currents (amperes) and fault signal are shown

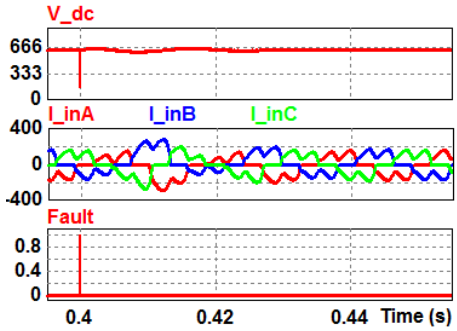

Figure 16. Fault mode operation under short circuit fault at t=0.4 s. DC bus voltage (volts), unfiltered line currents (amperes) and fault signals are shown

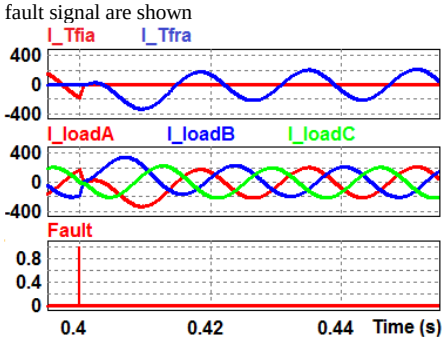

Figure 17. Fault mode operation under short circuit fault at t=0.4 s. Isolation (T_{fia}) and reconfiguration (T_{fra}) triac current (amperes), load currents (amperes) and fault signal are shown

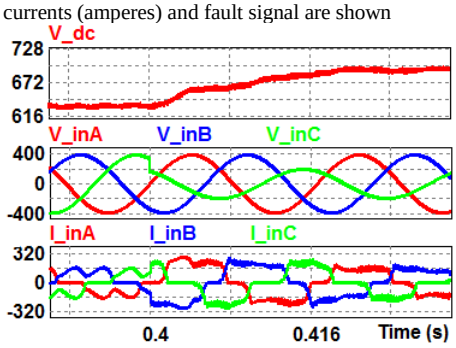

Figure 18. ASC operation with phase to neutral sag of phase C to 50% introduced at t= 0.4 s. DC bus voltage (volts), line voltages (volts), and un-filtered drive input currents (amperes) are shown

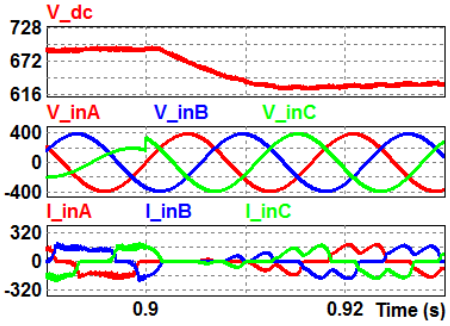

Figure 19. ASC operation with phase C returning to normal operation at t=0.9 s. DC bus voltage (volts), line voltages (volts), and un-filtered drive input currents (amperes) are shown

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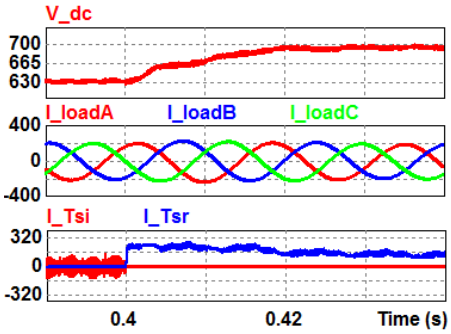

Figure 20. ASC operation with phase to neutral sag of phase C to 50% introduced at t = 0.4 s. DC bus voltage (volts), load currents (amperes), Sag isolation (T_{si}) and reconfiguration (T_{sr}) triac currents (amperes) are shown

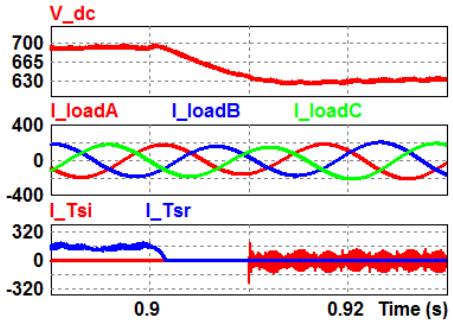

Figure 21. ASC operation with phase C returning to normal operation at t=0.9 s. DC bus voltage (volts), load currents (amperes), Sag isolation (T_{si}) and reconfiguration (T_{sr}) triac currents (amperes) are shown

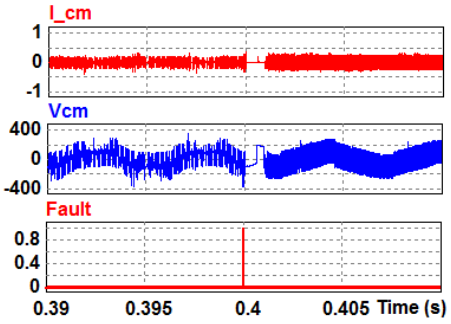

Figure 22. Common mode current (amperes) and voltage (volts) before and after fault

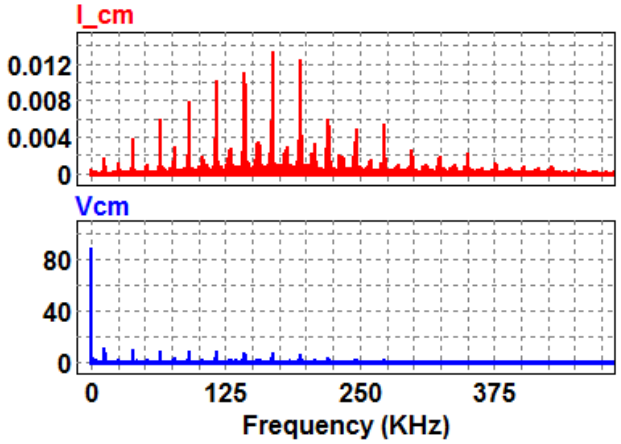

Figure 23. Common mode current (amperes) and voltage (volts) frequency for normal operation

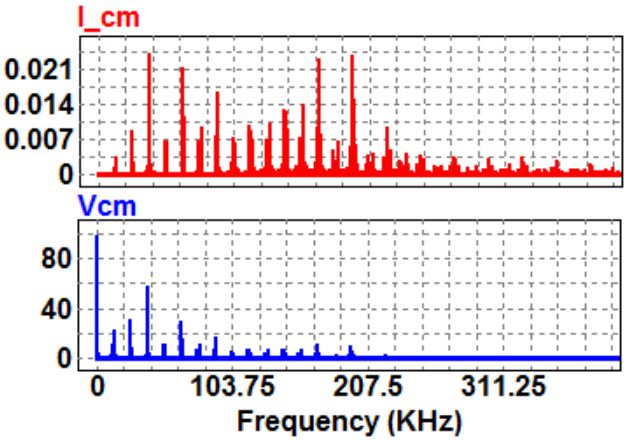

Figure 24. Common mode current (amperes) and voltage (volts) frequency spectrum for post fault operation

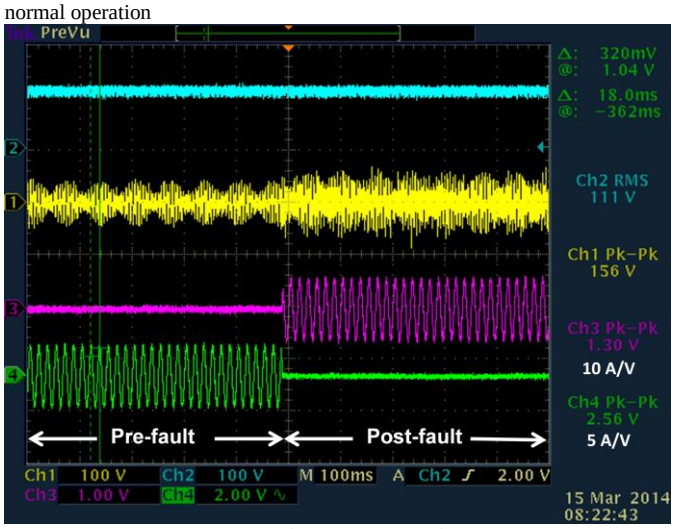

Figure 25. Experimental result for open circuit fault. Ch1: Common mode voltage at load neutral (V_{CM}), Ch2: DC bus voltage ($V_{\_DC}$), Ch3: T_{fra} current ($I_{\_Tfra}$) and Ch4: T_{fia} current ($I_{\_Tfia}$)

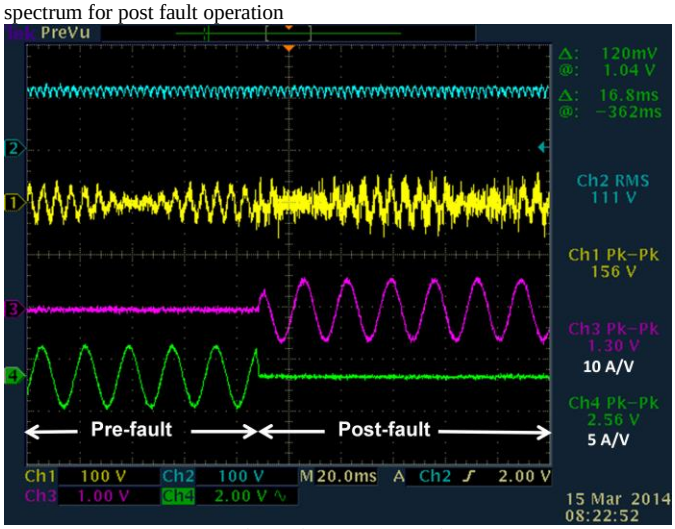

Figure 26. Zoomed in waveforms for open circuit fault, Ch1: Common mode voltage at load neutral (V_{CM}), CH2: DC bus voltage ($V_{\_DC}$), Ch3: T_{fra} current ($I_{\_Tfra}$) and Ch4: T_{fia} current ($I_{\_Tfia}$)

IV. Experimental Results

The experimental results obtained for common mode performance and fault mode operation are discussed in this section. The open circuit fault operation of the proposed topology is verified on a 1 hp rated experimental prototype constructed using Si-IGBT modules, with an R-L load standing in for the electric motor (power factor=0.9). The control is implemented using TI TMS320F28335 microcontroller and ALTERA Cyclone II FPGA. For the implementation, random turn-on solid state relays are used in place of triacs. A description of current and voltage parameters, and device labels can be found in Figure 3.

The open circuit fault is emulated by turning off the gating signal to S_{1A} at an arbitrary moment using an SPST switch on the FPGA board. After a detection time of 2 ms, hardware reconfiguration is activated by the controller, switching off triac T_{fia}.and switching on triac T_{fra} to replace the faulty leg with the healthy auxiliary leg.

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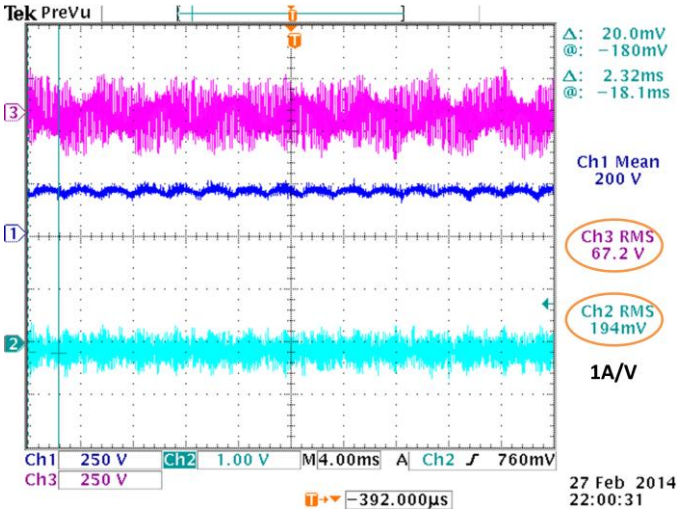

Figure 27. Common mode performance in Sine PWM (3-leg). Ch1: DC bus voltage ($V_{\_DC}$), Ch2: Common mode ground current ($I_{\_CM}$), Ch3: Common mode voltage at load neutral (V_{CM})

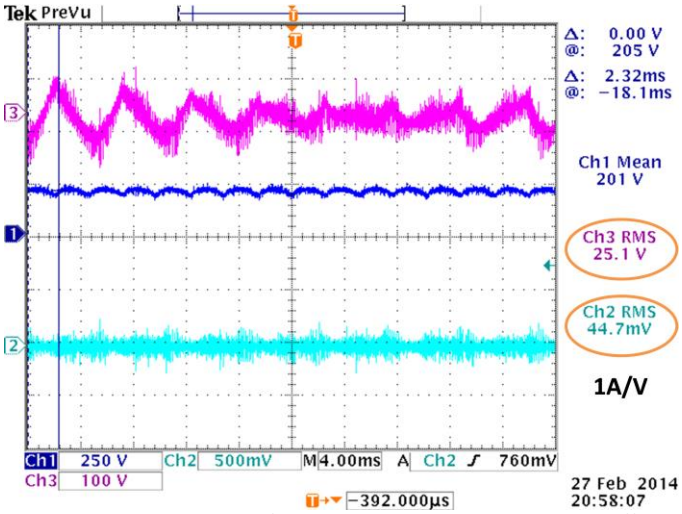

Figure 28. Common mode performance in AZSPWM (4-leg) (scales different from Figure 27). Ch1: DC bus voltage ($V_{\_DC}$), Ch2: Common mode ground current ($I_{\_CM}$), Ch3: Common mode voltage at load neutral (V_{CM})

After a predefined wait period (100 µs), the gating signals for the remaining two un-faulted legs and the auxiliary leg are updated, and the inverter enters fault mode operation. The operation of the system in open circuit fault mode is shown in Figure 25 and Figure 26. In the case of a 100 hp practical system, the handover of output current from isolation traic (T_{fia}) to reconfiguration triac (T_{fra}) is expected to be slower. The waveform for DC bus voltage ($V_{\_DC}$), common mode voltage (V_{CM}), triac T_{fra} current ($I_{\_Tfra}$) and triac T_{fia} current ($I_{\_Tfia}$) are shown.

It can be seen that the load current is transferred from triac T_{fia} (conducting pre-fault) to triac T_{fra} (conducting post fault), which demonstrates completion of the reconfiguration process. The beat frequency observed in the common mode voltage is due to the difference (≈ 5 Hz) in inverter output fundamental frequency and grid frequency. In the pre-fault condition, the system operates in AZSPWM 4-leg with active common mode voltage suppression. In the post-fault operation, the active common mode voltage suppression ability is lost and the system operates in AZSPWM 3-leg. It can be observed that common mode performance degrades in post fault condition, since 3-leg operation increases switching frequency harmonic components in the common mode voltage.

The common mode performances of the AZSPWM modulation strategy (4-leg) and sinusoidal PWM (3-leg) have been verified on the 1 hp rated experimental prototype. A DC bus voltage of 200V is used with a resistive load. A ground coupling capacitor (C_g) of 10 nF is used between load neutral and ground. The load neutral voltage and the ground current through coupling capacitor are shown in Figure 27 and Figure 28 for 3-leg Sine PWM and 4-leg AZPWM operation respectively. As in previous results, the beat frequency observed in the common mode voltage is due to the difference (≈ 5Hz) in inverter fundamental frequency and supply frequency. It can be seen that there is a significant reduction in rms value common mode voltage (~60%) and ground current (~80%) in the AZPWM case. As shown in the analysis section II.D, there is a third harmonic component in common mode voltage and high frequency components have been significantly attenuated.

V. Conclusion

A fault tolerant ASD topology for motor drive system was proposed in this paper to mitigate the effect of common mode voltage, voltage sags and device failures. An auxiliary inverter leg, three auxiliary diodes, and an isolation - reconfiguration circuit were added to a conventional ASD topology. The topology was discussed for three different modes of operation. The isolation and reconfiguration strategy for both voltage sags and device faults were described. Fault mode operation was discussed for both open and short circuit device failures. Once a failure was detected, the auxiliary leg was used to replace the faulted leg. A current shaping control was proposed for the auxiliary sag compensation mode. The common mode voltage performance for the proposed topology was analyzed and it was verified that CMDR performance was superior for 4-leg AZPWM for all modulation indices. Simulation results for a design example rated at 80 kW were presented for different modes of operation. Experimental results on a 1 hp system demonstrate the validity of the proposed auxiliary leg based system. The fault tolerance scheme was verified for open circuit fault. A significant reduction in common mode voltage of up to 60% and up to 80% reduction in ground current were achieved.

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