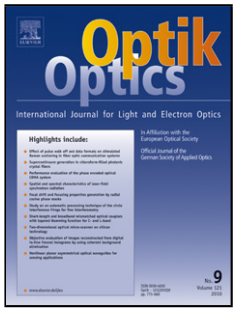

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An optimal design of Full adder based on 5-input majority gate in Coplanar Quantum-dot Cellular Automata

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Abstract

Quantum-dot cellular automata (QCA) is one of the alternative technologies that enable nanoscale circuit design with high performance and low power consumption features. In this aspect, QCA wire crossing is a challenging task in the coplanar QCA fabrication, as defects appear to be inherent due to two cell types in single layout structure. This work showcases an extensive structural and power analysis of previous 5-input majority gates. It has been found that the existing 5-input majority gates are not power efficient and the structures are not well optimized. To overcome this, we have proposed a new low-complexity coplanar 5-input majority gate, which consumes less power compared to prior designs. To evaluate the usefulness of proposed gate a new one bit full adder circuit is presented. The proposed full adder is more robust and enjoys single layer wire crossing, via clock phasing, which requires only one type of cell. The results show that the proposed full adder performs equally well compared to existing multilayer designs and performs better in case of previous coplanar full adder designs in all aspects. Our design achieves 20% improvement in cell count and consumes 7% less area in comparison to the best single layer design. QCADesigner tool is used to validate the layout of the proposed designs and QCAPro power estimator tool is used to evaluate the power dissipation of all considered designs.

Keywords: Quantum-dot cellular automata (QCA). 5-input majority gate. QCADesigner. QCAPro. Full adder.

1 Introduction

With the exponential decrease in feature size in CMOS technology, devices are more prone to high leakage current, high power density and are more sensitive to circuit noise [1]. This encourages researchers to come up with some alternative technologies like quantum-dot cellular automata (QCA), tunneling phase logic (TPL), single electron tunneling (SET), and carbon nanotube (CNT). In this aspect, QCA could be a feasible competitive alternative, which has none of the above problems and promises extremely low power consumption with small dimension and high speed operation [2, 3]. QCA also offers a new horizon in information computation. In QCA, a cell binds two free electron and the logic values ‘0’, ‘1’ depends on position of electrons inside the quantum-dot cell, which are driven by Coulombic interaction. Therefore, unlike the conventional CMOS a change in logic value from 1 to 0 does not yield discharging of the capacitor. Furthermore, the information is transferred as a

result of propagation of polarization between two cells due to the Coulombic interaction of electrons. In other way, there is no flow of current as in conventional CMOS. Hence, power dissipation due to change in logic and propagation does not add up to the total power dissipation [4]. This makes QCA more suitable over CMOS technology.

Different QCA based digital circuits have been investigated in recent years; structures for 5-input majority gate [5-13], designs for a one bit full adder [6,8,10,12,14-29], QCA based memory cells, flip flops [30-34] have also been studied. In most of the work, designs are not robust and vulnerable to fabrication defects due to wire crossing between the QCA components. So, an efficiently design of crossover wires can reduce the overall costs (i.e., both cell count and implementation complexity). Multilayer crossing is not favourable, due to its area overhead and fabrication issues [35]. However, coplanar crossover is achieved by the use of 45^0 rotated QCA cells [36], but end up with problems, such as reduce robustness and high implementation cost [37], due to two types of QCA cells. The idea behind this work is to devise power efficient and robust QCA circuits using single type cell (i.e., 90^0 QCA cells), and analyze the power dissipation of existing and proposed 5-input majority gates. The proposed 5-input majority gate requires a lesser number of cells and draws little power compared to the best reported one in literatures. Further, an optimal single layer one bit full adder is designed by considering proposed gate, which is based on single type cell.

The rest of the paper is organized as follows: Section 2 gives a review on QCA logic, structures, different kind of wire crossing techniques and models for power dissipation. Section 3 provides detailed analysis about existing 5-input majority gates. A new 5-input majority gate and its simulation along with physical proof, and power analysis of prior designs are addressed in section 4. In Section 5, we present a glimpse of available full adder circuits and based on proposed 5-input majority gate, an efficient one bit full adder is proposed. Simulated results of proposed designs and comparison to previous works are inspected in section 6 and finally paper concludes in Section 7.

2 QCA fundamentals

In QCA a single cell is considered to construct each and every element (Computational and wires) of a circuit. Each cell consists of four quantum-dots at the corners and two of them contain free electrons. These electrons can quantum-mechanically tunnel between the four dots. Potential barriers of tunnelling junctions are controlled by local electric fields. This field, siege electron movement or permits electron movement by simply raising or lowering

potential barriers respectively. An isolated cell can settle in one of the three different states. Barrier lowering gives rise to a *null* state, where electrons are free to place at any dots. Remaining two states occur when barriers are raised. The cells in these states maintain a minimum energy. They are represented as P= +1 (logic 1) and P= -1 (logic 0) due to Coulombic interaction between electrons in a quantum cell [3], as shown in Fig. 1(a).

2.1. Basic structures

An inverter and majority voter (MV) gate are the fundamental gates that are used to construct any QCA gates and circuits. Wiring between two logic blocks is done by the cascade of Quantum cells, as shown in Fig. 1(b). Fig. 1(c), (d) depict two different implementations of an inverter [3, 36]. First inverter has more cells than the second inverter, but comes with more functionality. Two different QCA implementations of majority gate are shown in Fig. 1(e). The majority gate function is described by the following equation:

$$MV(A, B, C) = F = AB + BC + CA \quad (1)$$

A majority gate can be modified to a 2-input AND gate or a 2-input OR gate. To realize AND gate or OR gate, one of the input terminals of majority gate is set to P= -1 or P= +1 respectively.

2.2. Clocking

All QCA circuits need proper clocking to control the flow of information, which also provides necessary power to drive the circuit. QCA clocking is based on Landauer clocking. To drive the input to the desired output, signals need to be passed through four clock zones. Clock signals for each zone are distinct and 90^0 phase shifted [38, 39]. This clock zone provides the necessary electric field, which changes the potential barriers. So, clock zones enable the computation in a sequential manner, i.e. when computation is going on in one zone, the previous zone must hold its outputs. This can be achieved by dividing each signal clock into four phases: *Switch, Hold, Release,* and *Relax* [40] as shown in Fig. 2.

Switch phase starts with cell polarization and computation occurs. When the clock reaches highest level, second, i.e. *Hold* phase starts. In this phase cells are completely polarized, which prevents electrons to tunnel through the barrier. Barrier and cell polarization are reduced at the falling edge of the clock, called *Release* phase. The final phase, i.e. *Relax*

phase starts at the low level of the clock. In this phase cell becomes unpolarized and no barrier exists between the dots.

2.3. Crossing

In QCA structures fabrication of interconnection between components needs to be handled efficiently for a better stability. Till now, there are two different types of crossover are available. These are coplanar and multilayer. In multilayer crossover, multiple layers are used as in CMOS circuit design for interconnection between components as depicted in Fig. 3(a). In coplanar crossover strategy, wire crossing is done by two different cells. These cells are orthogonal to each other, so they operate without affecting neighboring cells. The first wire consists of cells of 90^0 orientations and second wire has only 45^0 orientations as shown in Fig. 3(b). The main drawback of this scheme is that any misalignment of cells during fabrication may cause a cross coupling between the two wires. Works have been done to mitigate such effects, and also to increase the robustness of the circuits, but all these end up with large area overhead [41, 42]. Another type of coplanar wire crossing is addressed in S. H. Shin [43]. In this method wire crossing is based on interference of clocking phases as depicted in Fig. 4.

3. A review on QCA based 5-input majority gate

For two decades QCA based logic circuits are limited to 3-input majority gates. Meanwhile, researchers have shown the 5-input majority gate based designs are efficient in terms of area occupied and faster than the traditional ones. All the designs incorporate the same synchronization approach of 3-input majority gate. As of now, various QCA based structures for 5-input majority gate have been addressed [5-13]. The Boolean function representation of the 5-input majority gate can be expressed as Eq. (9).

$$M(A,B,C,D,E) = ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE \quad (9)$$

In the QCA layout of the first structure in [5] shown in Fig. 6(a), the output cell is surrounded by other input cells so, it is impossible to access it in a single layer. Fig. 6(b) presented in [6] suffers from unwanted effect as input cells are close to each other. Structures in [7] and [8] tried to mitigate the above problems as shown in Fig. 6(c) and Fig. 6(d) respectively. Similar works also have been addressed in [9, 10] and corresponding structures are shown in Fig. 6(e), (f) respectively. A single layer accessible and non-symmetrical

structure design is presented in [13] shown in Fig. 6(g), which requires only 11 cells, but not so encouraging as the input cells are close to each other.

4. Proposed 5-input majority gate

4.1. Power dissipation model

Work by Timler & Lent initially developed a power estimation model for QCA based circuit [44]. A Hamiltorian matrix is used to measure energy related to a QCA cell. By considering Hartree–Fock approx imation [45] and mean-field approach Coulombic interaction between QCA cells [44, 46], Hamiltonian matrix for an array of cell is expressed as

$$H = \begin{bmatrix} -\frac{E_k}{2}\sum_i c_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i c_i f_{i,j} \end{bmatrix} = \begin{bmatrix} -\frac{E_k}{2}\left(C_{j-1}+C_{j+1}\right) & -\gamma \\ -\gamma & \frac{E_k}{2}\left(C_{j-1}+C_{j+1}\right) \end{bmatrix} \quad (2)$$

where $f_{i,j}$ is a geometrical factor representing electrostatic interactions between cell i and cell j due to the geometrical distance and polarization of the i^{th} juxtaposed cell is represented by C_i. If the space between neighboring cells are equal, then $f_{i,j}$ is interpreted as the kink energy, which can be calculated using the electrostatic interaction between all electrons in two cells, i and j, as [8]

$$E_{i,j} = \frac{1}{4\pi\varepsilon_0\varepsilon_r}\sum_{n=1}^{4}\sum_{m=1}^{4}\frac{q_{i,n}q_{j,m}}{\left|r_{i,n}-r_{j,m}\right|} \quad (3)$$

At each clock cycle the expectation value of QCA cell energy is expressed as

$$E = \langle H \rangle = \frac{\hbar}{2}\cdot\vec{\Gamma}\cdot\vec{\lambda} \quad (4)$$

where $\hbar$ is the Planck constant, $\vec{\Gamma}$ is the energy environment vector of the cell and Coherence vector is represented as $\vec{\lambda}$. The Hamiltonian vector is presented as

$$\vec{\Gamma} = \frac{1}{\hbar}\left[-2\gamma, 0, E_k(C_{j-1}+C_{j+1})\right] \quad (5)$$

Here $(C_{j-1}+C_{j+1})$ represents the sum of neighboring polarizations. Power flow between neighboring cells is shown in Fig. 5. As mentioned in [44, 47], P_{in} and P_{out} are the inflow signal power and the released signal power for a QCA cell. During the *switch* phase, P_{clock} amount of energy transfer to the cell as inter-dot barriers are raised. Similarly, in *Release*

phase the energy gets returned to the clocking circuit as barriers are reduced. During this process a small power is dissipated in the clocking circuit named as P_{diss} [46, 47]. The total instantaneous power for a cell is given as

$$P_t = \frac{dE}{dt} = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}\cdot\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2 \tag{6}$$

where P_1 combines the difference of input and output signal powers and clocking power to the cell and P_2 is the dissipated power [47]. According to [44], Hamiltonian and Coherence vectors can be used to calculate the energy dissipation in one clock cycle T_{cc} = [-T, T] as

$$E_{diss} = \frac{\hbar}{2}\int_{-T}^{T}\vec{\Gamma}\cdot\frac{d\vec{\lambda}}{dt}dt = \frac{\hbar}{2}\left(\left[\vec{\Gamma}.\vec{\lambda}\right]_{-T}^{T} - \int_{-T}^{T}\vec{\lambda}\cdot\frac{d\vec{\Gamma}}{dt}dt\right) \tag{7}$$

The upper bound power dissipation model in [47] is presented as

$$P_{diss} = \frac{E_{diss}}{T_{cc}} < \frac{\hbar}{2T_{cc}}\vec{\Gamma}_{+}\times\left[-\frac{\vec{\Gamma}_{+}}{\left|\vec{\Gamma}_{+}\right|}\tanh\left(\frac{h\left|\vec{\Gamma}_{+}\right|}{k_B T}\right) + \frac{\vec{\Gamma}_{-}}{\left|\vec{\Gamma}_{-}\right|}\tanh\left(\frac{h\left|\vec{\Gamma}_{-}\right|}{k_B T}\right)\right] \tag{8}$$

Here $\vec{\Gamma}_{+}$, $\vec{\Gamma}_{-}$ represents $\vec{\Gamma}(+T)$ and $\vec{\Gamma}(-T)$ respectively, k_B defines the Boltzmann constant and T is the temperature.

Authors in [48] addressed a power dissipation model by considering above concepts and developed a power estimation tool known as QCAPro. This helps to evaluate the total power loss in a QCA circuit as a combination of leakage and switching power when clock changes.

4.2. Structural Analysis

The proposed structure of majority gate is depicted in Fig. 7(a). It comprises 10 quantum-dot cells, 5 inputs, 1 output and 4 middle cells. It is worth noticing that all the cells are implemented in a single layer, so it is easy to access the cells with no additional layers in the design. Polarization of middle cells and output cell can be changed by fixing polarization of input cells. The proposed symmetric structure allows one of the input cells and output cell to be placed at any of the 4 locations labelled L1, L2, L3 and L4 in 12 different ways. This feature makes the gate more flexible and robust, unlike existing gates. In this design the middle cell 1 is polarized by input cells A and B. In a similar manner, cell 4 is polarized by input cells B and C. Also, cells 2 and 3 get combined effect from their neighbours and input cells D and E. These effects transfer the majority outcome of inputs to the output and results a 5-input majority gate.

Further, all the input and output cells are not trapped by other cells, which overcomes the shortcoming in prior designs. To verify the structure, simulation result has been presented in Fig. 7(b), which achieves expected output with higher polarization. Structural analysis of the proposed gate with all existing gates is noted in Table 1 by considering several parameters like cell counts, output polarization strength, area occupied and coplanar accessibility to input and output cells. Though the designs in [5] and [6] require less area for implementation, yet these designs are not fully single layer accessible. Our proposed gate enjoys full accessibility to input and output cells. In addition, proposed structure shows a significant improvement in terms of complexity and area covered in comparison to other designs [7-13]. A 5-input majority gate can be modified to a 3-input AND gate or a 3-input OR gate. To realize AND gate or OR gate, two of the input terminals of 5-input majority gate are set to P=-1 or P=+1 respectively as shown in Fig. 8(a), (b). Input and output waveforms for the AND and OR gate are depicted in Fig. 9(a), (b).

4.3. Physical proof

For a 5-input majority gate, 32 different input states are required to validate the gate. Out of 32 different input states, we have considered only one state (A=1, B=1, C=1, D=0, E=1) to check the exactness of the gate, due to paucity of space and other states can be similarly verified. Polarization of middle cells and output cell can be changed by fixing polarization of input cells.

Let's consider, all the quantum cells are of equal size (18nm×18nm) and two neighboring cells are separated by 2nm. QCA cells are represented in rectangles and electrons position in a cell is shown as circles in all figures. Electrons in a cell are arranged in such a way that minimizes their potential energy to achieve stability.

The potential energy U between two electron charges is measured using (2), where k is fixed colon, q_1 and q_2 are electric charges and r is the distance between two electric charges. U_T is the summation of potential energies that is calculated from Eq. (11) [49-51]. Two different states for electrons, x and y are considered for cell 1, as shown in Fig. 10(a) and 10(b). The idea behind this is to find a state that exhibits minimal potential energy.

$$U = \frac{kq_1q_2}{r} = \frac{A}{r} = \frac{23.04\times10^{-29}}{r} \tag{10}$$

$$U_T = \sum_{i=1}^{n} U_i \tag{11}$$

Fig. 10(a)(electron x)

$$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{20.09\times10^{-9}} \approx 1.14\times10^{-20}\,\text{J}$$

$$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{20.09\times10^{-9}} \approx 1.14\times10^{-20}\,\text{J}$$

$$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{10.19\times10^{-9}} \approx 2.26\times10^{-20}\,\text{J}$$

$$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{34.40\times10^{-9}} \approx 0.67\times10^{-20}\,\text{J}$$

$$U_{T_{11}} = \sum_{i=1}^{4} U_i = 5.21\times10^{-20}\,\text{J}$$

$$U_{T_1} = \sum_{i=1}^{2} U_{1i} = 7.93\times10^{-20}\,\text{J}$$

Fig. 10(a)(Electron y)

$$U_1 = \frac{A}{r_1} = \frac{23.04\times10^{-29}}{42.94\times10^{-9}} \approx 0.54\times10^{-20}\,\text{J}$$

$$U_2 = \frac{A}{r_2} = \frac{23.04\times10^{-29}}{42.94\times10^{-9}} \approx 0.54\times10^{-20}\,\text{J}$$

$$U_3 = \frac{A}{r_3} = \frac{23.04\times10^{-29}}{21.54\times10^{-9}} \approx 1.06\times10^{-20}\,\text{J}$$

$$U_4 = \frac{A}{r_4} = \frac{23.04\times10^{-29}}{39.29\times10^{-9}} \approx 0.58\times10^{-20}\,\text{J}$$

$$U_{T_{12}} = \sum_{i=1}^{4} U_i = 2.72\times10^{-20}\,\text{J}$$

Fig. 10(b) (electron x)

$$U_{T_{21}} = \sum_{i=1}^{4} U_i = 2.92\times10^{-20}\,\text{J}$$

$$U_{T_2} = \sum_{i=1}^{2} U_{2i} = 8.16\times10^{-20}\,\text{J}$$

Fig. 10(b) (electron y)

$$U_{T_{22}} = \sum_{i=1}^{4} U_i = 5.24\times10^{-20}\,\text{J}$$

For the total potential energy (U_T) of the electrons, x and y with respect to electrons (e1, e2, e3, e4) in both states are calculated using (2) and (3). It is noted that the state in Fig. 10(a) is more stable. Similar analysis is done for rest of the middle cells and potential energies of final output are calculated based on the potential energies of cells (1, 2, 3, 4) as shown below:

cell 2:	cell 3:	cell 4:	Cell out:
$U_{T_1} = 13.9\times10^{-20}\,\text{J}$	$U_{T_1} = 20.08\times10^{-20}\,\text{J}$	$U_{T_1} = 7.95\times10^{-20}\,\text{J}$	$U_{T_1} = 17.67\times10^{-20}\,\text{J}$
$U_{T_2} = 34.39\times10^{-20}\,\text{J}$	$U_{T_2} = 33.88\times10^{-20}\,\text{J}$	$U_{T_2} = 13.75\times10^{-20}\,\text{J}$	$U_{T_2} = 9.46\times10^{-20}\,\text{J}$

For all the cells, U_{T1} represents potential energy in -1 polarization and U_{T2} represents potential energy in +1 polarization. All the measured polarizations are satisfied with the polarization of cells when implemented as depicted in Fig. 10(a).

4.4. Power Analysis

In order to measure the power consumption of the proposed gate and existing ones, QCAPro [48] has been used as a power evaluator tool. For evaluation three different tunneling energies are taken (0.5 E_k, 1.0 E_k, 1.5 E_k) at 2 K temperature. Fig. 11 shows energy dissipation maps of various 5-input majority gates [5-11, 13] with tunneling energy of 0.5 E_k. Cells with higher power dissipation are represented by darker colors in thermal hotspot maps.

A comparative analysis of power consumption is depicted in Table 2, where leakage and switching energies contribute to total energy dissipation.

From Table 2**,** it is noticed that our design achieves lower power dissipation in comparison to all existing coplanar 5-input majority gate structures. For better readability, Fig. 12, 13 and 14 are provided for average leakage energy, average switching energy and total energy dissipation respectively for all considered designs. From Fig. 12, it is apparent that proposed gate is superior over the design [7-10, 13] and designs in [5, 6] achieve least leakage energy. However, proposed gate produces less switching energy as compared with existing design [5-10] for different tunneling energies shown in Fig. 13. Fig. 14 provides an overall comparison of total energy dissipation for all the presented structures. It is worth noticing that the total energy dissipation of the proposed gate is less compared to the best existing design [13] except at tunneling energy of 0.5 E_k This low power and minimum area features facilitate designers to realize ultra-low power and complex QCA circuits.

5 Single Bit QCA Full adder

Full adder is rudimental for most of the digital circuits, having a high speed and less complex full adder is significantly important. In QCA, it is realized using majority gates. Various works have been done in this direction [6,8,10,12,14-29]. Most of the designs are limited to 3-input majority gates except in [6, 8, 12, 16]. In [17], a one bit full adder has been realized using five 3-input majority gates and three inverters. Further, a simplified version of this design is implemented is presented, which comprises of four 3-input majority gates and three inverters. In [18], an optimized configuration for a full adder is presented, which consumes three 3-input majority gates and two inverters. However, a more optimized full adder circuit is achievable using 5-input majority gate, which reduces the cell counts as well as area occupation. In [6], authors have implemented one bit full adder using only four gates (one 3-input majority gate, two inverters in addition to one 5-input majority gate). Similar work has been addressed in [16], which consumes 3 gates (one 3-input majority gate, one inverter in addition to one 5-input majority gate). In [6,8,12,16-20,23,25,26,28,29], authors tried to implement full adder using multilayer, but multilayer crossover may not be easy from the fabrication perspective [52] and hard to implement.

5.1. Proposed QCA one bit Full adder

Design of one bit full adder, even larger bits and incorporating with signal distribution network (SDN) is a challenging task. For such systems, the complexity increases in terms of number of wires crossing, so more prone to defects that occurs due to QCA fabrication of single layer crossing using two different cells (90^0 and 45^0) in a single layout. In this work, an optimal single layer QCA based full adder is designed and implemented using proposed 5-input majority gate, which incorporates the robust single layer crossing method using single cell (90^0). Schematic of one bit full adder is depicted in Fig. 15. For implementation, it requires only 49 cells and spreads over an area of 0.04 μm^2. It consumes four clock phases to produce valid carry output and sum. The layout of the proposed full adder is shown in Fig. 16(a), which utilizes a coplanar 3-input and 5-input majority gate. The QCADesigner based simulation result for the proposed adder is shown in Fig. 16(b). This indicates the correct operation of proposed structure and a valid output after 1 clock cycle.

6 Simulation Results

All the proposed circuits are simulated using the simulator QCADesigner-2.0.3 [53]. Simulation engine is set to coherence vector type in QCADesigner tool using the parameters as shown in Table 4.

A comparison between proposed full adder and all existing full adder designs is illustrated in Table 3 over different performance parameters. It can be inferred from Table 3, that the proposed full adder performs equally well in delay, area occupation and the complexity as compared to the best multilayer design [12]. It is worth noticing that the cell count and area of proposed full adder is also superior to all previous coplanar designs [10,14,15,18,21,22,27], while its delay is less than that of any existing coplanar designs. Our design gains 20% improvement in cell count and consumes same area in comparison to the best single layer design [27].

In addition, we have also studied the effect of temperature variation on the output polarization of the proposed 5-input majority gate and the full adder. The simulations have been done with various temperature values starting from 1 K, and then maximum and minimum polarizations for the output cell have been noted down. Plot of output polarization versus temperature for the 5-input majority gate and the full adder are shown in Fig. 17 and

Fig. 18 respectively. From the plots, it can be concluded that the output polarization remains positive for a wide range of temperature, hence provides robust designs.

7. Conclusion

In this work, an efficient 5-input majority gate has been proposed with physical proof. To support this, a detailed analysis of structures and power issues of all prior ones and proposed 5-input majority gate was performed. To investigate leakage power and switching power dissipation, QCAPro, a power estimation tool was used and all designs are realized and evaluated using QCADesigner 2.0.3 tool. To showcase the efficacy of the proposed majority gate, a new one bit full adder structure was introduced, which inculcates coplanar non-crossover wires, via clock phasing. It is observed that these coplanar structures are robust for considerable variation in temperature and yield more compact digital circuits with respect to existing designs. The results confirmed that the presented structures have outperformed all prior designs and shows significant improvements in terms of power consumption, complexity, area occupation and input to output clock delay. Proposed optimal structures can lead to designing of more complex and high performance QCA nanoscale circuits in the future.

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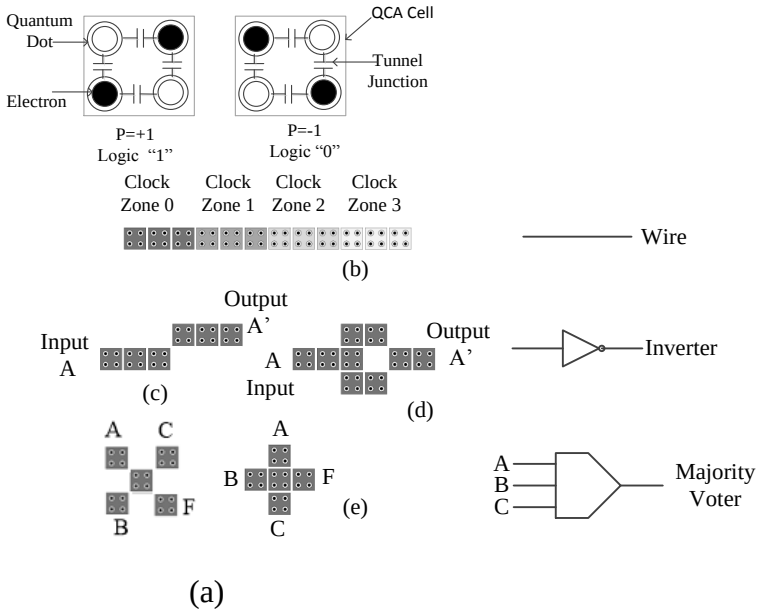


Fig. 1. QCA (a) Two different polarization of Quantum-dot cell (b) QCA wire (c), (d) Two different realization of inverter (e) Majority gate

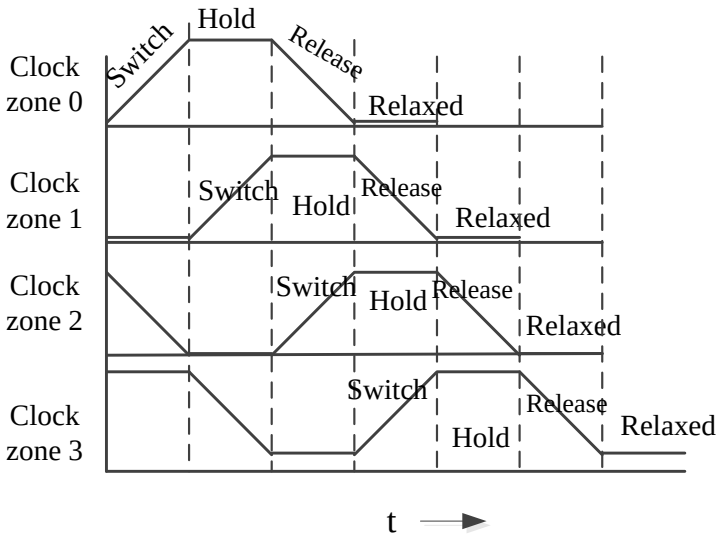
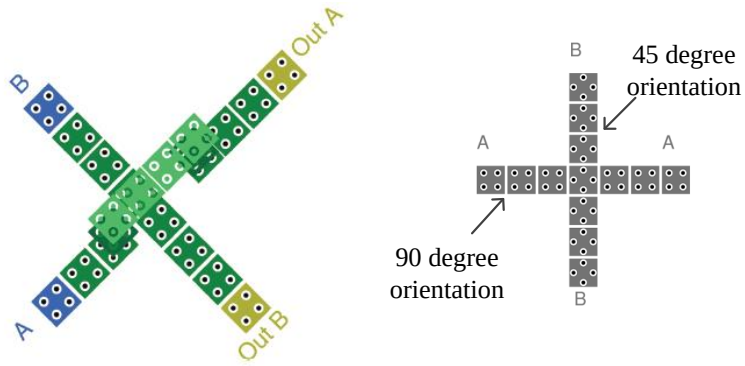


Fig. 2. QCA clocking with four phases



(a) (b)

Fig. 3. Wire crossing (a) Multilayer (b) Coplanar

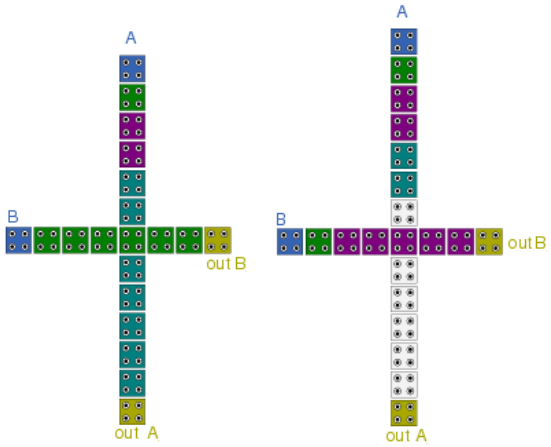


Fig. 4. Wire crossing using single cell cells

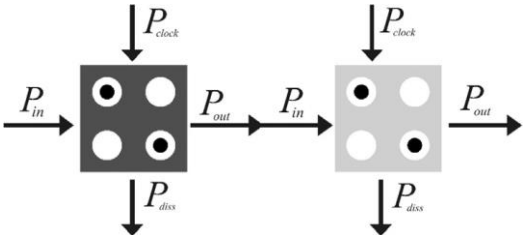


Fig. 5. Power flows between two QCA

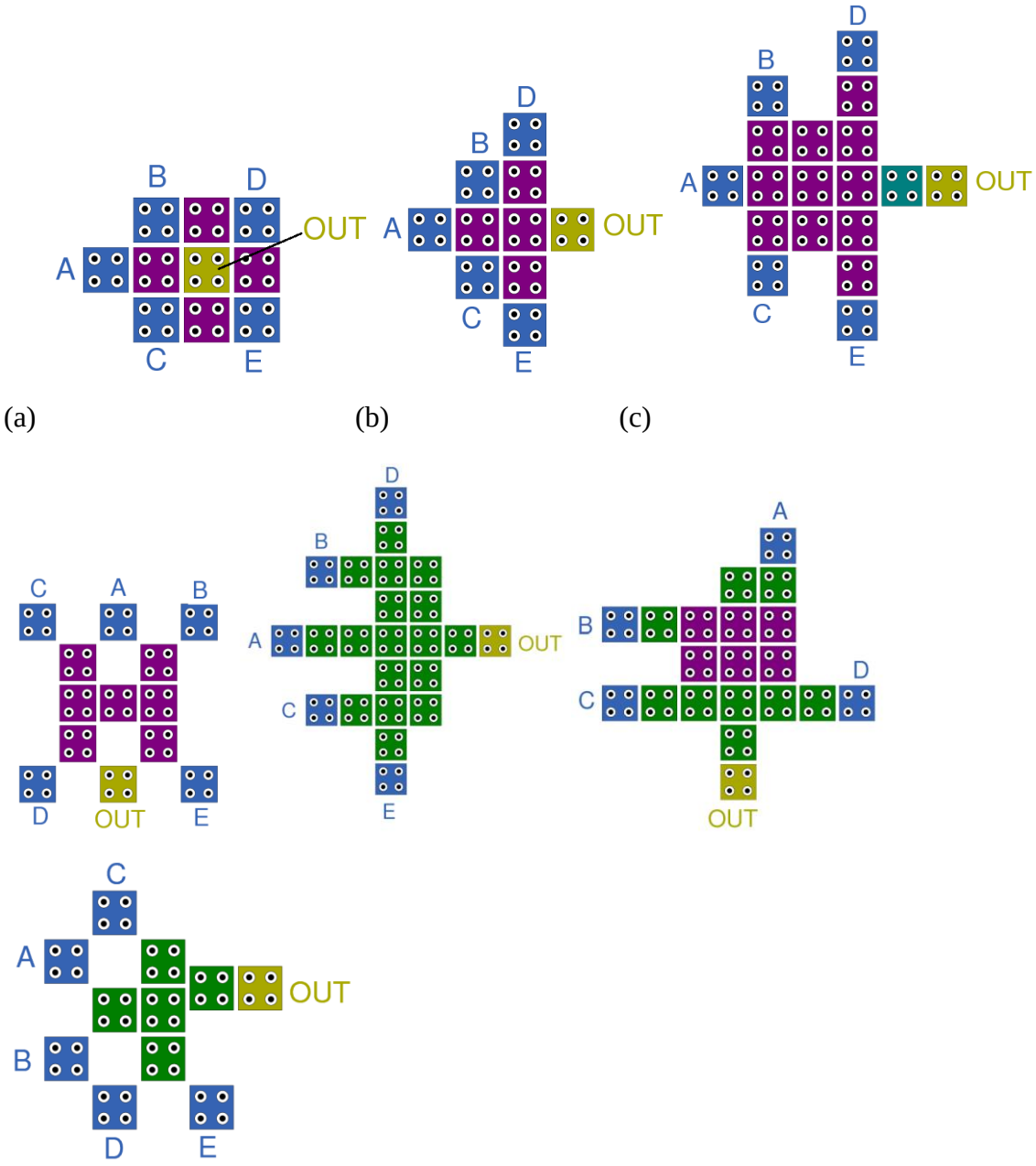
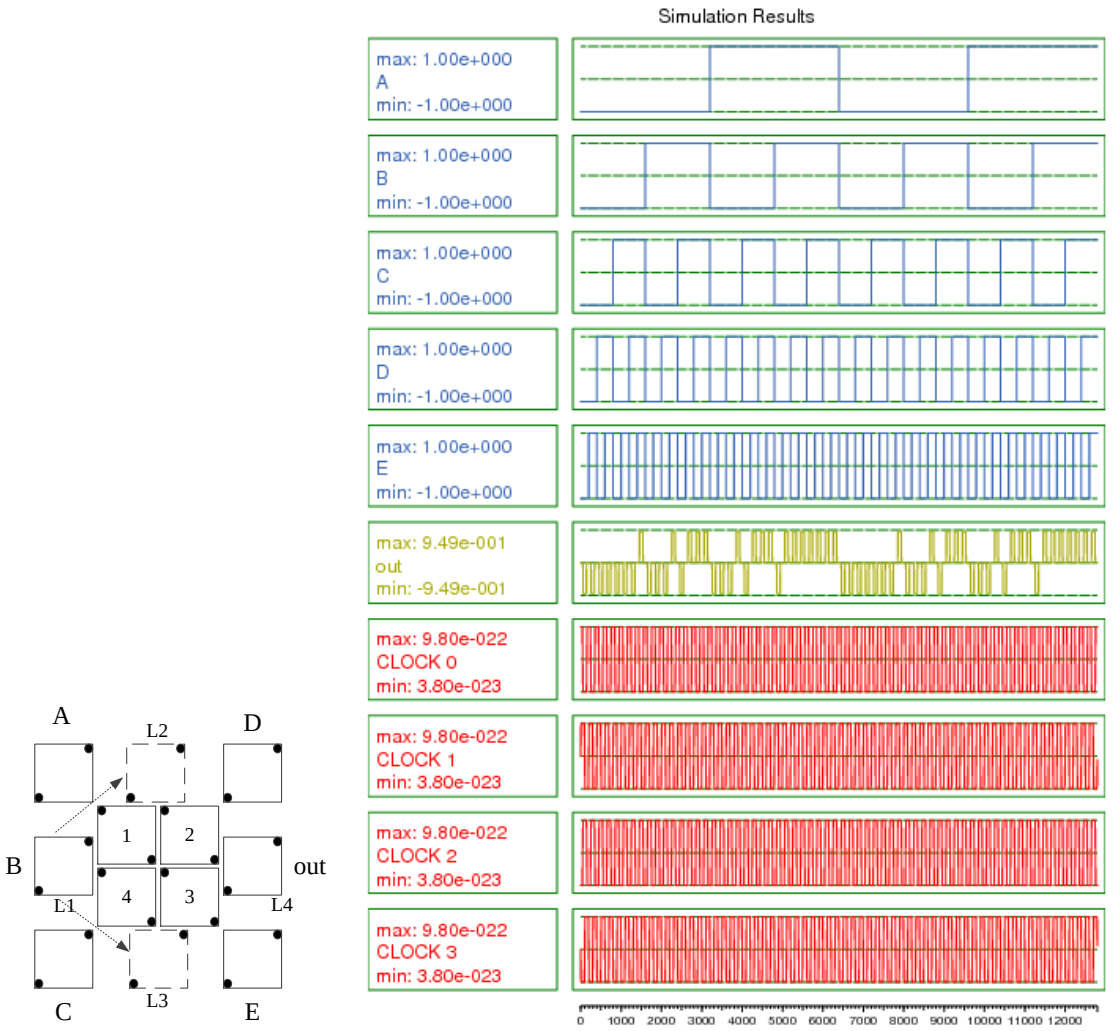


Fig. 6. Five-input majority gate (a) design in [5] (b) design in [6] (c) design in [7] (d) design in [8] (e) design in [9] (f) design in [10] (g) design in [13]

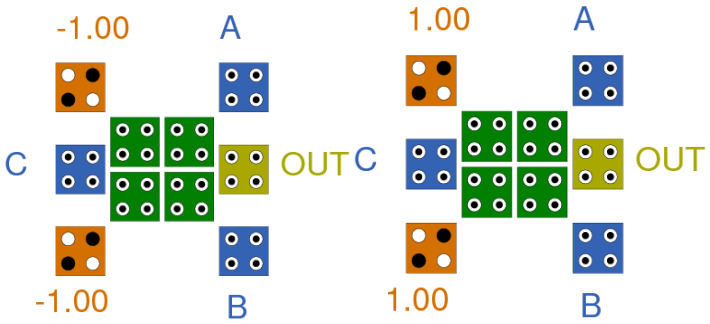


(a) (b)

Fig. 7. 5-input majority gate

(a) Proposed gate symmetric structure

(b) Simulation result for proposed majority gate

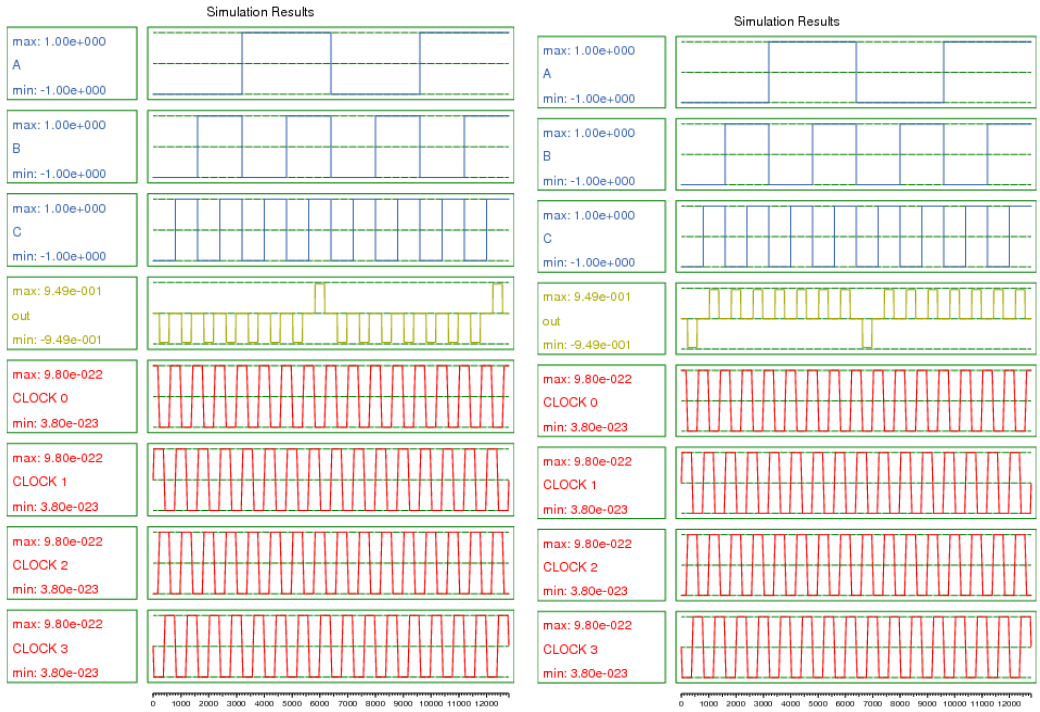


(a) (b)

Fig. 8. Primitive gates layout

(a) 3-input AND gate layout

(b) 3-input OR gate layout

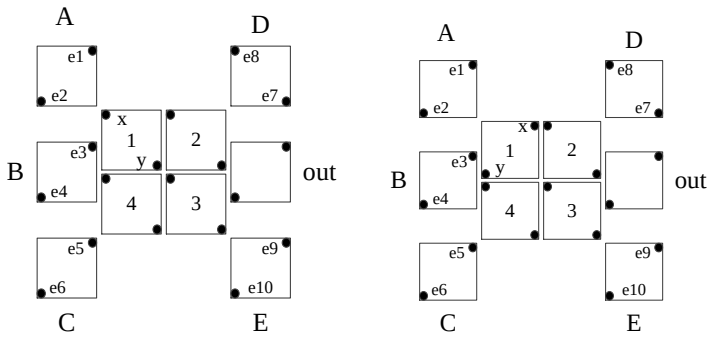


(a) (b)

Fig. 9. Primitive gates simulation

(a) Simulation result for AND gate

(b) Simulation result for OR gate

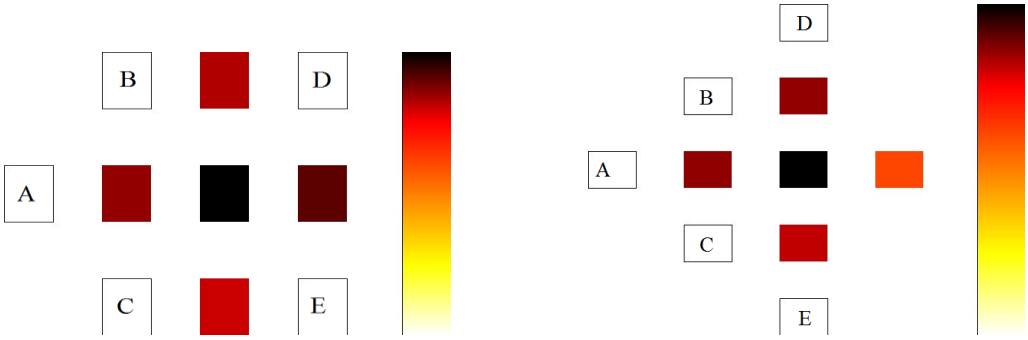


(a) (b)

Fig. 10. Two state of cell 1

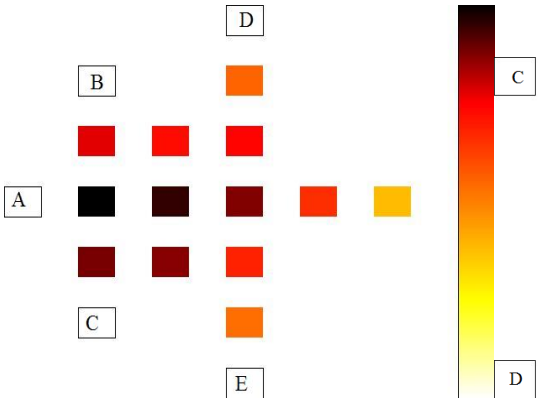
(a) Cell 1 with value ‘0’

(b) Cell 1 with value ‘1’

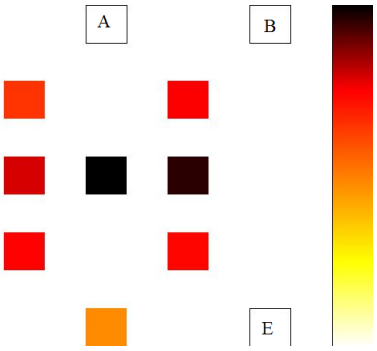


(a)

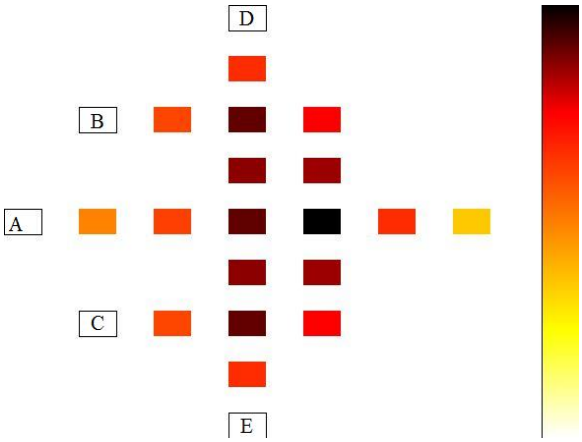
(b)



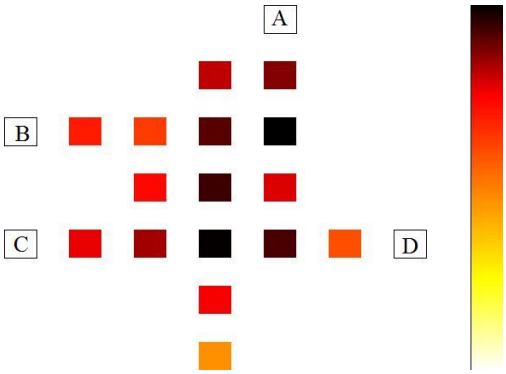
(c)



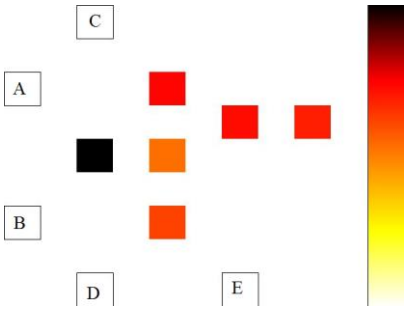
(d)



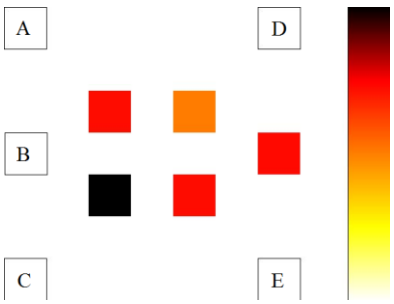
(e)



(f)



(g)



(h)

Fig. 11. Power dissipation maps for 5-input majority gates at 2 K temperature and tunneling energy of 0.5 E_k (a) design in [5] (b) design in [6] (c) design in [7] (d) design in [8] (e) design in [9] (f) design in [10] (g) design in [13] (h) proposed circuit.

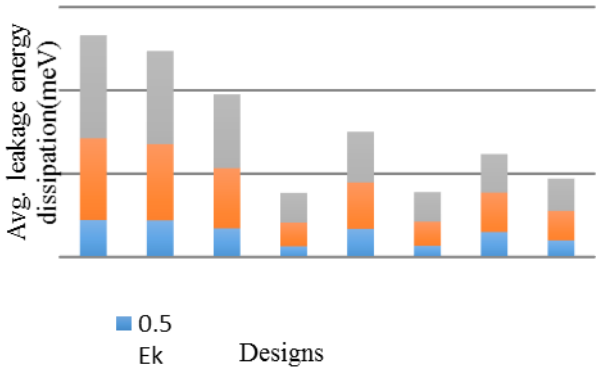


Fig. 12. The average leakage energy dissipation of the existing and proposed 5-input majority gates at different tunneling energy levels (T=2.0 K)

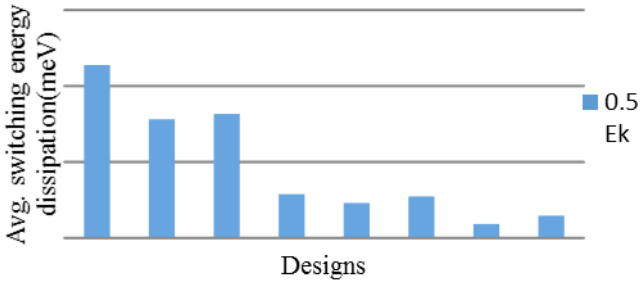


Fig. 13. The average switching energy dissipation of the existing and proposed 5-input majority gates at different tunneling energy levels (T=2.0 K)

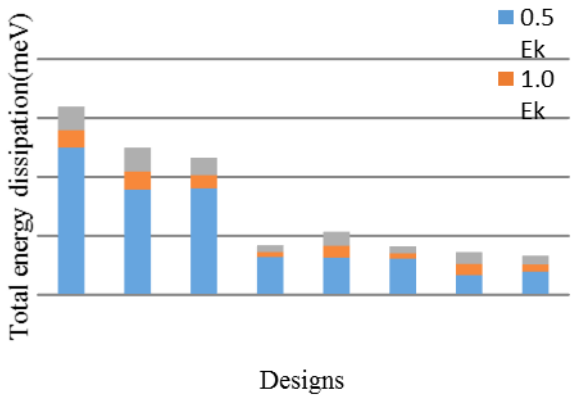


Fig. 14. Total energy dissipation of the existing and proposed 5-input majority gates at different tunneling energy levels (T=2.0 K)

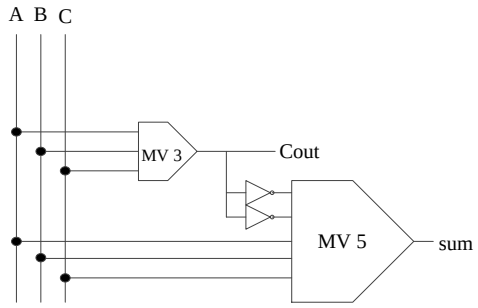
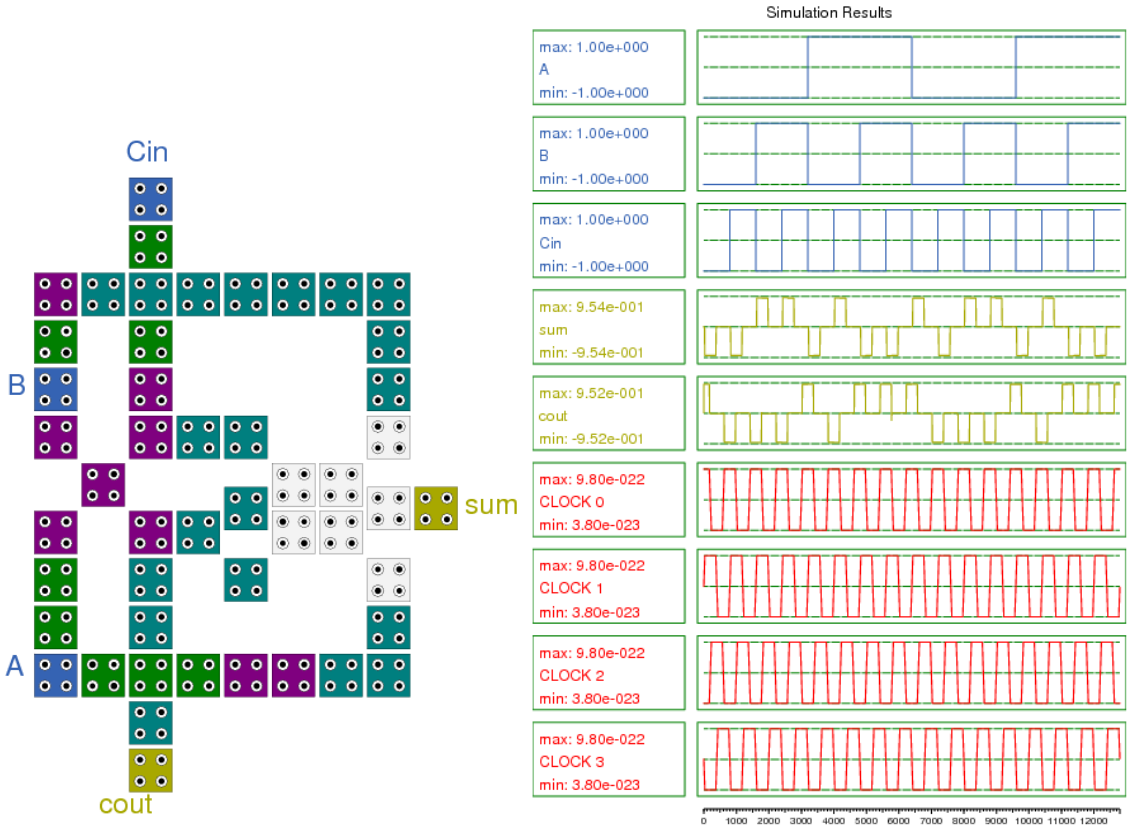


Fig. 15. Schematic of QCA based full adder [6]



(a) (b)

Fig. 16. Proposed full-adder

(a) Layout of proposed full-adder

(b) Simulation of proposed full-adder

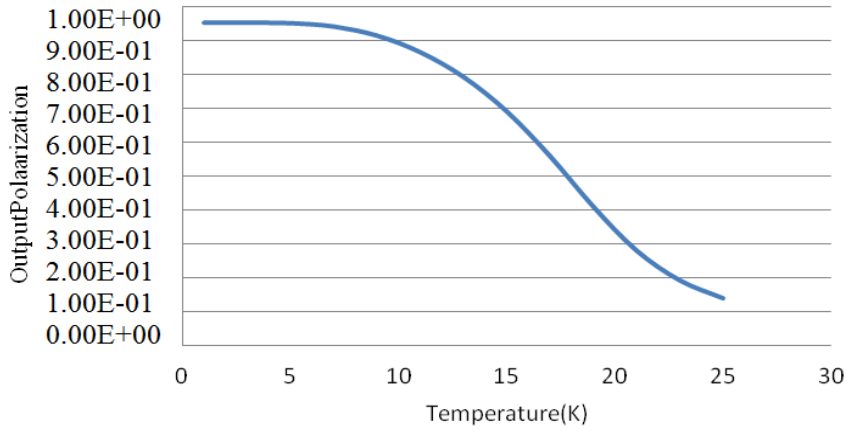


Fig. 17. Polarization versus Temperature for proposed majority gate

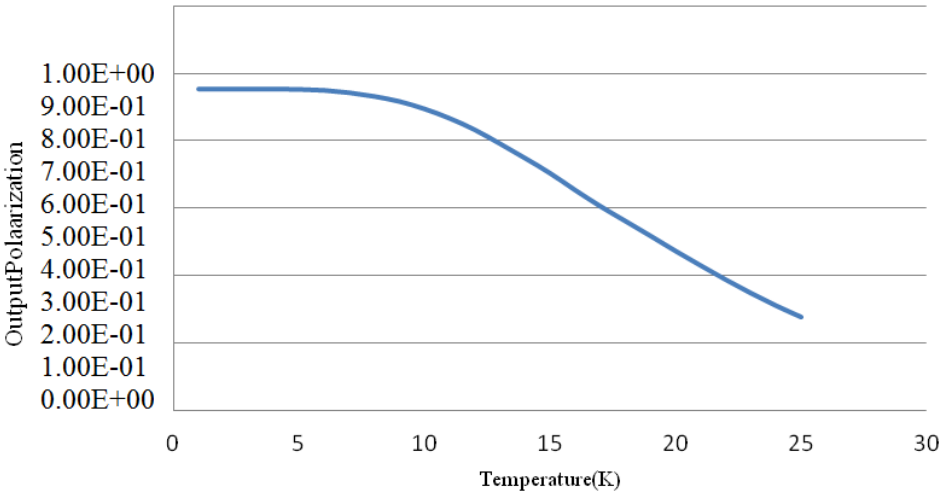


Fig. 18. Polarization versus Temperature for full adder (sum bit)

Table 1 Structural analysis of 5-input majority gates

5-input Majority gate structures	No. of cells	Polarization (e^{-001})	Area occupied(nm^2)	Single layer accessibility to the input and output cells
S. Angizi et al. [9]	23	9.52	24564	Yes
S. Hashemi et al. [10]	20	-	19044	Yes
R. Akeela et al. [8]	18	9.53	16284	Yes
S. Hashemi et al. [12]	18	9.5	16284	Yes
	17	9.5	18644	Yes
A. Roohi et al. [8]	13	8.24	9604	Yes
B. Sen et al. [11]	13	9.54	9604	No
S. Sheikhfaal et al.[13]	11	9.48	9604	Yes
K. Navi et al. [5]	10	9.96	4524	Output cell is surrounded by the other cells, No Single layer accessibility to the output cell, needs multilayer layout
K. Navi et al. [6]	10	9.5	7644	No
Proposed	11	9.49	9604	Yes

Table 2 Power Consumption comparative analysis

Designs	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)			Total energy dissipation (meV)		
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
Previous design [9]	4.44	14.25	26.61	45.51	41.59	37.29	49.96	55.84	63.90
Previous design [10]	4.41	13.55	24.73	31.24	28.31	25.21	35.66	41.85	49.94
Previous design [7]	3.44	10.67	19.52	32.66	29.89	27.01	36.1	40.56	46.53
Previous design [6]	1.28	4.14	7.69	11.53	10.37	9.16	12.81	14.51	16.85
Previous design [8]	3.38	8.95	15.03	9.23	7.7	6.41	12.61	16.65	21.44
Previous design [5]	1.35	4.25	7.8	10.94	9.84	8.7	12.29	14.09	16.5
Previous design [13]	2.99	7.73	12.35	3.69	2.77	2.15	6.68	10.5	14.5
Proposed design (Fig. 14(h))	2.00	5.53	9.41	5.9	4.80	3.90	7.90	10.34	13.31

Table 3 Comparison of full adders on QCA

Full adder	No. of cells	Area(μm2)	Delay(clock cycles)	Layer Type
[16]	>107*2	>.9*2	NA	Multilayer
[17]	192	0.20	NA	-
[19]	135	0.14	1.25	Multilayer
[25]	105	0.14	0.75	Multilayer
[29]	95	0.087	2	Multilayer
[20]	93	0.087	1	Multilayer
[24]	82	0.09	0.75	Multilayer
[12] Design 2	79	0.05	1.25	Multilayer
[26]	79	0.064	1	Multilayer
[23]	73	0.080	0.75	Multilayer
[6]	73	0.04	0.75	Multilayer
[28]	61	0.03	0.75	Multilayer
[8]	52	0.04	0.75	Multilayer
[12] Design 1	51	0.03	0.75	Multilayer
[14]	292	0.62	3.5	Coplanar
[15]	220	0.36	3	Coplanar
[18]	145	0.16	1	Coplanar
[21]	105	0.17	1	Coplanar
[22]	102	0.097	2	Coplanar
[10]	71	0.06	1.5	Coplanar
[27]	59	0.043	1	Coplanar
Proposed design	49	0.04	1	coplanar(single cell, 90^0)

Table 4 QCADesigner parameters for Coherence vector engine

Parameter			Value
Cell size			18 *18 nm^2
Relaxation time			1.000000e-015s
Time step			1.000000e-016s
Radius of effect			80 nm
Relative permittivity			12.9
Clock high			9.8e−22J
Clock low			3.8e−23J
Clock amplitude factor			2.000
Layer separation			11.5000 nm
Clock shift			0.000000e+000
Time step			1.000000e-016s
Total simulation time			7.000000e-011s