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A Novel Robust QCA Full-adder

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Abstract

Quantum-Dot Cellular Automata (QCA) as a candidate technology to replace CMOS promises extra low-power, extremely dense and high speed structures at a nano scale. This paper presents a novel robust QCA full-adder based on an efficient five-input majority gate. This design in contrast to its counterparts uses a robust crossover scheme and surpasses the best previous robust designs in terms of area, delay and complexity. Regarding the efficient layout of this component, it is used to design Ripple Carry Adders with different sizes. The simulations of the proposed designs were done using the both coherence and bi-stable simulation engines of QCA designer version 2.0.3 and same results were achieved which indicate the efficiency and robustness of the proposed designs.

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Keywords: Quantum-Dot Cellular Automata (QCA); Full-Adder; Ripple Carry Adder; Robustness; Coplanar Crossover Scheme.

1. Introduction

The Quantum-dot Cellular Automata (QCA) as a novel nanotechnology, Kummamuru et al. (2003), Orlov et al. (2003), Timler and Lent (2003) has attracted research's attentions Akeela and Wagh (2011), Hänninen and Takala (2010), Kim et al. (2007), Tougaw and Khatun (2013). The structure of a 90^0 QCA cell can be seen in Fig. 1a. As shown in this figure, it contains four quantum dots and two electrons that can move within the cell and occupy two corners diagonally. Fig. 1b demonstrates the QCA layout of a robust three-input majority gate. In this layout, the QCA clocking rule for realizing a robust QCA circuit against sneak noise paths, Hänninen and Takala (2010), Kim et al. (2005), Kim et al. (2007), has been considered (as shown in Fig. 1b, in a robust three-input majority gate, three

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clocking zones with a 90^0 phase delay are used to produce output). According to Rahimi et al. (2007), different types of majority gates such as a five-input majority gate can be used to design QCA circuits .Some of the presented layouts for a five-input majority gate can be seen in Akeela and Wagh (2011), Hashemi et al. (2012) and Navi et al. (2010).

Two types of crossover schemes have been introduced to design QCA circuits: the multi-layer and coplanar crossover schemes, Bhanja et al. (2007), Devadoss et al. (2009), Hashemi and Navi (2014), Shin et al. (2013), Tougaw and Lent (1994), Tougaw and Khatun (2013). Since the required technology for implementing a multi-layer QCA circuit has not yet been introduced, Hänninen and Takala (2010) the coplanar crossover scheme is used to design one-layer QCA circuits. The first coplanar crossover scheme can be seen in Fig. 1c, Tougaw and Lent (1994). It uses 90^0 and 45^0 QCA cells and needs a high precision for QCA cell placement, Devadoss et al. (2009), Hänninen and Takala (2010). Fig. 1d demonstrates the QCA layout of the proposed robust coplanar crossover scheme in Hashemi and Navi (2014). As shown in this figure, it uses only 90^0 QCA cells and works based on a proper clock assignment (it uses two clocking zones with a 180^0 phase delay at the crossing point). Also, this scheme in contrast to its best counterpart, Shin et al. (2013) uses additional clocking zones at the vertical and horizontal wires. Using this mechanism, the input signals are transmitted without any impact on each other (as shown in Fig. 2d, the two outputs a and b are transmitted using QCA cells which are in clocking zone 1 and 3 respectively).

To date, different structures, Pudi and Sridharan (2012), Rahimi et al. (2007), Tougaw and Lent (1994), Wang et al. (2003) and layouts (e.g. the QCA full-adder layouts presented in Abedi et al. (2015), Angizi et al. (2014), Hänninen and Takala (2010), Hashemi et al. (2012), Kim et al. (2007), Pudi and Sridharan (2012)) for a QCA full-adder have been introduced. This paper, presents a novel robust one-layer full-adder layout using an efficient five-input majority gate and the robust crossover scheme in Hashemi and Navi (2014). Based on comparison results, it has an efficient structure and surpasses its best counterparts in terms of area, delay and complexity. The proposed layout also is used to design Ripple Carry Adders with different sizes.

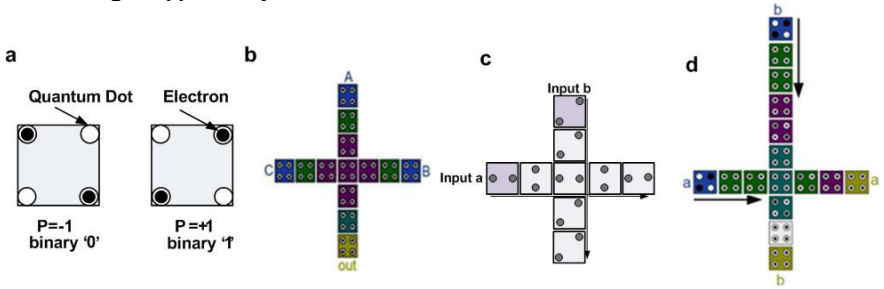

Fig. 1. (a) A 90^0 QCA cell with its binary encoding; (b) A robust QCA three-input majority gate, Hänninen and Takala (2010), Kim et al. (2005), Kim et al. (2007); (c) The coplanar crossover scheme in Tougaw and Lent (1994); (d) The proposed robust crossover scheme in Hashemi and Navi (2014).

2. A New Robust QCA Full-Adder

In this section, based on the presented design in Rahimi et al. (2007), a robust QCA full-adder constructed using three and five input majority gates is introduced. Fig. 2a demonstrates the structure of this design. As shown in this figure, the carry is produced by Maj1 and its inversion is used as the two inputs of the five-input majority gate to produce sum value. The QCA layout of the five-input majority gate can be seen in Fig. 2b. According to this layout, it has an efficient QCA cell arrangement and uses three clocking zones with a 90^0 phase delay to produce output: The QCA cells which transmit the input signals (the input signals *b*, *c*, *d* and the two inversions of the input signal *a*) are in clocking zone0 while the six QCA cells which produce the result are in clocking zone1 and finally the result is transmitted using QCA cells which are positioned in clocking zone2). Based on this layout, the output can easily be used as the input of other QCA circuits.

Figure 2c demonstrates the QCA layout of the proposed full-adder. Based on this figure, it uses the robust coplanar crossover scheme, Hashemi and Navi (2014) to crossover wires (the crossing points are presented as 1 and 2). Also, it is clear that this layout uses the QCA clocking rule in Hänninen and Takala (2010), Kim et al. (2005) and

Kim et al. (2007) to realize a robust three-input majority gate and avoiding sneak noise paths in designing larger QCA circuits (Based on Fig. 2c, the three-input majority gate uses three QCA clocking zones with a 90^0 phase delay to produce output).

Since the proposed full-adder uses the robust coplanar crossover scheme and is robust against sneak noise paths, it is a suitable component for designing larger QCA circuits. In this paper, it is used to design Ripple Carry Adders (RCAs) with different sizes (i.e. 4, 8 and 16 bit RCAs). Fig. 3a, illustrates the QCA layout of the 4-bit Ripple Carry Adder. As shown in this figure, the carry value produced by a QCA full-adder is used as the carry-input value of the next one. Also, based on this layout, it is clear that additional clocking zones are used to synchronize the input (*A0-A3*, *B0-B3*) and output (*S0-S3*, *Carry*) signals.

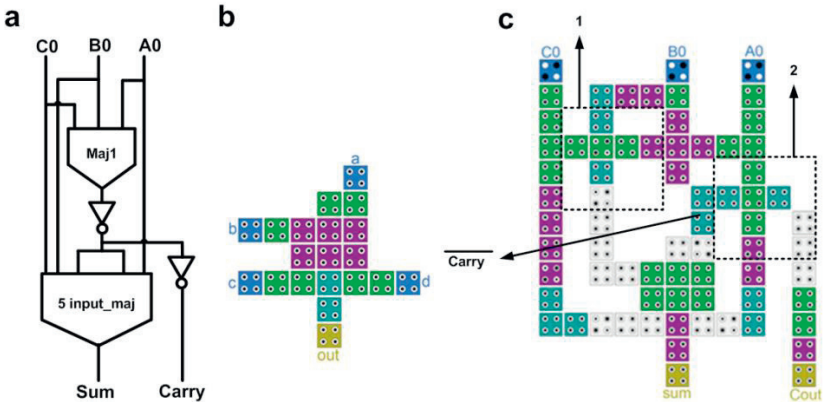

Fig. 2. (a) The schematic of the full-adder based on the presented structure in Rahimi et al. (2007); (b) The QCA layout of the proposed five-input majority gate; (c) The QCA layout of the robust one layer full-adder.

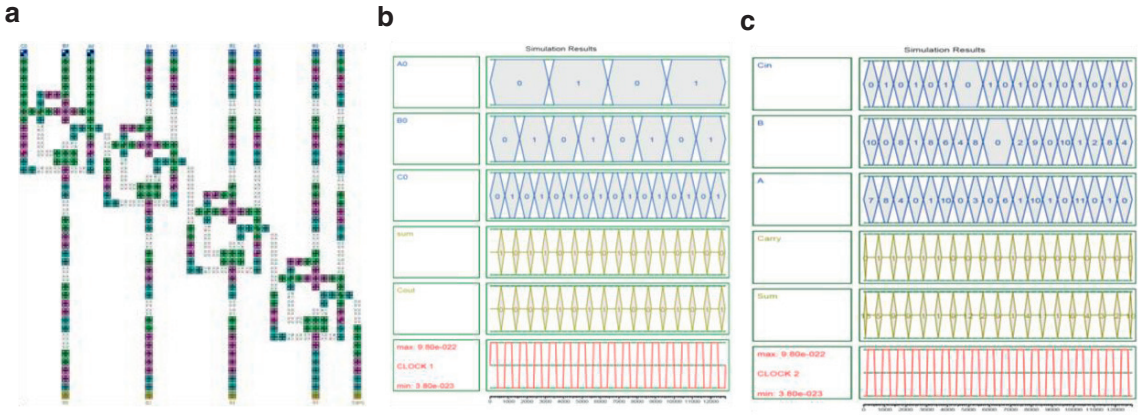

Fig. 3. (a) The QCA layout of the 4 bit Ripple Carry Adder constructed using the proposed robust QCA full-adder in Fig. 2c; (b) The simulation results of the proposed QCA full-adder in Fig. 2c; (c) The simulation results of the proposed 4 bit RCA.

3. Simulation and Comparison Results

In this paper, simulations (as shown in Fig. 3b and 3c) were done using the default parameters of the both engines of QCAdesigner (bi-stable and coherence-vector simulation engines) version 2.0.3 and same results were achieved which indicate the correctness of the proposed designs (based on Fig. 2c and Fig. 3a, the simulation results of the

QCA full-adder and the 4 bit RCA are valid after the second and fifth falling edge of clock 1 and 2 respectively). Table 1 demonstrates the basic structure and crossover scheme of the QCA full-adder layouts in Abedi et al. (2015), Angizi et al. (2014), Hänninen and Takala (2010), Kim et al. (2007), Pudi and Sridharan (2012). As shown in this table, the presented layout in Kim et al. (2007) is based on the full-adder structure in Wang et al. (2003) which is composed of three three-input majority gates and two inverters. Also, this layout uses the coplanar crossover scheme in Tougaw and Lent (1994) to crossover wires. It is worth mentioning that the full-adder layouts in Kim et al. (2007), Hänninen and Takala (2010) use the QCA clocking rules in Hänninen and Takala (2010), Kim et al. (2005), Kim et al. (2007) to achieve a robust structure against sneak noise paths.

As shown in Table 1, some of the previous layouts have been redesigned using the robust crossover scheme in Hashemi and Navi (2014). Based on this table, the QCA layout in Pudi and Sridharan (2012) uses a multi-layer crossover scheme. However, regarding the suitable structure of this full-adder, it has been redesigned using the coplanar crossover scheme in Hashemi and Navi (2014) (as shown in Fig. 4a) and is compared with the proposed layout. The redesigned layouts of Angizi et al. (2014) and Abedi et al. (2015) can be seen in Fig. 4b and 4c. This is done due the vulnerability of their crossover scheme, Shin et al. (2013) against sneak noise paths, Hashemi and Navi (2014). Based on Fig. 4, it is clear that in the redesigned layouts, the QCA clocking rule for constructing a robust three-input majority gate has been considered (the area, delay and complexity of these new layouts can be seen in Table 1).

Comparison results between the proposed full-adder and the best robust one-layer layout (Fig. 4a) in terms of area, delay and complexity indicate that the new full-adder (Fig. 2c) in comparison to this design, leads to around 24, 33 and 37.5 percent improvements in terms of complexity, area and delay. Based on these results, the new layout can be used as a suitable component for designing larger robust QCA circuits. The area, delay and complexity of Ripple Carry Adders with different sizes can be seen in Table 2.

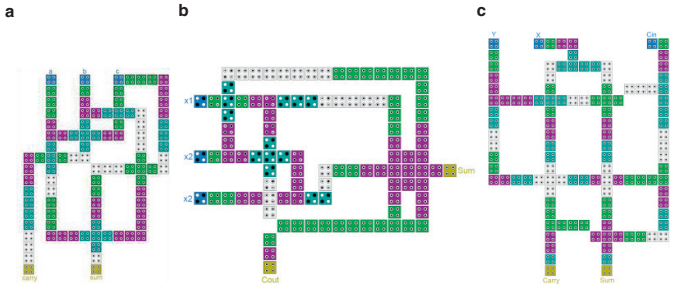

Fig.4. (a), (b) and (c). The redesigned full-adder layouts of Pudi and Sridharan (2012), Angizi et al. (2014), Abedi et al. (2015).

Table 1. The comparison results between the proposed full-adder and its best counterparts.

QCA full-adder layout	Basic Full-adder Structure	Type of majority gates	Type of crossover scheme	Redesign layouts	Complexity (number of QCA cells)	Area ($\mu m^{\wedge 2}$)	Delay (clock cycle)
Kim et al. (2007)	Wang et al. (2003)	Three-input	Tougaw and Lent (1994)	---	220	0.36	3
Hänninen and Takala (2010)	Wang et al. (2003)	Three-input	Tougaw and Lent (1994)	---	101	0.1	2
Pudi and Sridharan (2012)	Pudi and Sridharan (2012)	Three-input	Multi-layer	Fig.4 (a)	94	0.09	2
Angizi et al. (2014)	Rahimi et al. (2007)	Three and five input	Shin et al. (2013)	Fig.4 (b)	103	0.11	1.5
Abedi et al. (2015)	Wang et al. (2003)	Three-input	Shin et al. (2013)	Fig.4 (c)	111	0.13	2.75
The new QCA layout proposed in Fig. 2 (c)	Rahimi et al. (2007)	Three and five input	Hashemi and Navi (2014)	---	71	0.06	1.25

Table 2. The area, delay and complexity of the proposed RCAs with different sizes

	Size	Complexity (number of QCA cells)	Area (μm^2)	Delay (clock cycle)
Ripple Carry Adders (RCAs) constructed using the proposed full-adder in Fig.2 (c)	4	442	1	2
	8	1254	3	4
	16	4030	5	6

4. Conclusion

Designing a robust and one layer QCA full-adder is of great importance to design arithmetic circuits. In this paper a robust QCA full-adder was introduced. This design uses an efficient five-input majority gate and a robust coplanar crossover scheme. Comparison results demonstrate that this layout surpasses its best counterparts in terms of area, delay and complexity and can be a suitable component for realizing robust QCA circuits. Regarding the efficiency of the proposed layout, it was used to design Ripple Carry Adders with different sizes**.**

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