Design of non-restoring binary array divider in majority logic-based QCA

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A novel quantum-dot cellular automata (QCA) design for the non-restoring binary array divider is presented, which is constructed using the proposed coplanar QCA Exclusive-OR gate and full adder. The results show that proposed designs have better performances than the best existing structures in terms of common design metrics. The presented 3 × 3 and 4 × 4 dividers are able to achieve 65, 75, 45% and 41, 27, 41% reductions in cell count, latency, and area, respectively.

Introduction: Quantum-dot cellular automata (QCA) technology is one of the suitable nano-computing technologies that may solve CMOS-based device problems because of the scaling down of CMOS. It inculcates a new approach of computation and information transformation. A QCA cell is the basic element in QCA technology, which binds two free electrons within four quantum dots. The fundamental gate in QCA is the majority voter gate that can be configured to construct any QCA structures. All the computations and data propagations are done by a four-phased clocking scheme. Different QCA-based arithmetic logic circuits have been discussed in several works [1–13]. Among these, the design of dividers is the major concern as it has a great impact on the overall performance of any processing unit. 'non-restoring divider' (NRD) algorithm has more advantages over RD algorithm because it overcomes problems such as delay due to the restoration process, realising control logic, and unnecessary power dissipation. In addition, multi-layer QCA designs are not easy to fabricate as well as feasibility of many designs leaves them unfavourable. Therefore, most of the designers restrict themselves by opting single-layer QCA designs. The proposed coplanar QCA divider is based on the non-restoring algorithm, which requires arrays of 'complement adder/subtractor cells' (CAS cells). Each cell is composed of a 2-input Exclusive-OR (XOR) gate and a 1 bit full adder. The proposed designs are not only better than the prior single-layer QCA designs, but also exhibit considerable superiority over the existing multi-layer designs. QCADesigner is used to verify the functional correctness of all proposed designs.

Design of CAS cell: The schematic logic diagram of the CAS cell is depicted in Fig. 1*a*, where the XOR gate takes two inputs: B_i and P (control signal) and results in XOR_OUT. The full adder operates on three inputs: A_i, XOR_OUT, and C_i (input carry). The carry (C_o) and sum (S_i) for the full adder are expressed as follows:

$$C_o = A_i \cdot \text{XOR\_OUT} + \text{XOR\_OUT} \cdot C_i + C_i \cdot A_i \tag{1}$$

$$S_i = A_i \oplus \text{XOR\_OUT} \oplus C_i \tag{2}$$

The QCA implementation of the CAS cell is shown in Fig. 1*b*. The proposed CAS cell uses a new structure for 3-input XOR gate based on QCA cells interactions (as shown in the red box) without incorporating 3-input majority gates. A 2-input XOR gate can be designed by fixing one of the inputs to 0. The 2-input XOR gate is shown in solid square which requires only 13 quantum cells and spreads over an area of 0.02 μm^2, its delay is 0.5 clock cycles (Fig. 1*b*).

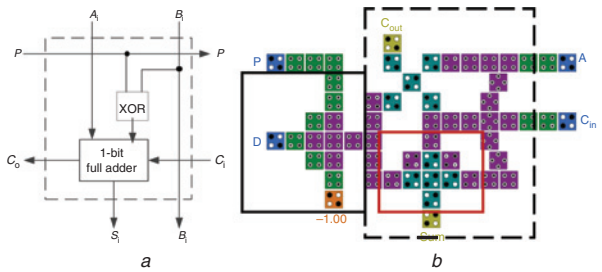

Fig. 1 *CAS cell*
a Schematic logic diagram
b QCA layout

The 1 bit adder is shown in dashed square that comprises only 38 cells and an area occupation of 0.03 μm^2 with 0.5 clock cycles delay (Fig. 1*b*). Our proposed XOR gate, full adder, and NRD have better performance than the prior best designs as shown in Tables 1–3, respectively.

Table 1: Comparison of 2-input XOR gates

XOR gate	Cell count	Latency (clock cycle)	Area (μm^2)	Layer type
[8]	60	1.5	0.09	coplanar
[9]	67	1.25	0.06	coplanar
[10]	29	0.75	0.03	not needed
Proposed	14	0.5	0.02	not needed

Table 2: Comparison of full adders

Full adder design	Cell count	Latency (clock cycle)	Area (μm^2)	Layer type
[1]	79	1	0.064	multi-layer
[2]	73	1	0.04	multi-layer
[3]	60	0.75	0.07	multi-layer
[4]	63	0.75	0.05	coplanar
[5]	59	1	0.043	coplanar
[6]	52	0.75	0.04	coplanar
Proposed	38	0.5	0.03	coplanar

Table 3: Comparison of non-restoring basic cell

CAS cell	Cell count	Latency (clock cycle)	Area (μm^2)	Layer type
[11]	235	1.75	0.35	multi-layer
[12]	147	2.25	0.27	coplanar
Proposed	60	0.75	0.08	coplanar

Design of NRD: Let n be the number of bits for the algorithm, i represents iteration index, R_i is the partial remainder, q is the quotient set, Y is the divisor, and r is the final remainder. Non-restoring division is defined by the following equations [7]:

$$q_{i+1} = \begin{cases} 1, & \text{if } R_i > 0 \\ 0, & \text{if } R_i < 0 \end{cases} \tag{3}$$

$$R_{i+1} = \begin{cases} 2R_i - Y, & \text{if } R_i > 0 \\ 2R_i + Y, & \text{if } R_i < 0 \end{cases} \tag{4}$$

$$r = \begin{cases} 2^{-n} \cdot R_n, & \text{if } R_i > 0 \\ 2^{-n} \cdot (2R_n + Y), & \text{if } R_i < 0 \end{cases} \tag{5}$$

In binary NRD, the partial remainder is calculated from an addition or subtraction of the dividend and the right shifted form of the divisor. The sign of the partial remainder is used to determine the quotient bit. This quotient bit decides whether to add or subtract the shifted divisor in the next cycle.

For the purpose of illustration, we have presented the layout of the 3 × 3 NRD in Fig. 2, which can be extended up to $n \times n$ divider. It comprises a 2D array of adders that help to propagate the carry. A control signal P manages the operation of the CAS cell as a subtractor or an adder. The divisor, dividend, and quotient are represented by $(y_0 y_1 y_2)$, $(x_0 x_1 \times_2 x_3 \times_4)$, and $(q_0 q_1 q_2)$, respectively. The left most bit y_0 and x_0 are used for the signs. Owing to the compact CAS cells, the proposed divider layout achieves minimal latency and area. The QCA implementation of the 3 × 3 NRD requires 1686 cells covering an area of 3.40 μm^2 with 6.75 clock cycles delay.

Comparison results: The comparison results of existing and proposed QCA dividers are shown in Table 4. It can be perceived that the proposed structure excels all the best reported designs presented in [6, 11, 12]. The proposed 4 × 4 divider achieves 38 and 63% improvements in latency and area occupation, respectively, when compared with the best results.

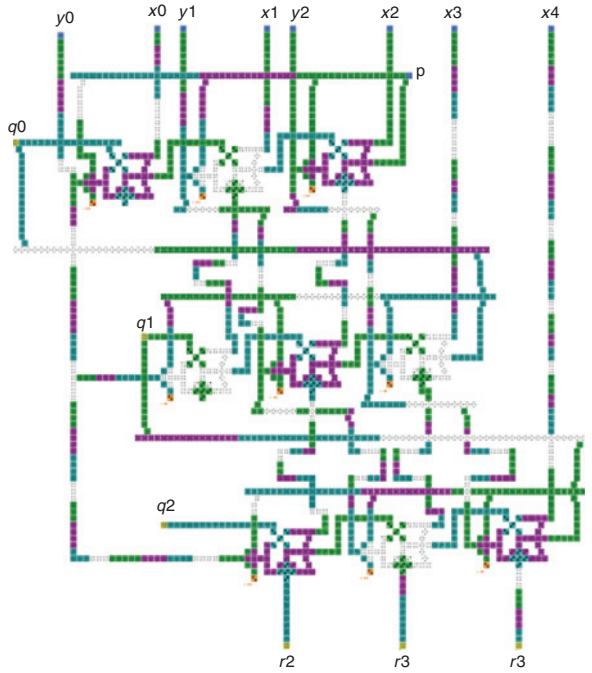

Fig. 2 *QCA implementation of 3 × 3 non-restoring binary divider*

Table 4: Comparison of dividers

Dividers	Cell count	Latency (clock cycle)	Area (μm^2)	Layer type
3 × 3 RD [6]	6451	37	86.22	coplanar
3 × 3 NRD [12]	3742	26.25	6.22	coplanar
Proposed 3 × 3 NRD	1686	6.75	3.40	coplanar
4 × 4 NRD [12]	6865	47.25	10.95	coplanar
4 × 4 NRD [11]	5351	16.5	15.51	multi-layer
Proposed 4 × 4 NRD	3180	12	6.5	coplanar

Plot of latency against different operand size for NRD, RD, and the proposed NRD is shown in Fig. 3.

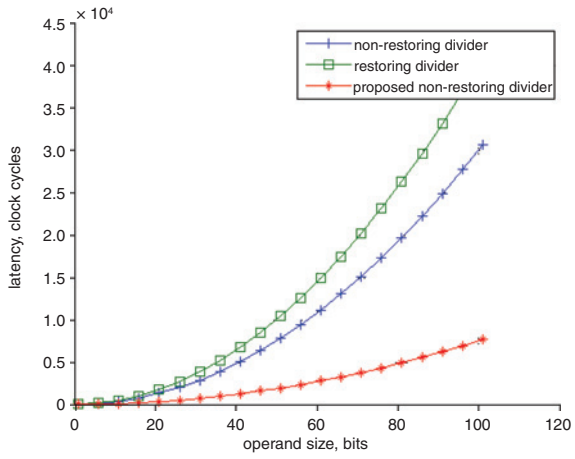

Fig. 3 *Latency of QCA dividers for different operand sizes*

For an n-bit operand size NRD and RD, the latency is given by $3n^2-0.75$ and $4n^2-1$, respectively. In the proposed coplanar n-bit divider some of the wire crossings are done by clock-zone-based crossover approach [14] and the rest are implemented by wires of 45 and 90° cells. Hence, the presented divider achieves an overall latency of $3n^2/4$.

Conclusion: A non-restoring binary array divider is proposed in the correspondence using single-layer QCA technology. Our design uses a more compact form of full adder and XOR gate, which has manifested significant improvements over all existing single-layer and multi-layer designs that resulting in reduced complexity, smaller area, and lower latency. Hence, the presented divider proves to be more advantageous and best alternative for large data size computation.

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One or more of the Figures in this Letter are available in colour online.

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