# High boosting type Z-Source Inverter/ Improved Z-Source Inverter for Solar Photovoltaic System

Vadthya Jagan
Department of Electrical Engineering
Indian Institute of Technology Roorkee
Roorkee - 247 667, India
E-mail: jagan.iitr@gmail.com

Dr. Sharmili Das
Department of Electrical Engineering
Indian Institute of Technology Roorkee
Roorkee - 247 667, India
E-mail: shamanids@gmail.com

***Abstract*— In this paper, two topologies are presented for solar PV system, namely voltage lifting ZSI and voltage lifting Improved ZSI. These proposed inverters possess very high voltage boost. By replacing the middle diode in one of the switched inductor (SL) cell of SL-ZSI/2SL-qZSI with capacitor ($C_{VL}$) high voltage gain can be obtained and also number of L, C and diodes gets reduced, which reduces weight, space and cost of the system. Very small shoot through duty cycle results in high voltage boost, thus efficiency can also be increased. Proposed topologies are analyzed in the steady state and their performances are validated using simulated results obtained in MATLAB/Simulink. This paper presents operating principles, analysis and simulation results, and compares them with SL-ZSI/2SL-qZSI.**

**Keywords— ZSI, qZSI, VL-ZSI, VL-Improved ZSI, SL-ZSI and 2SL-qZSI.**

## I. INTRODUCTION

Conventional energy sources are about to emptied, therefore new type of non-conventional energy sources such as wave, tidal, wind, fuel and solar are encouraged. Among all renewable energy sources PV/solar cell is widely used because of its advantages like it is abundant, clean and pollution free. Globally, the total installed capacity of PV system is about 177GW by the end of 2014 [1].

The characteristics of PV cell changes with Irradiation and Temperature. Therefore, the peak power point also changes. In order to track this peak point and to continuously deliver the maximum available power to the load irrespective of weather condition, several maximum power point tracking techniques are available in the literature [2]. The main drawback of PV cell is that it will produce low DC voltage. So in order to increase this low DC voltage and to convert it to high AC voltage, high boosting Inverters are needed [3].

Conventional single-stage inverter has to be oversized to cope with the wide PV module voltage changes, usually at a range of 1:2. To interface the low output voltage of an inverter to the grid, a bulky low-frequency transformer is necessary at the cost of a large size, decrease in efficiency, loud acoustic noise and high cost [4, 17]. To minimize the KVA rating of the inverter and to boost the voltage to the required level, the two-stage inverter uses a boost converter instead of a transformer [5]. The extra DC/DC stage increases the complexity of the circuit and the cost and reduces the system efficiency. In addition to above mentioned drawbacks, the VSI is vulnerable to EMI noise in terms of reliability. To overcome the conceptual and theoretical barriers and limitation of the VSI, the Z-Source inverter was proposed in 2002 [3].

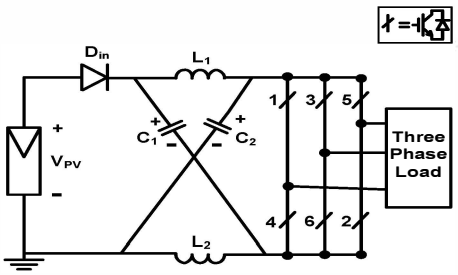



Fig. 1. PV Panel fed Conventional Z-Source Inverter [6].

## II. INTRODUCTION TO CONVENTIONAL IMPEDANCE NETWORK INVERTER TOPOLOGIES

The basic Z-Source Inverter was proposed in [6] as shown in Fig. 1, which provides both buck and boost voltage inversion functions. The 2-port impedance network which uses two capacitors $C_1$ and $C_2$ and two inductors $L_1$ and $L_2$ are connected in the form of X-shape and it couples the main inverter circuit to the PV voltage source. To boost the voltage to the required level an additional shoot through zero state is added to the switching state. When the PV module generates sufficient large voltage to produce the desired AC voltage, then the shoot though zero state is not used and ZSI operates as a conventional VSI (i.e., just like buck inverter).When the PV module produces low voltage, the shoot through state was used to boost the voltage. In the basic ZSI the ground of the DC source is not same as that of the converter and it draws discontinuous input current from the source and the capacitors must sustain high voltages. An Improved ZSI was proposed in [7] is shown in Fig. 2(a), to reduce the drawback of conventional ZSI such as to avoid the voltage stress across the capacitors, to suppress the high inrush current and to reduce the resonance between the inductors and capacitors at start up. To overcome the problems that are found in basic ZSI, the qZSIs were proposed in [8] is shown in Fig. 2(b).

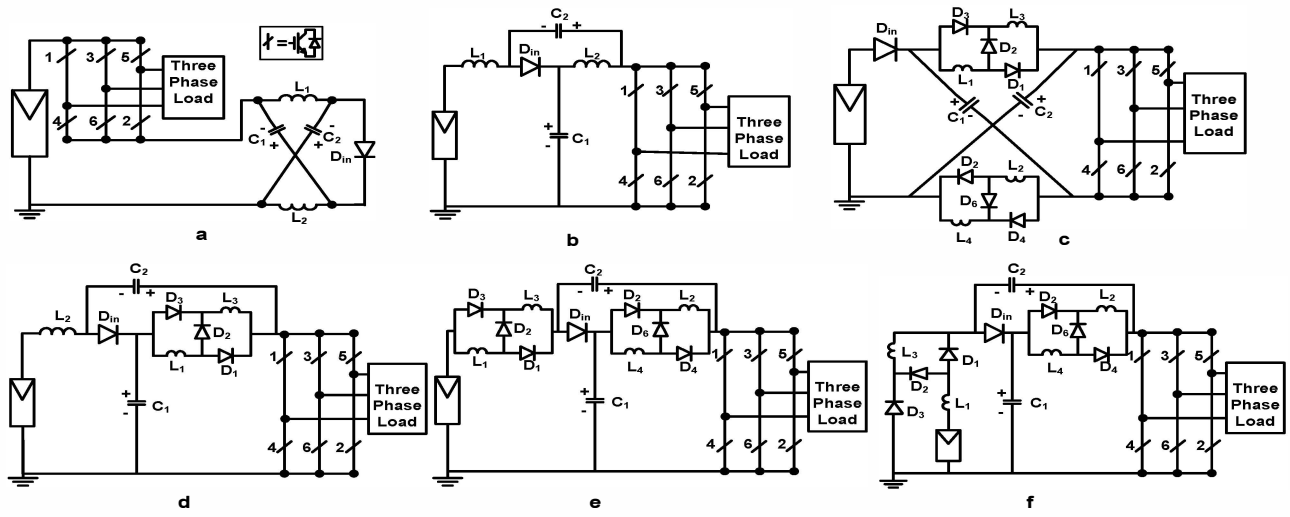



Fig. 2. Different Impedance-Source Inverter topologies. (a). Improved - ZSI [7]. (b). Quasi Z-Source inverter [8]. (c). Switched Inductor Z-Source inverter [9]. (d). One - Switched Inductor Quasi Z-Source inverter [10]. (e). Ripple input current - 2SL-qZSI and (f). Continuous input current - 2SL-qZSI [11].

The boost factor of ZSI, Improved ZSI and qZSI can be expressed as follows.

$$B = \frac{V_{PN}}{V_{PV}} = \frac{1}{(1-2(T_0/T))} = \frac{1}{(1-2D_0)} \quad (1)$$

Where $T_0$ is the shoot through state during the switching period T and $D_0$ is the duty cycle.

The boost factor (1) indicates that when $D_0$ ranges from 0 to 0.5, B varies between zero and infinity. In reality, the infinite value of boost factor is not reachable because of the parasitic effects that are found in the physical components practically. The maximum boost factor of the ZSI, Improved ZSI and qZSI is usually two [11]. Therefore these Impedance source inverters [6, 7 and 8] are not suitable for fuel cell or PV applications where both buck voltage and high boost voltage gain is required. So, in order to improve the boost factor, the switched inductor (SL) cell is placed in place of inductors and is shown in Fig. 2(c). It consists of four inductors ($L_1$, $L_2$, $L_3$ and $L_4$), two capacitors ($C_1$ and $C_2$) and seven diodes ($D_{in}$, $D_1$, $D_2$, $D_3$, $D_4$, $D_5$ and $D_6$). The combinations of $L_1$-$L_3$-$D_1$-$D_3$-$D_5$ and $L_2$-$L_4$-$D_2$-$D_4$-$D_6$ acts as switched inductor (SL) cells. The boost factor of SL-ZSI [9] is increased to:

$$B = \frac{1+D_0}{1-3D_0} \quad (2)$$

Despite this increase in the boost factor, the SL-ZSI has significant drawback similar to basic ZSI [3, 6]. In order to reduce the drawback of SL-ZSI [9] and to increase the boost factor, a new SL-qZSI was proposed in [10]. Only one SL-cell is used to boost the voltage to required level and is shown in Fig. 2(d). $L_1$-$L_3$-$D_1$-$D_3$-$D_2$ combination act as one switched inductor (SL) cell. The boost factor of SL-qZSI is follows

$$B = \frac{1+D_0}{1-2D_0-D_0^2} \quad (3)$$

To further improve the boost factor, a modified 2SL-qZSI's were proposed [11] as shown in Fig. 2(e) and Fig. 2(f). The boost factors of both topologies of 2SL-qZSI is defined as

$$B_r = \frac{1+D_0}{1-3D_0}, \quad B_c = \frac{1}{1-3D_0} \quad (4)$$

The boost factor, $B_r$ of rSL-qZSI is same as that of SL-ZSI [9]. Whereas the boost factor, $B_c$ of cSL-qZSI is lower than SL-ZSI [9]. To further increase the boost factor of an impedance network, two novel topologies are proposed here.

## III. Operation and Principle of Proposed Topologies

Fig. 3 shows the proposed high boosting VL-ZSI and VL-Improved ZSI. The main difference between SL-ZSI/2SL-qZSI and the proposed topologies is, in the proposed topologies only one switched inductor (SL) cell is sufficient to get required boosting factor. For the same input and output voltage, a very small shoot through duty cycle of proposed topologies produces required boosting when compared to SL-ZSI/2SL-qZSI [9, 10, and 11]. Therefore switching losses can be reduced and it increases the system efficiency. The VL-ZSI shown in Fig. 3(a) has the drawbacks similar to SL-ZSI [9], such as discontinuous input current, does not share common ground and higher voltage stress across the capacitors. The VL-Improved ZSI shown in Fig. 3(b) has the following features when compared to VL-ZSI.

- It shares the common ground with DC sources.
- The voltage stress across the capacitors is low and
- It provides continuous and flatter input current from the source.

Table-I shows the comparison of passive components, capacitor voltage stress and peak DC-Link voltages of different impedance network topologies and the proposed topologies. The proposed topology uses lesser passive components and it provides higher voltage gains compared to SL-ZSI/SL-qZSI [9, 10, and 11].

TABLE-I

COMPARISON OF PASSIVE COMPONENTS, VOLTAGE STRESS AND DC LINK VOLTAGE OF PROPOSED TOPOLOGIES WITH OTHER TOPOLOGIES

| | *Conventional ZSI[6]* | *Improved ZSI[7]* | *Quasi ZSI[8]* | *SL-ZSI[9]* | *One-SL-Quasi-ZSI[10]* | *2SL-Quasi-ZSI[11]* | *Proposed Topologies* | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | *VL ZSI* | *Improved VL ZSI* |
| No. of Inductors | 2 | 2 | 2 | 4 | 3 | 4 | 3 | 3 |
| No. of capacitors | 2 | 2 | 2 | 2 | 2 | 2 | 3 | 3 |
| No. of diodes | 1 | 1 | 1 | 7 | 4 | 7 | 3 | 3 |
| $V_{C1}$ | $\frac{(1-D_0)}{(1-2D_0)}V_{PV}$ | $\frac{D_0}{(1-2D_0)}V_{PV}$ | $\frac{(1-D_0)}{(1-2D_0)}V_{PV}$ | $\frac{(1-D_0)}{(1-3D_0)}V_{PV}$ | $\frac{(1-D_0)}{(1-2D_0-D_0^2)}V_{PV}$ | $\frac{(1-D_0)}{(1-3D_0)}V_{PV}$ | $\frac{(1-D_0)}{(1-3D_0)}V_{PV}$ | $\frac{(1+D_0)}{(1-3D_0)}V_{PV}$ |
| $V_{C2}$ | $\frac{(1-D_0)}{(1-2D_0)}V_{PV}$ | $\frac{D_0}{(1-2D_0)}V_{PV}$ | $\frac{D_0}{(1-2D_0)}V_{PV}$ | $\frac{(1-D_0)}{(1-3D_0)}V_{PV}$ | $\frac{2D_0}{(1-2D_0-D_0^2)}V_{PV}$ | $\frac{2D_0}{(1-3D_0)}V_{PV}$ | $\frac{2(1-D_0)}{(1-3D_0)}V_{PV}$ | $\frac{2D_0}{(1-3D_0)}V_{PV}$ |
| Boosting Factor | $\frac{1}{(1-2D_0)}$ | $\frac{1}{(1-2D_0)}$ | $\frac{1}{(1-2D_0)}$ | $\frac{(1+D_0)}{(1-3D_0)}$ | $\frac{(1+D_0)}{(1-2D_0-D_0^2)}$ | $\frac{(1+D_0)}{(1-3D_0)}$ | $\frac{2}{(1-3D_0)}$ | $\frac{2}{(1-3D_0)}$ |
| $V_{CVL}$ | Not Applicable | | | | | | $\frac{(1-D_0)}{(1-3D_0)}V_{PV}$ | $\frac{(1-D_0)}{(1-3D_0)}V_{PV}$ |

Therefore there is a reduction in volume, weight, space and cost of the systems and it also increases the system efficiency.

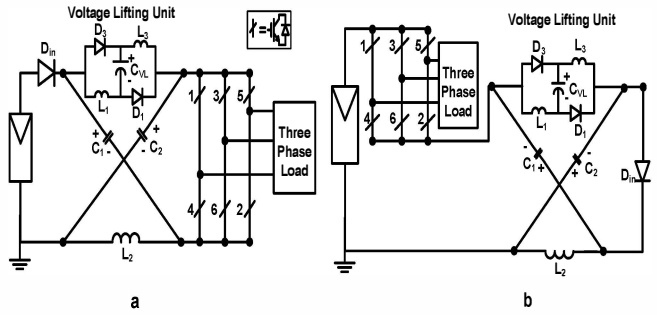



Fig. 3. Proposed high boosting Impedance Source inverter topologies. (a). Voltage Lifting Z Source Inverter, (b). Voltage Lifting Improved ZSI to reduce the capacitor voltage stress.

### *A. Operating principles and derivations of boost factor*

Fig. 4 shows the equivalent circuits of high boosting VL-ZSI and VL-Improved ZSI. These proposed impedance type inverters have an additional shoot through state in addition to the two - zero states and six - active states similar to the conventional Z-source inverter [6]. The combinations of $L_1$-$L_3$-$D_1$-$D_3$-$C_{VL}$ act as Voltage Lifting (VL) unit [18].

*1) Shoot though state:* In this state as shown in Fig. 4(a, c), the diode $D_{in}$ is OFF whereas the diodes $D_1$ and D3 are ON. The inductor $L_2$ of VL-ZSI is charged by capacitor $C_2$ in parallel as shown in Fig. 4(a). Similarly, inductors $L_1$ and $L_3$ are charged by capacitors $C_1$ and $C_{VL}$ in parallel as shown in Fig. 4(a). Whereas the inductor $L_2$ of VL-Improved ZSI is charged by capacitor $C_1$ and input source voltage and the inductor $L_1$ and $L_3$ are charged by capacitor $C_2$ and input source voltage as shown in Fig. 4(c). Therefore inductors $L_1$, $L_2$ and $L_3$ stores energy during shoot through state.

**VL-ZSI**

$$V_{L2} = V_{C2}$$

$$V_{L1} = V_{L3} = V_{CVL} = V_{C1}$$

**VL-Improved ZSI**

$$V_{L2} = V_{PV} + V_{C1}$$

$$V_{CVL} = V_{L1} = V_{L3} = V_{PV} + V_{C2}$$

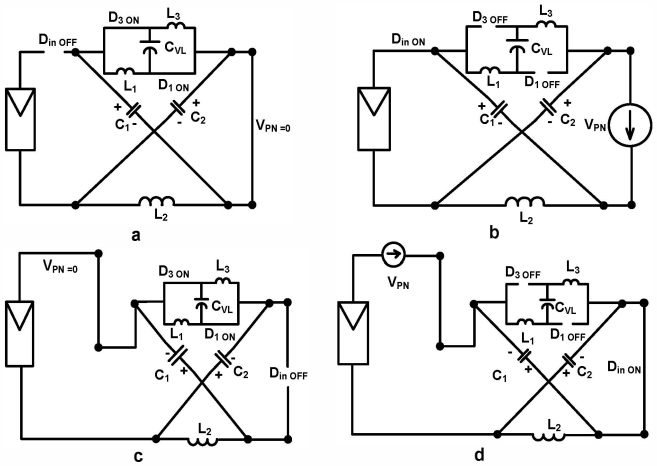



Fig. 4. Equivalent circuits of voltage lifting ZSI (Upper units) and voltage lifting Improved ZSI (Lower units) when the units in (a, c) shoot through state and (b, d) non – shoot through state.

*2) Non- Shoot though state:* In this state as shown in Fig. 4(b, d), the diode $D_{in}$ is ON whereas diodes $D_1$ and $D_3$ are OFF. As shown in Fig. 4(b), the inductors $L_1$ and $L_3$ are connected in series from the voltage lifting unit and the stored energy in these inductors are transferred to the main circuit or DC link. The stored energy in inductor $L_2$ is also transferred to the main circuit. The inductors $L_1$, $L_2$ and $L_3$ are connected in series as shown in Fig. 4(d) and the stored energy in these inductors are also transferred to the main circuit.

**VL-ZSI**

$$V_{L2} = V_{PV} - V_{C1} \tag{5}$$

$$V_{L1} = V_{L1\_non} = V_{PV} + V_{C1} - V_{L3} - V_{C2}$$

$$V_{L3} = V_{L3\_non} = V_{PV} + V_{C1} - V_{L1} - V_{C2}$$

**VL-Improved ZSI**

$$V_{L2} = -V_{C2} \tag{6}$$

$$V_{L1} = V_{L1\_non} = V_{CVL} - V_{C1} - V_{L3}$$

$$V_{L3} = V_{L3\_non} = V_{CVL} - V_{C1} - V_{L1}$$

By applying, the volt-second balance principle to inductors $L_1$ and $L_3$. The average voltage across the inductors $L_1$ or $L_3$ in non-shoot through state of VL-ZSI and VL-Improved ZSI respectively as follows.

$$V_{L1\_non} = V_{L3\_non} = (V_{PV} + V_{C1} - V_{C2}) + \frac{D_0}{(1-D_0)} V_{C1}$$

$$V_{L1\_non} = V_{L3\_non} = (V_{PV} - V_{C1} + V_{C2}) + \frac{D_0}{(1-D_0)} (V_{C1} + V_{PV})$$

At steady state condition, the average voltage of the inductor $L_1$ over one switching period (T) should be zero. From the above two equations.

**VL-ZSI**

$$D_0 V_{C1} + (1-D_0)\{V_{PV} + V_{C1} - V_{C2} + \frac{D_0}{(1-D_0)} V_{C1}\} = 0$$

$$V_{C2} = \frac{(1+D_0)}{(1-D_0)} V_{C1} + V_{PV} \tag{7}$$

**VL-Improved ZSI**

$$D_0(V_{PV} + V_{C2}) +$$

$$(1-D_0)\frac{D_0(V_{PV} + V_{C2}) + (1-D_0)(V_{PV} + V_{C2} - V_{C1})}{(1-D_0)} = 0$$

$$V_{C2} = \frac{(1-D_0)}{(1+D_0)} V_{C1} - V_{PV} \tag{8}$$

Applying Volt-second balance principle to $L_1$ from (5), (6), (7) and (8).

**VL-ZSI**

$$V_{C1} = \frac{(1-D_0)}{(1-3D_0)} V_{PV}, \quad V_{C2} = 2\frac{(1-D_0)}{(1-3D_0)} V_{PV} \tag{9}$$

and the stress across capacitor of the voltage lifting unit,

$$V_{CVL} = \frac{(1-D_0)}{(1-3D_0)} V_{PV} \tag{10}$$

**VL-Improved ZSI**

$$V_{C1} = \frac{(1+D_0)}{(1-3D_0)} V_{PV}, \quad V_{C2} = \frac{2D_0}{1-3D_0} V_{PV} \tag{11}$$

Voltage across the voltage lifting capacitor,

$$V_{CVL} = V_{PV} + V_{C2}$$

Therefore,

$$V_{CVL} = \frac{(1-D_0)}{(1-3D_0)} V_{PV} \tag{12}$$

The peak DC link voltage across the inverter bridge circuit can be written as follows.

**VL-ZSI**

$$V_{PN} = V_{C1} + V_{C2} - V_{PV}$$

$$V_{PN} = \frac{2}{(1-3D_0)} V_{PV} \tag{13}$$

**VL-Improved ZSI**

$$V_{PN} = V_{C1} + V_{C2} + V_{PV}$$

$$V_{PN} = \frac{2}{(1-3D_0)} V_{PV} \tag{14}$$

The boosting factors of both topologies are same and the boost ability of proposed topologies is higher than the SL-ZSI/2SL-qZSI [9, 11]. Fig. 5 compares the boosting factor of different conventional impedance source inverters and proposed topologies.

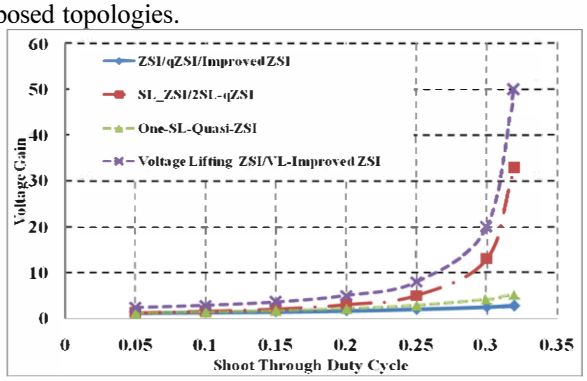



Fig. 5. Comparison of boosting factors of the different Impedance source inverter topologies and the Proposed topologies.

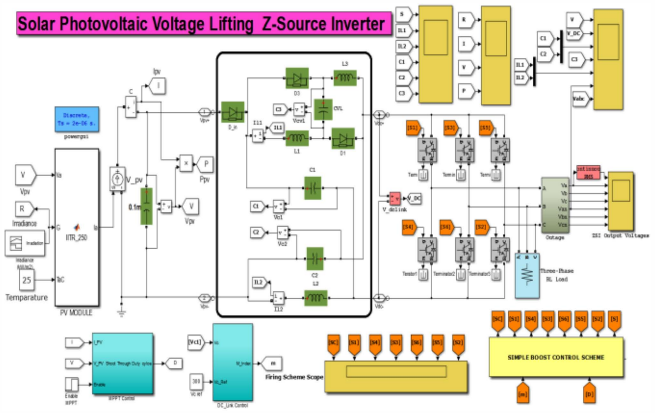
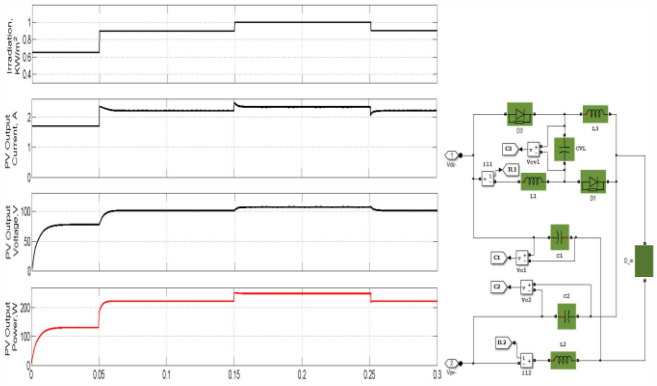



Fig. 6. Simulation diagram of a high boosting type Impedance-Source Inverter.

## B. *PWM control for the proposed topologies*

There are different methods of PWM control techniques are available in literature [12]. Among them simple boost [6], maximum boost [13] and maximum constant boost control [14] are the three basic PWM control techniques. In case of simple boost control method [6], the shoot though time ($T_0$) per total switching cycle is constant, which means the boost factor, B is also constant. The only drawback of this simple boost control is the large voltage stress across the switch. In order to reduce this voltage stress and to increase boosting factor, the maximum boost control method was used for the simulations analysis. In maximum boost control method, by

turning ON all zero states into shoot through zero states, we can achieve maximum shoot though period ($T_0$), thus maximum boost factor for any given modulation index without disturbing the output waveforms.



(a) (b)

Fig. 7. (a). Variation of PV-Module output Current, Voltage and Power under different Insolation condition and (b). Simulation model of VL-Improved ZSI.

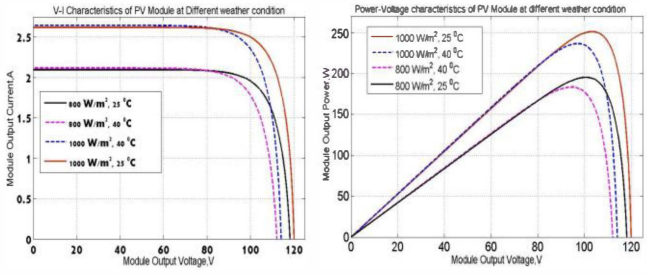



Fig. 8. Characteristics of PV-Module at different Irradiation and Temperature condition.

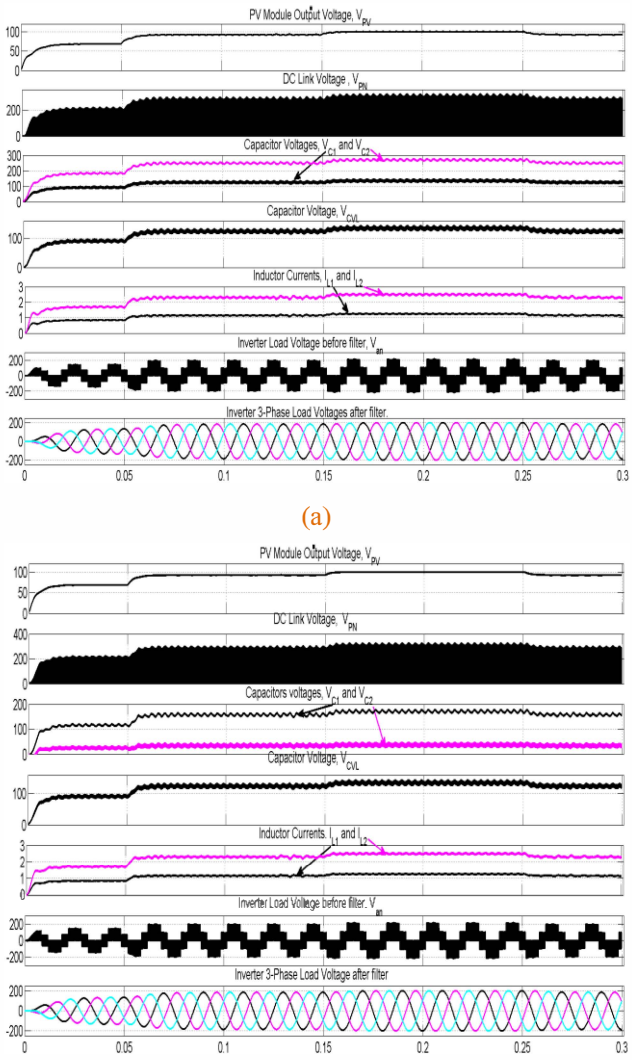
## IV. Simulation Results

To verify the aforementioned theoretical calculations, simulations was performed using MATLAB/Simulink. Photovoltaic module have non linear V-I characteristics. Its output power and output voltage changes according to irradiation and temperature. Fig. 8 shows the characteristics of Photovoltaic module at different Irradiation and temperature levels. The output current of PV module mainly changes with irradiation and the output voltage changes with temperature. The simulations are performed with the following parameters: $L_1 = L_2 = L_3 = 27.2$mH, $C_1 = C_2 = C_{VL} = 5.41\mu$F and Load resistance, R = 100Ω per phase; the switching frequency is 10 kHz.

Table-II: PV MODULE PARAMETERS

| S.No | Parameter | Value |
|---|---|---|
| 1 | Peak output power(MPP) | 251W |
| 2 | No. of series cells | 200 |
| 3 | Voltage at maximum power ($V_{MPP}$) | 103 V |
| 4 | Current at maximum power($I_{MPP}$) | 2.45A |
| 5 | Open circuit voltage($V_{OC}$) | 120V |
| 6 | Short circuit current($I_{SC}$) | 2.62A |

The simulations diagram for the proposed topology of VL-ZSI is shown in Fig. 6. For the VL-Improved ZSI, the impedance network shown in Fig. 6 with block square box replaces with Fig. 7(b). The terminals Vpv+, Vdc+ are short circuited and Vpv- and Vdc- of Fig. 6 is connected with Vpv- and Vdc- of Fig. 7(b) respectively. Table-II shows the PV module parameters at standard test condition(i.e., at irradiation of 1000 W/m$^2$ and Temperature of 25$^0$C).




(a)

(b)

Fig. 9. Simulation results of PV output voltage, DC link voltage, Capacitor voltages, Inductor currents and Inverter output voltage of (a). VL-ZSI, (b). VL-Improved ZSI at $D_0 = 0.12$ and M= 0.88.

Fig. 7(a) shows the variation of PV module output current, voltage and power when there is variation in irradiation and the temperature of PV module is kept constant. The purpose of the system is to produce 3-phase sinusoidal voltage from the PV module whose voltage changes from 20 to 120V DC depending upon weather condition. The tracking of peak power for different insolation condition was shown in Fig. 7(a). When there is a step change in insolation from 0.9 to 1 Sun at 0.15sec, the operating voltage shifts to 103V from 90V and there is corresponding increment in current also. The MPPT was tracking and delivering available peak power to the load irrespective of the weather condition. When the PV

module generates sufficient large voltage to produce the required AC voltage, then the shoot though state is not used and ZSI operates as a conventional VSI (i.e., just like buck inverter).When the PV module produces low voltage, the shoot through state was used to boost the voltage. Therefore to obtain desired output voltage, the shoot through state or the boost factor was used.

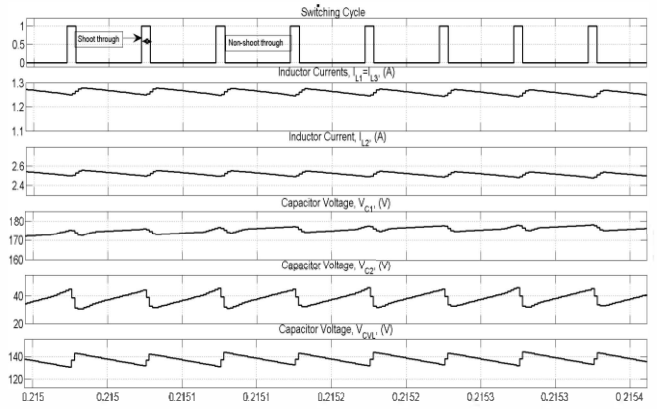



Fig. 10. Simulation results of Inductor currents and Capacitor Voltages during Shoot though and Non-Shoot Through period.

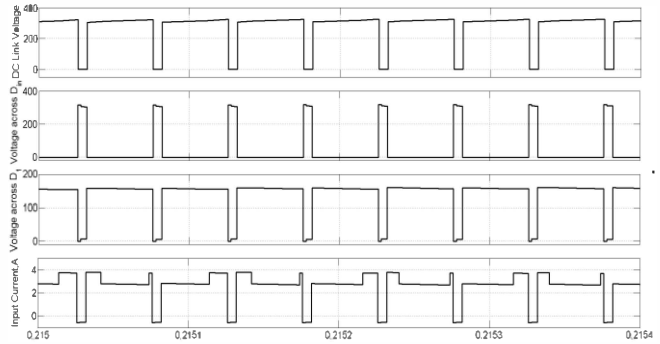



Fig. 11. Simulation results of DC link Voltage, Diode Voltages ($V_{\_Din}$, $V_{D1}$= $V_{D3}$) and Input current to the VL-ZSI.

Fig. 9 shows the variation of Module output voltage ($V_{PV}$), DC-Link voltage ($V_{PN}$), Capacitor voltages ($V_{C1}$, $V_{C2}$ and $V_{CVL}$), Inductor currents ($I_{L1}$, $I_{L2}$) and Load voltage under the variation of weather condition. These simulations are performed in open loop condition. Even though, the variation in weather condition occurs, the PV module was operating at peak power point as shown in Fig. 7(a). An incremental conductance technique was used here to track the maximum power point [16]. From Fig. 9(a) we can observe that, the stress across the capacitor $C_2$ is more while using VL-ZSI. To reduce the stress across the capacitor $C_2$, the VL-Improved ZSI is preferred. Fig. 10 shows the currents through the inductors ($I_{L1}$, $I_{L2}$ and $I_{L3}$) and the voltage across the capacitors ($V_{C1}$, $V_{C2}$ and $V_{CVL}$) and Fig. 11 shows the dc link voltage, diode voltages and input current during shoot through and non-shoot through states.

## V. Conclusion

This paper presents the operating principles and analysis of high boosting type VL-ZSI and VL- Improved ZSI and are possess very high voltage boost. Compared with the SL-ZSI and 2SL-qZSI, for the same input and output voltage, the proposed topologies offers reduced passive component count, less space, reduced capacitor stress, higher voltage boost, lower shoot through period and higher modulation index which results in lower THD. Therefore these topologies are applicable to fuel cell or photovoltaic applications..

## References


[1] International Energy Agency, "PVPS report snapshot of global PV 1992-2013, " Rep. IEAPVPS T1-24:2014.

[2] T. Esram and P.L.,Chapman, "Comparison of Photovoltaic Array Maximum PowerPoint Tracking Techniques," *IEEE Trans. on Energy Conversion*, Vol. 22, No. 2, pp. 439- 449, June 2007.

[3] F. Z. Peng, "Z-Source Inverter," in *Proc. IEEE/IAS Annu. Meeting*, pp. 775–781, Oct.2002.

[4] S. Jain and V. Agarwal, "A single-stage grid connected inverter topology for solar PV systems with maximum power point tracking, " *IEEE Trans. Power Electron.,* vol. 22, no. 5, pp.1928 -1940. Sep-2007.

[5] G. R. Walker and P. C. Sernia, "Cascaded DC-DC converter connection of photovoltaic modules," *IEEE Trans. Power Electron.,* vol. 19, no. 4, pp.1130 -1139 2004.

[6] F. Z. Peng, "Z-Source Inverter," *IEEE Trans. Ind. Appl.,* vol. 39, No. 02, pp.504–510, Mar./Apr. 2003.

[7] Y. Tang, S. J. Xie, C. H. Zhang and Z. G. Xu, "Improved Z-source inverter with reduced Z-source capacitor voltage stress and soft-start capability," *IEEE Trans. Power Electron.,* vol. 24, no. 2, pp. 409–415, Feb. 2009.

[8] Anderson, J., Peng, F.Z., "Four quasi-Z-Source inverters," *Proc. of IEEE Power Electronics Specialists Conference PESC'2008*, pp. 2743-2749, 15-19 June 2008.

[9] M. Zhu, K. Yu, and F. L. Luo, "Switched inductor Z-source inverter," *IEEE Trans. Power Electron.,* vol. 25, no. 8, pp. 2150–2158, Aug. 2010.

[10] M.K. Nguyen, Y. Lim and G. Cho, "Switched-inductor quasi-Z-source inverter," *IEEE Trans. Power Electron.,* vol. 26, no. 11, pp. 3183–3191,Apr. 2011.

[11] M.K. Nguyen, Y.C. Lim and J.H. Choi, "Two switched-inductor quasi-Z-source inverters," *IET Power Electronics,* vol. 5, no. 7, pp.1017-1025, August 2012.

[12] Miaosen Shen, Jin Wang, Alan Joseph, Fang Z. Peng, Leon M. Tolbert and Donald J. Adams, "Maximum Constant Boost Control of the Z-Source Inverter," *Proc. of IEEE IAS* 2004.

[13] F. Z. Peng, M. Shen and Z. Qian, "Maximum boost control of the Z-source inverter," *IEEE Trans. Power Electron.,* vol. 20, no. 4, pp. 833–838, Jul. /Aug. 2005.

[14] M. Shen, J. Wang, A. Joseph, F. Z. Peng, L. M. Tolbert, and D. J. Adams, "Constant boost control of the Z-source inverter to minimize current ripple and voltage stress," *IEEE Trans. Ind. Appl.,* vol. 42, no. 3, pp. 770–778, May/Jun. 2006.

[15] Y. Liu, Baoming Ge, Haitham Abu-Rub and F.Z. Peng, "Overview of Space Vector Modulations for Three-Phase Z-Source/Quasi-Z-Source Inverters," *IEEE Trans. Power Electronics,* vol. 29, no. 4, pp. 2098-2108, April 2014.

[16] K. H. Hussein, I. Muta, T. Hoshino and M. Osakada, "Maximum photovoltaic power tracking: An algorithm for rapidly changing atmospheric conditions," *Proc. IEE - Generation, Transmission, Distribution,* vol. 142, no. 1, pp. 59–64, Jan. 1995.

[17] T. J. Liang, Y. C. Kuo and J. F. Chen, "Single-stage photovoltaic energy conversion system," *Proc. Inst. Elect. Eng.,* vol. 148, no. 4, pp.339 - 344 2001.

[18] Linlin Li and Yu Tang, "A high set-up quasi-Z-source inverter based on voltage-lifting unit," *IEEE - Energy Conversion Congress and Exposition (ECCE)*, pp. 1880 - 1886, Sept. 2014.