An Improved Quasi-Z-Source Inverter for Grid-Connected Photovoltaic System

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Abstract—An improved quasi-Z-source inverter for grid-connected photovoltaic system is proposed in this study. Two tapped-inductors are substituted for the inductors of quasi-Z-source inverter (qZSI) respectively. Compared with the classic topology, the proposed topology can not only arise the boost ability but also make the voltage stress be decreased. The operation principle and voltage stress of the proposed topology is analyzed theoretically and compared with that of qZSI and switched-inductor quasi-Z-source inverter (SL-qZSI). The results of simulations and experiments are shown to validate the feasibility of the proposed topology.

Index Terms—tapped-inductor, quasi-Z source inverter, boost ability, voltage stress.

I. I NTRODUCTION

The Z-source-inverter (ZSI) uses an unique impedance network to overcome the disadvantages of the conventional voltage-source inverters [1]. ZSI can boost the input voltage using the shoot-through state and modulation index in a single stage. Besides, no dead time is needed, thus the output voltage is free from voltage distortion. So it is very suitable for application with low input voltages, such as photovoltaic and fuel cells [2-5]. However, traditional ZSI has several obvious disadvantages, such as low boost ability, discontinuous input current and high voltage stress in capacitors and switches. To overcome the defects of ZSI, quasi-Z-source inverter (qZSI) was proposed in [6], [7]. Compared with classical ZSI, qZSI has some advantages such as continuous input current and lower passive component ratings.

Though qZSI has overcome the disadvantages of ZSI, its boost factor is as the same as ZSI. Therefore, the improvement on qZSI is something worthy of researching.

In [8], a step-up network is added before qZSI to improve boost ability, but the topology is complicated and the boost ability is still limited. In [9], two coupled magnetic inductors are used instead of the inductors of qZSI to improve boost ability. Though the topology is simplified, it is difficult to avoid the negative effect of leak inductance. In [10], a switched-inductor quasi-Z-source inverter (SL-qZSI) is proposed. Though SL-qZSI improves the performance of classical qZSI, its boost ability is also limited.

To enhance the boost ability of qZSI, this paper applies tapped-inductor to traditional qZSI to create an improved qZSI. Compared with qZSI and SL-qZSI, the improved qZSI has higher boost ability, lower voltage stress on capacitors. Finally, the feasibility and correctness of the proposed algorithm are verified through the simulation and experimental results.

II. QZSI and SL-qZSI

Fig.1 shows the topology of qZSI, which inserts the shoot-through zero vector in the traditional zero vector to get the boost ability by using the shoot-through state and the modulation index in a single stage.

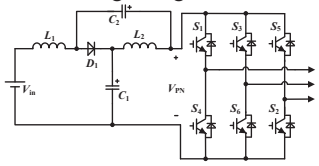

Fig. 1. The topology of qZSI

According to [1], the booster factor of qZSI is:

$$B = \frac{V_{PN}}{V_{dc}} = \frac{1}{1-2D} \tag{1}$$

Where D is the ratio of the shoot-through time T_{sh} and the switching period T, V_{PN} is the peak value of the DC link voltage.

Fig. 2 shows the topology of SL-qZSI, which uses a switched inductor to replace the original inductance L_2 to increase the boost ability.

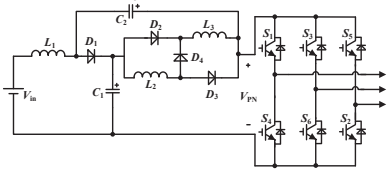

Fig. 2. The topology of SL-qZSI

From [10], the booster factor of SL-qZSI is:

$$B = \frac{1+D}{1-2D-D^2} \tag{2}$$

According to formula (1) and (2), although SL-qZSI has higher boost ability than qZSI, its range of promoting is limit. Thus, the shoot-through duty ratio should be higher when we need higher booster gain, what creates lower modulation index. According to [1], low modulation index will cause the deterioration of fundamental frequency inversion of the inverter, as well as bringing in high order harmonic distortion, which will significantly reduce output performance.

III. The Proposed Topology

The topology of improved qZSI can be seen in Fig. 3.

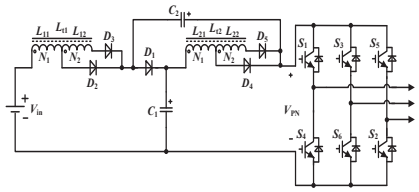

Fig. 3. The topology of improved qZSI

By using two groups of passive network including the tapped-inductor to replace the inductance (L_1 and L_2) in traditional qZSI, the higher boosting ability can be obtained. For the convenience of analysis, in the modified topology, the parameters of two tapped-inductors are the same, and considering the coupling coefficient is not 1 in actually, the following equation can be obtained.

$$\begin{cases} L_{11} = L_{21} \\ L_{12} = L_{22} \\ L_{11} + L_{12} = L_{21} + L_{22} = L_{t1} = L_{t2} \\ N = N_2 / N_1 \\ L_{12} / L_{11} = L_{22} / L_{21} = N^2 K^2 \\ L_m = K\sqrt{L_{11}L_{12}} = K\sqrt{L_{21}L_{22}} \end{cases} \tag{3}$$

Where N is the turn ratio of the tapped inductor, N_2 is the number of turns of L_{12} and L_{22}, N_1 is the number of turns of L_{11} and L_{21}, L_m is the mutual inductance, K is the coupling coefficient. For the convenient of analysis, the tapped-inductor is viewed as an ideal state whose K is equal to 1 [11].

A. Circuit Analysis

As same as traditional qZSI, the modified qZSI also has extra shoot-through zero vector except traditional six effective vectors and two zero vectors. Therefore, its working principle is similar to traditional qZSI which has two working conditions that are shoot-through state and non-shoot-through state.

1) Shoot-through State

When the inverter is in the shoot-through state, which can be equivalent to the short circuit condition, its equivalent circuit diagram is shown in Fig. 4.

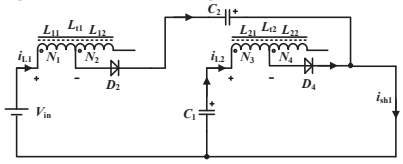

Fig. 4. Shoot-through state

During the shoot-through state, D_1, D_3 and D_5 are off, while D_2 and D_4 are on. The following circuit equation can be obtained:

$$\begin{cases} V_{L11} = V_{C2} + V_{in} \\ V_{L12} = N(V_{C2} + V_{in}) \\ V_{L21} = V_{C1} \\ V_{L22} = NV_{C1} \end{cases} \tag{4}$$

2) Non-shoot-through State

The state includes six effective vectors and two zero vectors. The inverter bridge can be equivalent to a voltage source, whose equivalent circuit diagram is shown in Fig. 5.

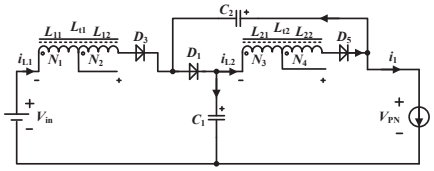

Fig. 5. Non-shoot-through state

During the non-shoot-through state, D_1, D_3 and D_5 are on, while D_2 and D_4 are off. The following circuit equation can be obtained:

$$\begin{cases} V_{L12} = NV_{L11} \\ V_{L11} = V_{C1} - V_{in} - V_{L12} \Rightarrow V_{L11} = \dfrac{V_{C1} - V_{in}}{1+N} \\ V_{L22} = NV_{L21} \\ V_{L21} = V_{C2} - V_{L22} \Rightarrow V_{L21} = \dfrac{V_{C2}}{1+N} \end{cases} \tag{5}$$

Applying the volt-second balance principle to the inductors (L_{11} and L_{21}) and setting the shoot-through duty ratio as D, from (4) and (5) we obtain:

$$\begin{cases} D(V_{C2} + V_{in}) = (1-D)\dfrac{V_{C1} - V_{in}}{1+N} \\ DV_{C1} = (1-D)\dfrac{V_{C2}}{1+N} \end{cases} \tag{6}$$

Following formula can be derived by (6)

$$\begin{cases} V_{C1} = \dfrac{1-D}{1-ND-2D} V_{in} \\ V_{C2} = \dfrac{ND+D}{1-ND-2D} V_{in} \end{cases} \tag{7}$$

Due to $V_{PN}=V_{C1}+V_{C2}$, so the peak voltage of the DC link can be described as follows:

$$V_{PN} = \frac{1+ND}{1-ND-2D} V_{in} = BV_{in} \tag{8}$$

Where B 错误!未找到引用源。 is the boost factor of the improved qZSI.

From formula (8), we can see that the boost factor is decided by both the shoot-through duty ratio and the turn ratio. When the shoot-through duty ratio is fixed, the boost factor increases with the turn ratio.

Fig.6 shows the comparison of the boost ability of the three topologies.

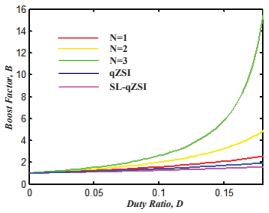

Fig. 6. Comparisons of the boost ability of the three topologies

It can be seen from Fig.6 clearly that, compared with qZSI and SL-qZSI, the modified qZSI has higher boost factor with the same shoot-through duty cycle, which makes modulation ratio M has greater modulation range. Therefore, the improved qZSI will improve the quality of output.

B. Boost Control Strategy

The modified space-vector PWM (SVPWM) control strategy is proposed in this paper because it leads to high utilization ratio of the dc-link voltage, lower harmonic distortion rate, fast dynamic response and higher modulation index [12].

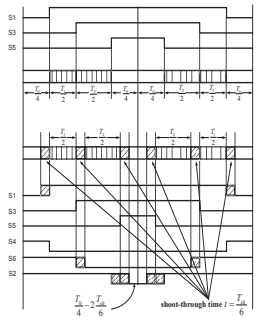

Fig. 7. Modified SVPWM switching sequence

Any given reference voltage can be obtained through synthesizing the neighboring basic space vector and zero vector. By taking part of the zero vector time as shoot-through state time, we derive a modified SVPWM strategy without having effects on resultant voltage vector and switching frequency. The improved space vector in a switching period is divided into active vector, zero vector and shoot-through zero vector. The modified SVPWM switching sequence is shown in Fig.7.

IV. Comparison to QZSI and SL-qZSI

A. Voltage Gain

As the description of [1], the voltage gain G can be described as:

$$G = MB = \frac{V_0}{V_{in}/2} \tag{9}$$

Where V_0 is the peak value of output phase voltage, V_{in} is the input voltage.

According to [12], the average duty ratio of shoot-through state D can be described as:

$$D = \frac{2\pi - 3\sqrt{3}M}{2\pi} \tag{10}$$

Substituting formula (8) and (10) into (9), the voltage gain G of the improved qZSI can be described as:

$$G = MB = \frac{\pi M - \sqrt{3}M^2}{2\sqrt{3}M - \pi} \tag{11}$$

Fig.8 shows the comparison of the voltage gain in the three topologies. As shown in Fig.8, under the same voltage gain, the improved topology possesses larger modulation index than the other two topologies. So, the output quality of the inverter is improved.

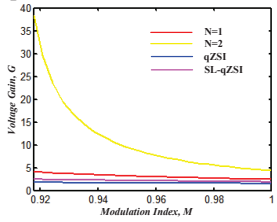

Fig. 8. Comparisons of the voltage gain in the three topologies

Fig.9 represents the correlativity between the voltage gain and the shoot-through duty ratio of the three topologies. As shown in Fig.9, the improved topology need lower shoot-through duty ratio than the other two topologies under the same voltage gain. Thus, the power loss of the improved topology will become less than qZSI and SL-qZSI.

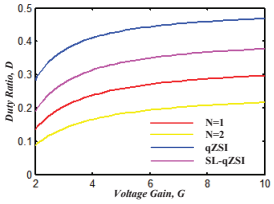

Fig. 9. Relationship between the voltage gain and shoot-through ratio of the three topologies

B. Capacitor Voltage Stress

To be fair, the three inverters are set to have the same input voltage V_{in} and the same voltage gain G. From equation (10), we can obtain:

$$M = \frac{2\pi - 2\pi D}{3\sqrt{3}} \tag{12}$$

Substituting formula (12) into formula (9), the shoot-through duty ratio D of the improved qZSI can be described as:

$$D = \frac{2\pi N + 6\sqrt{3}G + 3\sqrt{3}GN - 2\pi - \sqrt{\Delta}}{4\pi N} \tag{13}$$

Where

$$\Delta = (2\pi - 2\pi N - 6\sqrt{3}G - 3\sqrt{3}GN)^2 - 8\pi N(3\sqrt{3}G - 2\pi)$$

Substituting formula (13) into formula (7), the voltage stress across C_1 of the improved qZSI can be obtained.

Similarly, the shoot-through duty ratio D of SL-qZSI can be represented as:

$$D = 1 - \frac{3\sqrt{3}\cdot\left[(24\sqrt{3}\pi G - 8\pi^2) - \sqrt{\Delta}\right]}{4\pi(27G - 6\sqrt{3}\pi)} \tag{14}$$

Where $\Delta = (8\pi^2 - 24\sqrt{3}\pi G)^2 - 32\pi^2 G(27G - 6\sqrt{3}\pi)$

The shoot-through duty ratio D of qZSI can be represented as:

$$D = \frac{2\pi^2 + \pi G - 6\sqrt{3}\pi G}{2\pi^2 - 6\sqrt{3}\pi G} \tag{15}$$

Substituting equation (14) and (15) into the equation of C_1 for SL-qZSI and qZSI, the voltage stress across C_1 of SL-qZSI and qZSI can be obtained respectively.

Fig.10 describes the voltage stress across C_1 of the three topologies. As shown in Fig.10, when turn ratio N=1, the voltage stress across C_1 of the improved topology is larger than SL-qZSI and smaller than qZSI under the same voltage gain; when turn ratio N=2, the voltage stress across C_1 of the improved topology is smaller than qZSI and SL-qZSI under the same voltage gain.

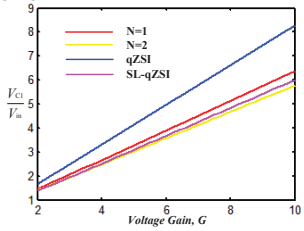

Fig. 10. Comparison of voltage stress across C_1 in the three topologies

The analysis of C_2 is similar to the analysis of C_1. Fig.11 describes the voltage stress across C_2 of the three topologies. As shown in Fig.11, when turn ratio N=1 and N=2, the voltage stress across C_2 of the improved qZSI is all lower than qZSI and SL-qZSI under the same voltage gain.

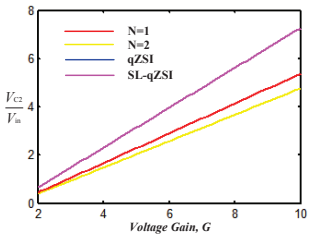

Fig. 11. Comparison of voltage stress across C_2 in the three topologies

V. Simulation Results

A. *Simulation Analysis of Boost Capacity*

In order to verify the above theoretical analysis, the simulation models of the three topologies were built by Matlab. The simulation parameters are shown as follows: L_{t1}=L_{t2}=L_1=L_2=L_3=1mH, C_1=C_2=2200μF, V_{in}=48V, D=0.15, N=2, L_f=5mH, C_f=20μF. The switching frequency is 10kHz, the three-phase balanced load is R=20Ω. In the simulation, all of the components are ideal.

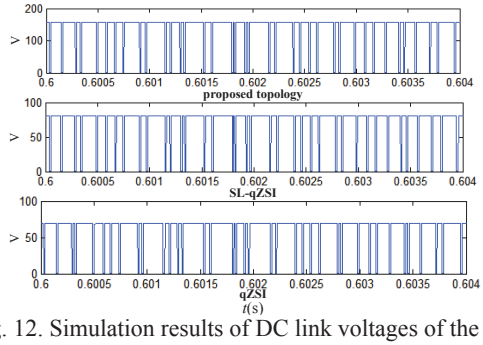

Fig. 12. Simulation results of DC link voltages of the three topologies when D is 0.15

Fig.12 shows the DC link voltages of the three topologies. From Fig.12, we can see that the peak value of the DC link voltage of the three topologies is 156V, 81V and 68V respectively. It indicates that the proposed topology has stronger boost ability.

B. *Simulation Analysis of the Voltage Stress*

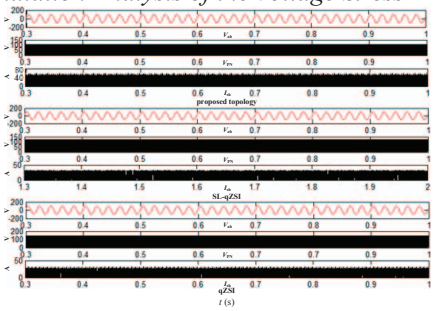

Fig. 13. Simulation results of output line-to-line voltages, DC link voltages and shoot-through currents of the three topologies based on the same voltage gain

Figs.13 and 14 show the simulation results of the DC link voltages, the shoot-through current and the capacitor voltage for the three topologies when the input voltage is 48V and the output line-to-line voltage is 100V. As shown in Fig.13, the DC link voltage of the three topologies is boosted to 108V, 130V and 145V respectively under the above condition. It indicates that the DC link voltage of the proposed topology becomes the lowest among the three topologies when they produce the same voltage gain. The result means that the voltage stress across the IGBTs of the proposed topology is smaller than that of the other two topologies.

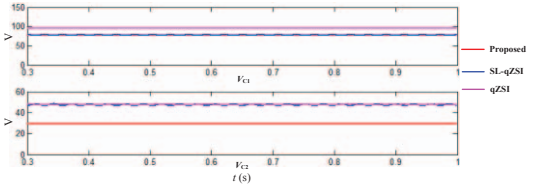

Fig. 14. Simulation results of V_{C1} and V_{C2} of the three topologies based on the same voltage gain

As shown in Fig.14, the voltage of C_1 for the proposed topology is slight lower than SL-qZSI and lower than qZSI, the voltage of C_2 for the proposed topology is lower than SL-qZSI and qZSI. It indicates that the voltage stress across the capacitors of the proposed topology are lower than the other two topologies. The simulation results are in good agreement with the theoretical analysis.

VI. Experimental Results

Experiments were carried out based on the TMS320F28335 DSP to verify the properties of the improved topology, and the experimental parameters were as the same as the simulation parameters.

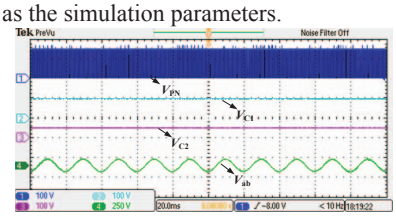

Fig. 15. The DC link voltage, capacitor voltage and output line-to-line voltage of the improved topology when D is 0.15

Fig.15 shows the DC link voltage, the capacitor voltage and the output line-to-line voltage when the shoot-through duty ratio is 0.15. As shown in Fig.15, for the reasons of the drop voltages of diodes and the line impedance, V_{PN}, V_{C1} and V_{C2} are boosted to 150V, 98V and 52V respectively. The experimental results are consistent with the theoretical analysis and the simulation results. It indicates that the improved topology has stronger boost ability compared with qZSI and SL-qZSI.

Fig.16, Fig.17 and Fig.18 show the DC link voltage, the capacitor voltage of the improved topology, SL-qZSI and qZSI respectively when the output line-to-line voltage is 100V. As shown in Fig.16, Fig.17 and Fig.18, when the output line-to-line voltage is 100V, V_{PN}, V_{C1} and V_{C2} of the improved topology are boosted to 104V, 76V and 28V respectively; V_{PN}, V_{C1} and V_{C2} of SL-qZSI are boosted to 122V, 76V and 46V respectively; V_{PN}, V_{C1} and V_{C2} of qZSI are boosted to 140V, 94V and 46V respectively. The experimental results indicate that with the same voltage gain, the improved topology has the lowest DC link voltage and the capacitor voltage. The experimental results are in good agreement with the simulation results and verify the correctness of the theoretical analysis.

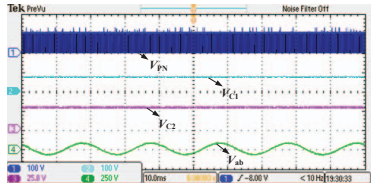

Fig. 16. The DC link voltage, capacitor voltage of the improved topology when output line-to-line voltage is 100V

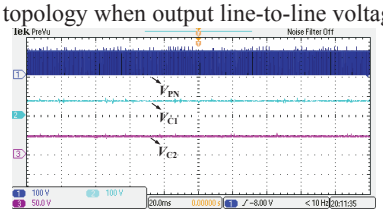

Fig. 17. The DC link voltage, capacitor voltage of SL-qZSI when output line-to-line voltage is 100V

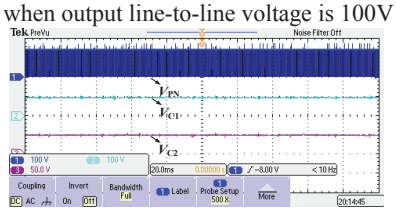

Fig. 18. The DC link voltage, capacitor voltage of qZSI when output line-to-line voltage is 100V

VII. Conclusion

This paper proposes an improved qZSI based on the classical qZSI. The proposed topology not only has the advantages of qZSI but also possess higher boost ability compared with qZSI and SL-qZSI. And with the same input voltage and the output voltage, the proposed topology produces lower DC link voltage and capacitor voltage. The improved topology uses higher modulation index than the other two topologies when the voltage gain is same. Meanwhile, unlike qZSI and SL-qZSI, the boost factor of the improved qZSI is decided by two factors: the shoot-through duty ratio *D* and the turn ratio *N*. So its design is more flexible. The simulation results and the experimental results have demonstrated these properties of the proposed topology.

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His current research interests include Z-source inverters, digital control of power converters and renewable energy.