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NoC routing protocols – objective-based classification

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ABSTRACT

NoCs (Network on Chips) are the most popular interconnection mechanism used for systems that require flexibility, extensibility and low power consumption. However, communication performance is strongly related to the routing algorithm that is used in the NoC. The most important issues in the routing process are: deadlock, livelock, congestion and faults. In this paper, a classification of NoC routing protocols is proposed according to the problems they address. Two main families emerge: mono objective and multi objectives. A discussion of the advantages and the drawbacks of each protocols family is given. A summary of the most used practices in this field and the less used ones is provided. This survey shows that it is hard to satisfy the four objectives at the same time with classical methods, highlighting the strengths of multi-objectives approaches.

1. Introduction

New applications running on SoCs (Systems on Chip) require additional performance because of their complexity and heterogeneity. Consequently, the need in more efficient communication mechanisms are constantly growing. This is why, inspired from traditional computer networks, the NoC (Network on Chip) paradigm was created.

NoCs were created to improve the following parameters: (i) bandwidth scalability compared to traditional bus architectures; (ii) energy efficiency and reliability; (iii) reusability.

A NoC architecture consists of a set of nodes called IPs (Intellectual Property) that may represent embedded memories, application specific components or mixed-signal I/O cores. Each IP has one router to ensure packets routing. A middle layer named adapter or network interface (NI) connects routers to IPs. All these components are connected by links.

The main role of a NoC is to ensure communication between IPs. The network reliability relies on a good communication strategy. Since the connectivity is not complete, routing is necessary to ensure packet transmission between source and destination nodes.

The design of NoC routing algorithms requires two types of parameters: those related to NoC architecture and those defining the routing protocol itself (Fig. 1)

Architecture parameters allow to determine the network topology (which can be regular 2D/3D or irregular); the type of the networks (static [1] or dynamic [2]), and two flow control methods [3][4][5]: buffered (using one of the following policies: Credit-based, handshake, Stall/Go, T-error, DBFC [6]), or unbuffered.

The routing algorithm must also be characterized by the strategy that is used for sending packets if it is source or distributed; its path definition strategy which can be deterministic, oblivious or adaptive (partially or totally); its commutation mode that may be packet switching, circuit switching or the hybrid mode named time division circuit. Finally, a routing protocol have to employ one of the following storing policies [1][7][8]: Store and forward, Virtual-cut-Through or wormhole.

Several works exist in this field where various techniques are proposed to address the routing problem from different points of view. They use different configurations and network models according to the parameters described above. However, it is not easy to point out the still pending issues. This is why a classification is necessary to better situate the various research works, to measure their complexity and their impact on network performance.

In this context, many surveys have been presented in literature proposing classifications or sets of routing protocols according to given characteristics. In the following, some related works are stated: Ni and McKinley [9] present one of the first surveys about NoC routing protocols treating wormhole routing techniques in direct networks. Boppana and Chalasani [10] perform a comparison of adaptive wormhole routing algorithms where several wormhole routing protocols are evaluated with various degrees of adaptivity. Al-Tawil et al. [4] present a survey of wormhole routing algorithms in mesh networks and a comparison between them taking into consideration the approach adaptivity, the length of paths, the

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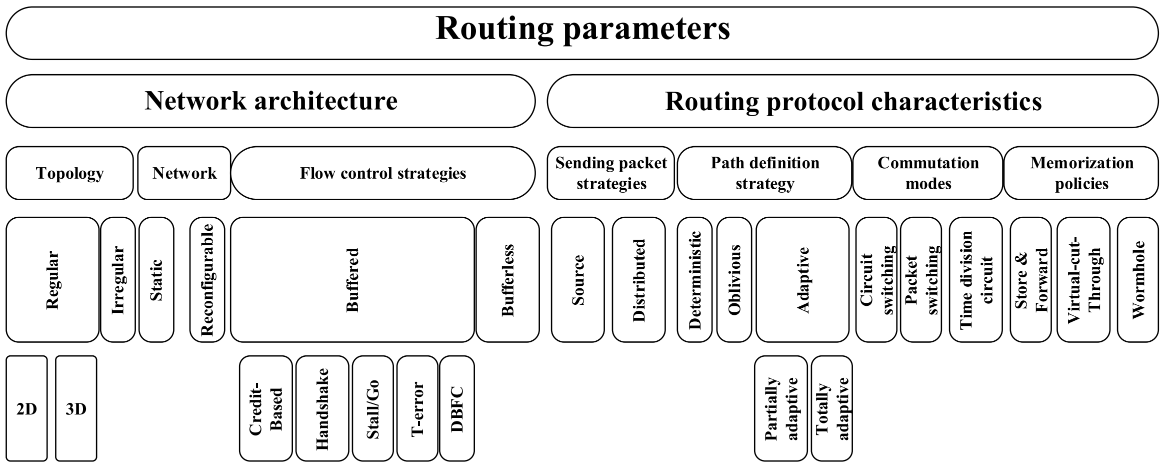

Fig. 1. NoC routing parameters.

presence of virtual channels, the topology and the number of tolerated faults. Chiu [11] enumerates a number of routing protocols developed for NoCs. Rantala et al. [12] present some oblivious and adaptive routing protocols. Bjerregaard and Mahadevan [13] give a complete survey of research and practices of NoC where various properties which can characterize the different routing protocols are defined. Similar work is presented by Agarwal et al. [3], where routing protocols are classified in various ways according to the routing decision, the length of path, the number of destinations and many other criteria. Boyan and Littman [14] present some protocols developed for irregular topologies and based on routing tables. Atagoziyev [7] analyses a number of routing protocols and makes a comparison between them. Gratz et al. [15] gather a number of protocols and make a classification according to the congestion criterion. Montanana et al. [16] summarize a set of fault tolerant routing protocols. Flich et al. [17] classify routing algorithms based on their requirements and their foundations. Routing protocols have been classified primarily based on their requirements for virtual channels, and their capability to guarantee minimal routing. Ebrahimi [18] presents also a number of NoC routing protocols aiming to avoid congestion with different techniques such as: collecting the network information, using artificial intelligence algorithms and employing 3D topology. Finally, Ebrahimi and Daneshtalab [19] present learning-based routing algorithms for on-chip networks.

The present work proposes a classification based on NoC routing algorithm objectives, which are: deadlock freedom, livelock freedom, congestion-awareness and fault tolerance. The reason for choosing this classification criteria is due to the fact that solutions proposed to reach these objectives are directly related to network performance. Consequently, a synthesis of existing strategies can clearly show the most studied objectives, frequently used techniques, pros and cons of each of them and those which are resource greedy.

The rest of this paper is organized as follows: the second section presents the four main NoC routing issues and the solutions proposed in the literature to solve them. A NoC routing protocol classification is presented in section three organized on three subsections: mono-objective algorithms, two-objectives algorithms and three and four-objectives algorithms. At the end of each subsection, a discussion is given about the characteristics of the algorithms it defines, both proposed solutions and obtained results. A summary of general parameters characterizing the NoC routing algorithms and the most used ones is given on section four. A conclusion giving some perspectives constitutes the last section, where different key research directions are highlighted.

2. Routing issues

Routing problems are diverse and have a negative impact on network performance. The present section details the most important problems that may be encountered during the data sending phase. These problems are listed in the following subsections.

2.1. Deadlock

It is considered as the most difficult problem in NoC routing protocols. It occurs when two or more packets are waiting for a resource to be released by the other(s). A cyclic dependence consequently takes place. Three strategies cope with deadlock: deadlock prevention, deadlock avoidance and deadlock recovery [7].

Several techniques exist to solve the deadlock problem in a NoC for 2D topologies. A trivial solution uses the deterministic routing where a fix path is used by all the data packets sent between each source and destination pair. However, deterministic approaches suffer from the under-utilization of channels [7] and cannot offer alternative paths. This can lead to two major problems in the network: congestion and no fault tolerance (defined in 2.3 and 2.4 respectively), and can also lead to performance decrease [20].

The second possible solution uses virtual channels providing alternative paths avoiding packets to be blocked and / or to block other ones. In this context, Dally and Seitz [21] introduce virtual channels to make the deadlock region acyclic. They show how this cycles absence in channels dependency graph constitutes a necessary and sufficient condition to guarantee deadlock free routing algorithms. This technique is generalized and leads to “Virtual networks” proposed by Jesshope et al. [22].

Glass and Ni [23] adopt another technique called “Turn Model”, which consists of permitting and prohibiting dependencies from one channel to another. In [[24] and [25], the avoidance of deadlock in adaptive routing with wormhole switching is made possible even with the presence of cycles in channel dependency graph. The only requirement is the existence of some subsets of channels defining a connected routing sub-function with an acyclic extended channel dependency graph. Duato [26] extends the latter work by providing a similar proof for virtual cut-through and store-and-forward switching techniques where restrictions required for wormhole switching are removed.

Dally and Aoki [27] introduce the concept of packet wait-for graph and prove deadlock freedom for a routing algorithm with cyclic dependencies by guaranteeing an acyclic packet wait-for graph. Lin et al. [28] prove that deadlock freedom can be reached if none of the channels in the network can be held

Table 1
Techniques used to avoid deadlock problem on NoC.

Solution type	Strategy	Switching technique	Condition type
Deterministic	–	–	–
Virtual channels	Prevention	–	–
CDG	Avoidance	–	Sufficient condition
Turn model	Prevention	Wormhole	–
Extended CDG	Avoidance	Wormhole	Sufficient condition
Acyclic packet wait-for graph	Avoidance	Wormhole	Sufficient condition
Message flow model	Avoidance	Wormhole	Necessary and sufficient condition
CWG	Avoidance	Wormhole	Necessary and sufficient condition
Extended CDG	Avoidance	Virtual cut-through and store-and-forward	Necessary and sufficient condition
Hamiltonian path strategy	–	–	–

forever. Schwiebert and Jayasimha [29] provide a new dependency graph, the Channel Waiting Graph (CWG) and the only restriction imposed for deadlock freedom is the use of local information for routing. In [30], Ebrahimi et al. opt for Hamiltonian path to ensure deadlock freedom in the NoC. However, according to Jackson and Hollis [31], there is no general method proving that a routing algorithm for a dynamically reconfigurable topology is deadlock-free, since the topology can change and channel may be removed or extended. Table 1 summarizes these techniques and their characteristics.

2.2. Livelock

It is the fact that a packet is near its destination without being able to reach it, because other packets hold all the channels that lead to it. This problem generally happens in adaptive routing strategies, and may be removed with several techniques such as minimal path, restricted non-minimal path and probabilistic avoidance [7].

2.3. Congestion

It is caused by the concentration of traffic in a network area producing a slow-down in data communication while other links are free elsewhere. The persistence of the situation can lead to a global congestion, reducing the performance of the network. Congestion usually happens when a deterministic protocol is applied or in the case of non-uniform traffic.

As a solution, many techniques are used. The most common and the most obvious one uses adaptive strategies. This is made possible by mixing different methods. One of the first proposed solution is Q-Learning [32] which is a sort of model-free reinforcement learning. It is able to provide agents with the capability to determine an optimal policy by registering different states during their move through the network. This technique was performed and used in the protocol developed by Ebrahimi and Daneshtalab [19], where routing tables are employed to get network information. To improve global network balance, Gratz et al. [15] propose a new routing policy called “RCA” which gives information about the part of the network that is subject to congestion whether it is local or not.

2.4. Network faults

In NoCs, some failures can take place especially when the network is very active. Failure is considered as a real problem when it causes a malfunction in the global network. There are two types of failures: (i) permanent, they never disappear and are usually due to damaged links; (ii) transient, they may disappear after a short time. To solve this problem, it is important to use [16] fault prevention, fault tolerance, fault removal or fault forecasting.

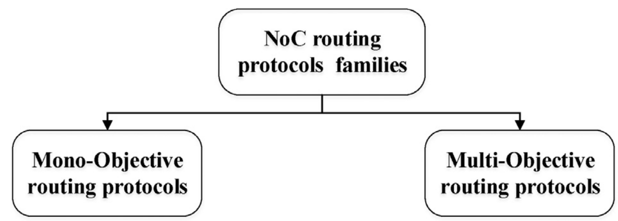

Fig. 2. NoC routing protocols families.

Many fault models exist in literature trying to make easier the fault detection and the fault tolerance. The most popular are: PN (Planar Network) [33], faulty blocs [34], fault rings and fault chain [35], the MCC for 2D mesh [36] and its extension to 3D mesh [37], faulty regions [38] and many other methods where some of them are cited in [39].

3. Routing algorithms classification

Each routing protocol is intended to address one or some of the problems identified in Section 2, in order to improve network performance. The objectives of NoCs routing can thus be expressed as follows:

- **Deadlock freedom** means that the network is not exposed to a risk of deadlock;
- **Livelock freedom** is the case where every packet transmitted in the network will not have to run indefinitely without finding a path to its destination;
- **Congestion-awareness** is the fact that a protocol avoids congestion ;
- **Fault tolerance** means that the protocol is able to get through network failures in order to continue its normal service.

In the following, a NoC routing protocol classification will be presented. It is based on objectives that each algorithm tries to achieve. There are two main families: mono and multi-objective protocols, as it is shown in Fig. 2.

Each family consists of three routing protocols sets according to their topologies: 2D, 3D and irregular/reconfigurable topology.

3.1. Mono-objective routing protocols

In certain proposed approaches, authors have focused on a single problem and have presented their solutions to overcome it. This section outlines this kind of algorithms where four categories could be highlighted: deadlock free protocols, livelock free protocols, congestion-aware protocols and fault tolerant protocols. However, as well as there is no approach that insures only livelock freedom, we will distinguish only three parts as it is shown in Table 2.

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Table 2
Mono-objective routing protocols categories.

Objectives	Deadlock freedom	Congestion-awareness	Fault tolerance
References	[11]	[47]	[52]
	[40]	[48]	[53]
	[41]	[49]	[54]
	[42]	[50]	
	[43]	[51]	
	[44]		
	[45]		
	[46]		

3.1.1. Deadlock free routing protocols

This section describes some routing protocols trying to solve the deadlock problem for 2D and 3D NoC topologies. In the case of 2D architecture, Chiu [11] presents the "Odd-Even", called generally OE, routing protocol. It uses partially adaptive routing without virtual channels and is based on two rules indicating the turns allowed and those prohibited. This decision is taken according to the node location, if it is in odd or even column. As a result, circular wait can never occur, and rightmost column segment of a circular waiting path which is essential for deadlock states can never appear. Hu and Lin [40] propose "SOE" where a central deadlock buffer is used to prevent deadlock situation instead of virtual channels. This gives a better performance in terms of average delay, saturation throughput and adaptiveness than OE . Jing et al. [41] propose "TDM-RA", that is based on two aspects: first, the strategy uses both baker [55] and maze [56] algorithms to allocate resources and determine which one is available for a given process, second, it exploits information about pairs of communicating cores and their time sequence constraints obtained from scheduling and mapping steps in order to avoid deadlock. This combination gives a low latency approach.

For 3D topologies, Ramanujam and Lin [42] propose "RPM" that improves average throughput. It avoids deadlock by using two virtual channels per dimension. "RMF" [43] is an evolution of this work where a better average latency and load balancing is achieved. Ying et al. [44], create "SBSM" and "DBSM" routing algorithms taking into account topology and routing. They use virtual channels and the Manhattan Distance. Lee and Choi [45] propose "Redelf" which is based on layered mesh network. What authors call "up-pivot" and "down-pivot" are introduced to make the transition between different layers following some rules. The idea is to modify "elevator-first" algorithm (described in Subsection 3.2.1) without using virtual channels to insure deadlock freedom. Obtained results show a low power consumption and high performance. Chao et al. [46] use a turn model to avoid deadlock in their algorithm named "VDLAPR". From Table 3 we can see that each routing protocol presented in the Subsection 3.1.1 brings a new method to avoid deadlock. Moreover, most of them use the wormhole switching technique without necessarily using virtual channels.

3.1.2. Congestion-aware routing protocols

To avoid congestion in networks on chip, Ebrahimi et al. [47] propose "HARAQ", an algorithm based on Q-learning and using one virtual channel in the Y dimension. The use of a learning model allows latency estimation from each output channel to destination and then avoiding congested ones. This method offers scalability and high adaptability. Farahnakian et al. [48] use Q-Routing [57] in "DuQAR" routing algorithm. It aims at reducing the congestion in the network by sending packets through a path that has the shortest Q-Value. The particularity of this algorithm is that, in order to avoid global congestion, it does not update frequently the Q-Value but it is done only if the average number of free buffers in the routers is greater than a minimum threshold.

Kuo et al. [49] introduce the concept of path diversity in their two routing algorithms "PDA" and "A-PDA". They define the notion of normalized path diversity (NPD) and use a reduced NPD table to store routing information. In [51], Silva Junior et al. use ACO (Ant Colony Optimization) and propose two routing protocols based on "Elitist Ant System" and "Ant Colony System", respectively named "REAS" and "RACS". In both algorithms, several colonies are used with interdependence between them to allow a simultaneous packet sending and to minimize transmission latency.

Silva Junior et al. [50] adapt the "REAS" protocol on 3D architecture to solve congestion problem on 3D topology.

Table 4 summarizes all methods defined in the Subsection 3.1.2. It is clearly observed that adaptive routing is the most used technique associated with Q-learning or metaheuristics to get around congested zones.

3.1.3. Fault tolerant routing protocols

Some routing protocols aim at solving the problem of failures in networks on chips with different methods. Among them, Chen and Chiu [52] present a "Message-Route" algorithm that is able to tolerate any number of faults. A method based on given rules is used to guide the direction of messages when they encounter rectangular faulty regions constructed by deactivating some non-faulty nodes. The deadlock freedom of this algorithm is proved in the same work. However, Holsmark and Kumar [58] provide a counterexample showing that it is not deadlock free. In [53], "SPSR" is developed to avoid broken links in the NoC. The method consists of two phases: first, searching a Manhattan Route between source and destination without broken links. If no such route exists, the second step called "deflection route detection" is triggered in order to overcome at least one faulty link. The advantage of this algorithm is that it reduces power consumption and offers low latency due to the use of only two bits to record hops.

Other methods propose fault-tolerance solutions by using a 3D topology, such as a "3D-FT" algorithm developed by Ebrahimi et al. [[54]. This work supports two kinds of failures: router and link failures. The protocol promotes shortest paths to overcome routers failures. If there is no choice, it applies a modification on routers architecture in order to avoid re-routing and increasing latency. However, in the case of link failures, it uses non-minimal paths if no shortest failure-free path is available.

These strategies are listed in Table 5 where additional characteristics are given. Number of failures supported by each protocol, and their types are also specified.

3.1.4. Discussion

The main challenge behind interesting on NoC routing problems is to increase the reliability of the network while ensuring a sensible performance. The main evaluated performances are: low latency, high throughput and low power consumption. However, many papers present experiments evaluating other metrics as it is shown in Section 4.6. Existing work show that for each problem, several ways can be used to solve it trying at each time to get better results.

Against this background, this section bundles a set of algorithms treating one NoC routing objective at a time. These approaches present the recent proposed methods to avoid a given routing problem (deadlock, congestion, failures) or to improve the performance already obtained by previous algorithms.

The analysis of these protocols reveals that in overall, each family evaluates the metric directly related to the studied objective. So, the deadlock free strategies are evaluated according to their average throughput under different traffic patterns, whereas in the

Table 3
Deadlock free NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Network	Path length	Based on	Virtual channel
Odd-Even	[11]	2000	Partially adaptive	Wormhole	2D	–	–	Turn Model	No
SOE	[40]	2012	Adaptive	Wormhole	2D	Static	–	OE	No
TDM-RA	[41]	2013	–	TDM[1]	2D	Static	–	Banker & Maze	No
RPM	[42]	2008	Oblivious	Wormhole	3D	Static	Partially Minimal	/	Yes
RMF	[43]	2012	Oblivious	Wormhole	3D	Static	Partially Minimal	–	Yes
SBSM/DBSM	[44]	2012	–	Wormhole	3D	Static	–	–	Yes
Redelf	[45]	2013	–	Wormhole	3D	Static	–	Elevator-First	No
VDLAPR	[46]	2013	Adaptive	Wormhole	3D	Static	–	Turn Model	No

[1] TDM: Time Division Multiplexer

Table 4
Congestion-aware NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Network	Path length	Based on	Virtual channel
HARAQ	[47]	2012	Adaptive	Wormhole	2D	Direct	Minimal & Non Minimal	Q-Learning	Yes
DuQAR	[48]	2012	Adaptive	Wormhole	2D	Static	–	Q-Routing	Yes
PDA/A-PDA	[49]	2012	Partially Adaptive	Wormhole	2D	Static	–	–	No
RCAS	[50]	2013	Adaptive	Wormhole	2D	Static	–	ACO (ACS)	No
REAS	[51] [50]	2013	Adaptive	Wormhole	2D/3D	Static	–	ACO (EAS)	No

Table 5
Fault tolerant NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Failure type/number	Path length	Based on	Virtual channel
Message Route	[52] [58]	1998	–	Wormhole	2D	Any number of faults	–	–	No
SPSR	[53]	2012	Source	Wormhole	2D	Any number of broken links	–	–	No
3D-FT	[54]	2013	Fully Adaptive	Wormhole	3D	Routers & Links Failures	Minimal & Non Minimal	–	Yes

congestion-aware and fault tolerant protocols, the latency seems to be the most evaluated parameter. Moreover, since most of the fault tolerant and congestion-aware protocols are adaptive, some papers evaluate also the power consumption and sometimes the obtained reliability.

It is also identified that most of comparisons are done with XY (defined in Section 3.2.1) since it is the reference protocol thanks to its easy implementation and high reliability in uniform traffic (considered as the most used in experiments according to the study presented in Section 4.5).

Actually, these observations are valid for all the protocols classified in different categories of the present survey.

To take advantage from these multiple ideas and those that are less recent, many researches mix them in order to obtain protocols solving more than one objective simultaneously, as it is presented in the following section 3.2 and 3.3.

3.2. Two-objectives routing protocols

This section includes a number of routing algorithms that have been proposed in the literature and that satisfy two objectives at a time (Table 6).

Table 6
Categories of Two-objectives NoC routing protocol.

Objectives \ Nb objectives	2 objectives				
Deadlock free	x	x	x		
Livelock free	x			x	x
Congestion-aware		x		x	
Fault tolerant			x		x
References	[23] [59] [60] [7] [61] [62] [63] [64] [65] [31] [20] [66] [67] [68]	[69] [70] [71] [72]	[4] [73] [74] [75] [76] [77] [78] [79] [80] [33]	[81] [82] [83] [84]	[85] [86]

3.2.1. Deadlock free and livelock free routing protocols

In the literature, many routing algorithms have tackled the both issues of deadlock and livelock in NoC. For 2D architectures, one of the first routing protocol developed is called XY. It is the most popular because of its easy implementation. XY is a deterministic protocol and its CDG (Channel Dependency Graph) is acyclic. This is why it is a deadlock free and livelock free routing protocol.

The “Turn model” idea is initially proposed by Glass and Ni [23] for non-dimensional meshes in order to solve the deadlock problem in networks. Its main characteristic is that it prohibits at least one turn in each of the many possible cycles in the network in order to prevent deadlock. It maintains a path between every pair of nodes and prohibits the minimum number of turn. Further, in turn model, the number of channels is finite what allows packets to reach their destinations after a limited number of hops, avoiding the livelock. Three versions of this protocol are proposed: “West-First” routing, “North-last” routing and “Negative-first” routing. Schwiebert and Jayasimha [59] opt for a fully adaptive approach in “Opt-y routing” and use virtual channels. They set the minimum number of virtual channels to 4n-2, from a total of nD mesh network. In 2D mesh topology, the algorithm requires a

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minimum of six virtual channels located at different turns. “Opt-y routing” is minimal, then it is also livelock free.

Seo et al. [60] develop an oblivious routing algorithm “O1TURN”, using two Virtual channels to avoid deadlock, and minimal paths to avoid livelock.

Based on XY and using deterministic routing with two virtual channels, Atagoziyev [7] proposes another protocol to avoid deadlock and livelock in NoCs called “XY-YX”. “IX/Y” is a deadlock free and livelock free routing algorithm proposed by Shafiee et al. [61], that has a similar principle with XY. Its advantage is that it improves traffic load balancing.

In [62], Ghosal et al. present “DiaMOT” routing protocol for a multilevel architecture. It extends XY to support a new architecture while ensuring deadlock freedom by proving that there is no cycle dependency.

Sebastian and Sharma [63] propose the “pure zigzag” algorithm as a new routing approach. It is deterministic and minimal, guaranteeing that the network is respectively deadlock free and livelock free. “MILP”, proposed by Bhardwaj et al. [64], uses a turn prohibition model [87] to simultaneously avoid deadlock and livelock.

For reconfigurable networks, Fu et al. [65] propose a deadlock free and livelock free method called “Abacus Turn Model” (AbTM). It guarantees that the network is deadlock free by applying the same rule as odd-even routing algorithm which consists in the fact that “a network is deadlock-free if both clockwise and counter-clockwise rightmost columns are removed from the network”. Moreover, it proves that the algorithm is livelock free since there is no drop and suspend packets during reconfiguration. There are two routing algorithms based on this method that inherit its properties: “Tug-war” and “Arm-wresling”. Both algorithms get good performances under non uniform traffic and reduce packets latency for all applications. Jackson and Hollis [31] propose a minimal routing protocol called “Opt-Bypass”,which is livelock free. The protocol achieves also the deadlock freedom objective by using one extra virtual channel and tighter constraints on the permitted turns. So, only the turns used in west-first routing algorithm are authorized. Kiasari et al. [20] propose “LAR” framework to enhance average latency in reconfigurable networks by prohibiting unnecessary turns and guaranteeing no cycle in CDG to ensure deadlock and livelock freedom.

For 3D topology, “LA-XYZ” is described by Ben Ahmed and Ben Abdallah [66] as a deadlock free and a livelock free routing algorithm since it is based on XYZ. Its main objectives are reducing latency and power consumption while enhancing throughput. Dahir et al. [67] resolve deadlock and livelock problems by extending the Turn Model and using Odd-even as basis for the algorithm called “HADR3D”. Dubois et al.[68] present “Elevator-First” which is a routing algorithm for irregular 3D topology solving deadlock and livelock problems by the use of two virtual channels.

More details about properties of each of those protocols and their environment are given in Table 7. We can see that they all use the wormhole technique switching, the majority of them take only the minimal paths and do not use virtual channels which reduces the use of buffer space.

3.2.2. Deadlock free and congestion-aware routing protocols

In order to avoid congestion in a NoC while maintaining it deadlock free, Su et al. [69] use ACO and propose “ACO-DAR” where deadlock is considered as an obstacle to be avoided by using ant packets ensuring at the same time congestion avoidance.

As solutions with 3D topology, Chen et al. [70] introduce the “TTABR” algorithm which aims to balance both traffic and temperature in the NoC by offering an alternative path beyond a congested region to get around it and without causing deadlock. This technique improves network throughput. In [71], “DyXYZ” is presented as a solution to solve, first, the congestion problem in the NoC (by using the neighboring nodes congestion information to make a transmission decision at a current node), and second, the deadlock problem by using 4, 4, and 2 virtual channels respectively along the X, Y, and Z dimension. Chen et al. [72] present “TAAR” discussing a routing method with a 3D mesh topology. The method consists of updating the topology table at each topology change. It thus protects packets from being blocked in the congested nodes. “TAAR” prevents deadlock by setting the depth of buffer queues at the packet size.

Table 8 gathers these approaches and specifies some additional characteristics. Once again, it can be observed that adaptive strategy is the one used to cope with congestion.

3.2.3. Deadlock free and fault tolerant routing protocols

This category gathers routing protocols satisfying deadlock avoidance and fault tolerance objectives. In [4], virtual channels are used to avoid deadlock in the “Node Labeling Technique” where labels are affected to nodes according to their situation. Healthy, unsafe, deactivated and faulty nodes are used in faulty region playing each one its role to ensure fault tolerance. Patooghy and Miremadi [73] introduce “XYX” deadlock free routing algorithm which is based on XY. It insures 60% of fault tolerance by sending a copy of each packet through a different path and then adopting error detection technique at destinations.

Zou and Pasricha [74] propose “NARCO”, which is based on OE turn model combined with packet replication to ensure fault tolerance, and uses two VCs to avoid deadlock. Chaix et al. [75] propose a deadlock free and fault tolerant technique making use of two virtual networks. Their method consists on sending periodically an IAM (I am Alive Message) from each node to detect failures. Based on the same architecture, Chaix et al. [76] develop “EPR” where four virtual channels are added and prohibited turns are used to avoid deadlock.

Similarly, in order to avoid faulty links, Yancang et al. [77] introduce a new model called “PR-WF” to extend turn model and ensure fault tolerance and deadlock freedom. This strategy uses three hierarchy buffers inside each node: a buffer in the router port, a pseudo-receiving (PR) buffer in network interface and the local IP cache. This method avoids prohibited turns caused by west-first algorithm and increases the number of links in the network.

In the case of irregular and/or reconfigurable topologies, Zhang et al. [78] propose a reconfigurable routing algorithm “RRA”, based on very low cost configuration represented by a 4-bits register to solve any faulty router topology. Moreover, its CDG (Channel Dependency Graph) is acyclic and thus deadlock free. Jovanovic et al. [79] propose “MPA” that is able to support faulty regions which are not necessary rectangular. The algorithm is also deadlock free because it is based on turn model. Another more simple protocol is shown in [80] called “TRAIN” where mesh topology is transformed into a tree to take benefit of resulting shortcuts. The algorithm guarantees fault tolerance by isolating faulty routers and links when detected, forming a sub network of non-faulty components. It also uses virtual cut-through switching technique to avoid deadlock.

Among algorithms using 3D topology, “iPAR” protocol developed by Xiang et al. [33] uses two virtual channels to avoid deadlock. It is based on a new faulty model called Planar Network (PN) [33] to collect fault information at each plan of the NoC and then, ensure tolerance of multiple number of faulty nodes.

A summary of all the algorithms defined in Subsection 3.2.3 are presented in Table 9. It also includes information about their path definition strategies, their switching techniques, the number of failures they support, and if they are using virtual channels or not.

Table 7
Deadlock free and livelock free NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Network	Path length	Based on	Virtual channel
XY	–	–	Deterministic	Wormhole	2D	Direct	Minimal	–	No
Turn Model	[23]	1992	Partially adaptive	Wormhole	2D	Static	Minimal & Non Minimal	–	No
			Fully adaptive						Yes
West-First	[23]	1992	Partially adaptive	Wormhole	2D	Static	Minimal & Non Minimal	Turn Model	No
North Last	[23]	1992	Partially adaptive	Wormhole	2D	Static	–	Turn Model	No
Negative First	[23]	1992	Adaptive	Wormhole	2D	Static	Minimal	Turn Model	No
Opt-y routing	[59]	1993	Fully adaptive	Wormhole	2D	–	Minimal	–	Yes
O1TURN	[60]	2005	Oblivious	Wormhole	2D	Static	Minimal	–	Yes
XY-YX	[7]	2007	Deterministic	Wormhole	2D	Direct	Minimal	XY	Yes
IX/Y	[61]	2008	Deterministic	Wormhole	2D	Direct	Minimal	XY	No
DiaMOT	[62]	2012	Deterministic	–	Hierarchical 2D	Static	–	XY	No
The pure Zigzag	[63]	2012	Deterministic	Wormhole	2D	Static	Minimal	–	No
MILP	[64]	2012	Oblivious	Wormhole	2D	–	–	–	No
AbTM	[65]	2011	Adaptive	Wormhole	2D	Reconfigurable	Minimal	Odd-Even	No
Arm-Wrestling	[65]	2011	Adaptive	Wormhole	2D	Reconfigurable	Minimal	AbTM	No
Tug-War	[65]	2011	Adaptive	Wormhole	2D	Reconfigurable	Minimal	AbTM	No
Opt-Bypass	[31]	2011	Fully Adaptive	Wormhole	Irregular	Reconfigurable	Minimal	Opt-y	Yes
LAR	[20]	2014	Deterministic	Wormhole	2D	Reconfigurable	Minimal & Non Minimal	–	No
LA-XYZ	[66]	2012	Deterministic	Wormhole	3D	Static	Minimal	XYZ	No
HADR3D	[67]	2013	Partially Adaptive	Wormhole	3D	Static	Minimal	Odd-Even Turn Model	No
Elevator-First	[[68]	2013	Distributed	Wormhole	Irregular 3D	Static	–	–	Yes

Table 8
Deadlock free and congestion-aware NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Network	Path length	Based on	Virtual channel
ACO-DAR	[69]	2012	Fully Adaptive	Wormhole	2D	Static	Minial & Non Minimal	ACO	No
TTABR	[70]	2013	Adaptive	Wormhole	Regular & Irregular 3D	–	Minimal & Non minimal	–	No
DyXYZ	[71]	2013	Fully Adaptive	Wormhole	3D	Static	–	–	Yes
TAAR	[72]	2013	Adaptive	Wormhole	Irregular 3D	–	Minimal & Non Minimal	–	No

3.2.4. Congestion-aware and livelock free routing protocols

To avoid congestion and livelock at the same time, Chang et al. [81] propose a low latency and a high throughput routing algorithm called “ACO-CAR” which is inspired from ACO to perform load balancing. It uses table-reformed technique to store information and eliminate redundant ones. This may cause the loss of information at destination node. That is why an intermediate destination is proposed as a cascaded point through which packets pass before reaching their final destinations. Similarly, in order to reduce entries number of the routing table used in ACO, Hsin et al. [82] use regions in their protocol named “RACO”.

The idea of Q-learning is adopted by Farahnakian et al. [83] for what they call “Bi-LCQ” routing algorithm. It uses two virtual channels and is based on CQ-Table (Cluster Q-table) where local and global congestion information about alternative routes are stored. Each cluster selects the less congested output channel. The protocol presents significant performance improvement. It reduces latency and area. Hsin et al. [84] introduce a strategy named “ACO-BANT” with a backward-ant mechanism and odd-even algorithm to solve the congestion problem and improve network performance.

The four algorithms defined in this section use minimal path, as it is shown in Table 10, therefore they are all livelock free.

3.2.5. Fault tolerant and livelock free routing protocols

To deal with link/router failures, Ali et al. [85] propose “NoC-LS” algorithm where routing tables are used in conjunction with a link state technique to minimize updates. It generates a dynamic routing and scalable approach whereas its paths are minimal. Ebrahimi et al. [86] present a simpler method called “MiCoF” witch is based on the shortest path. When a router failure is detected, packets take an alternative minimal path already foreseen in the architecture, maintaining hence a good performance in the network.

More characteristics of the both algorithms are defined in the Table 11.

3.2.6. Discussion

Approaches surveyed in this section bring solutions for two NoC routing problems among the four defined in Section 2. So, we have listed several algorithms divided into five categories.They concern different NoC architectures, regular mesh 2D, mesh 3D, reconfigurable networks and irregular topologies.

Naturally, each of them proposes a new idea but they share a couple of properties like the use of wormhole switching technique by almost of them to reduce the buffer space consumption.

We have also remarked that most of the deadlock free and livelock free algorithms are either the improvement or the modification of the two popular algorithms XY and Turn model. This is due to their easy implementation while maintaining high reliability.

As per Section 3.1, metaheuristics and learning methods are again used to avoid congested regions generating paths adaptively. Besides, the adaptive strategy is not only predominant in the congestion-aware algorithms but also in the fault tolerant ones.

In addition, some techniques employed to avoid congestion are not exploited to prevent or avoid other routing problems. For instance, Q-learning technique is frequently used to detect congested

Table 9
Deadlock free and fault-tolerant NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology/ Network	Failure type/number	Path length	Based on	Virtual channel
Node Labeling Technique	[4]	1995	Fully Adaptive	Wormhole	2D	Any number of link/router faults	Non Minimal	–	Yes
XYX	[73]	2009	-	Wormhole	2D	crosstalk,single event upset, electromagnetic interference, power supply disturbance	-	XY	Yes
NARCO	[74]	2010	Adaptive	Wormhole	2D	Permanent faults	Priority to Minimal	OE	Yes
EPR	[75] [76]	2010 - 2011	Adaptive	Wormhole	2D	Any set of multiple nodes and links failure	–	–	Yes
PR-WF	[77]	2011	–	Wormhole	2D	Permanent faulty links	Non Minimal	West First	No
RRA	[78]	2008	–	–	Reconfigurable 2D	Any one-faulty-router topology	–	–	–
MPA	[79]	2009	Partially Adaptive	Wormhole	Reconfigurable 2D	Faulty nodes and regions	–	Turn Model & XY	No
TRAIN	[80]	2010	–	Virtual cut-through	Irregular	Links and routers failures	–	–	No
iPAR	[33]	2009	Adaptive	Wormhole	3D	Many faulty nodes	Minimal / Non Minimal	PAR	Yes

Table 10
Congestion-aware and livelock free NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Network	Path length	Based on	Virtual channel
ACO-CAR	[81]	2010	Adaptive	Wormhole	2D	Static	Minimal	ACO	No
RACO	[82]	2010	–	Wormhole	2D	Static	Minimal	ACO	No
Bi-LCQ	[83]	2013	Adaptive	Wormhole	2D	Direct	Minimal	Q-Learning	Yes
ACO-BANT	[84]	2013	Adaptive	Wormhole	2D	–	Minimal	Odd-Even & ACO	No

Table 11
Fault tolerant and livelock free NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Failure type/number	Path length	Based on	Virtual channel
NoC-LS	[85]	2005	–	–	2D	Link/Router failures	Minimal	Link State Routing	No
MiCoF	[86]	2013	Fully Adaptive	Wormhole	2D	6 router faults / 8X8	Minimal	–	Yes

areas without taking advantage of it to collect information about faulty links/routers in order to avoid them. Similarly, routing tables are used in some solutions to avoid the congested zones and in others to detect failures, but they are rarely used to meet simultaneously the two objectives, even if the necessary information is already present within these routing tables. Techniques capitalizing on Q-value to get information about neighbors congestion could be also exploited to avoid deadlock.

However, the latter observation is valid only for protocols defined in this section and some of the ideas proposed in the present discussion are already developed as algorithms meeting more than two objectives defined in the Section 3.3.

3.3. Three and four-objectives routing protocols

In this section, routing protocols focused on achieving three and four objectives are detailed. Their references are gathered in Table 12 ordered according the number of objectives they achieve.

3.3.1. Deadlock free, livelock free and congestion-aware routing protocols

The first protocol in this category is “PFNF” that was developed by Upadhyay et al. [88] where a NoC is divided into two virtual networks. Messages are routed in the first one according to positive-first algorithm, and in the second one according to negative-first algorithm, this offers a uniform distribution of the

Table 12
Categories of three and four-objectives NoC routing protocol.

Objectives \ Nb objectives	3 objectives			4 objectives
Deadlock free	x	x	x	x
Livelock free	x	x		x
Congestion-aware	x		x	x
Fault tolerant		x	x	x
References	[88] [89] [90] [91] [92] [93] [94] [95] [96] [97] [98] [30]	[23] [99] [100] [101] [102] [103] [104] [6] [105] [106] [107] [108] [109] [110] [111] [112] [113] [114] [115] [116] [[54]	[117] [118] [119] [120] [121] [122]	[123] [124] [125]

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load through the network and good performance in terms of average latency and throughput. Moreover, the protocol ensures deadlock freedom because Duatos theorem is verified and livelock freedom since it is minimal. The "DyAD" routing protocol presented by Jingcao and Marculescu [89] combines both deterministic and adaptive routing to avoid congestion. The algorithm is associated with OE. "DyAD-OE" is deadlock free and livelock free. In "DyXY" [90], a stress value is used to estimate a less congested short path for transmitting packets. Consequently, using only short paths resolves deadlock and livelock problems.

In [91], an ACO based routing algorithm, called "AntNet", is presented. It uses control packets playing the role of ants to update routing tables based on network traffic status. It is considered deadlock free and livelock free because of its minimality. Nickray et al. [92] propose "Adaptive XY" routing which is an adaptive version of XY. It avoids congestion by using agent collaboration to share network congestion information as soon as the packet is submitted to transmission. To remove deadlock, a buffer space and an extra control logic for buffer are added. However, to avoid livelock some rules are established.

Huang and Hwang [93] present "Adaptive congestion aware" protocol. It uses information about neighbors buffers called buffers utilities. In order to avoid any problem of deadlock and/or livelock, it employs OE Turn model.

Puthal et al. [94] propose "C-Routing" algorithm to save space. It enhances Q-Routing [57] by integrating the cluster notion. Instead of storing a full routing table (which containing information about all the NoC) on each node, C-Routing stores only a small one with global information of inter cluster communication costs. Furthermore, it mixes deterministic mode with partially adaptiveness when necessary and uses XY in some turns (north direction) to avoid deadlock and livelock.

Based on Mad-y [126] and offering the maximal adaptiveness, "LEAR" developed by Ebrahimi et al. [95] is based on the packet deflection to avoid congested areas. A network CDG is proved acyclic guaranteeing deadlock freedom. In "LEAR", the number of hops is limited to ensure livelock freedom.

Ramakrishna et al. [96] present "GCA" where a new field is added in the header flit and used both to store congestion information and to update its own information about the global congestion state. In this work, VCs are used to avoid deadlock and minimality to avoid livelock.

Mak et al. [97] develop a routing algorithm for dynamic networks. They solve the problem of the large size of routing tables (caused by some techniques like Q-Routing [57]) by proposing "KSLA" strategy. The storage of routing decisions for all the destinations is replaced by the computation of routing decisions for nodes that are k-step away from the current node. An optimal decision is then made according to the fact that the destination is within a k-step region or not. To avoid deadlock, "KSLA" makes use of west-first turn model algorithm. As a solution on 3D architecture, "3D Deflection" [98] gets rid of buffers with minimal performance loss. It is based on a bufferless router in order to balance the utilization of inter-layer traffic. "3D Deflection" uses TSV ejection / injection scheme to avoid livelock and deadlock because no flits are ever stuck or waiting for other resources. "MAR" [30] uses recursive portioning to solve the congestion problem, Hamiltonian path to avoid deadlock and minimality to avoid livelock. This approach improves the average latency in the network.

Table 13 presents a full list of algorithms described in Subsection 3.3.1. It gives additional functional details that show a diversity of strategies used to achieve same objectives.

3.3.2. Deadlock free, livelock free and fault tolerant routing protocols

This category exposes routing protocols guaranteeing deadlock and livelock freedom as well as fault tolerance.

"Negative-First" [23] is one of the first algorithms proposed in this category, it is based on the turn model where negative directions are prohibited. This makes it deadlock free and livelock free. It supports both minimal and non-minimal paths and is fault tolerant in its non-minimal version.

Park et al. [99] extend e-cube [35] algorithm and propose two other protocols "F4" and "F3". They are based on fault-ring (f-ring) model to reduce the number of components that should be made faulty. The same idea of block fault model is employed in three other algorithms "Source-Directed routing", "Destination-Directed routing" and "Mixed-approach routing" [100] based on limited fault information, on virtual network to avoid deadlock and on minimal paths to guarantee livelock freedom.

In "Extended XY" [101], the block fault model is used to route packets around faulty regions while taking into consideration prohibited turns. Because it is based on OE, it ensures deadlock freedom. For livelock freedom, it is proved that "Extended XY" can deliver packets from a source to a destination regardless of the number and location of the faults. This protocol was reused in [102] and gave birth to "Extended XY/ Extended MCC".

Fick et al. [103] propose a deterministic fault tolerant routing algorithm named "BRS". It is based on the reconfiguration of the routing tables located at each router, transporting information regarding the links validity. This is done by respecting a number of rules. This technique contributes also to avoid deadlock.

Feng et al. [104] present "FTDR" and "FTDR-H" using Q-learning and reducing the number of routing table entries. Both protocols collect information about faulty links and update the routing table while choosing each time the shortest path. "FTDR" and "FTDR-H" are deadlock free because packets never wait in switches, and livelock free by limiting misrouting.

Yongqing et al. [6] present "ADBR" which is an algorithm avoiding faulty links in the NoC by using one or several intermediate nodes between each pair source - destination. The number of intermediate nodes is computed according to fixed rules. The algorithm guarantees also a deadlock freedom, by adopting a new flow control technique called "DBFC" [6], and livelock freedom by using minimal paths.

Xiangming et al. [105] combine XY with YX and develop a protocol called "RRPID" which is deadlock and livelock free. The principle of this routing algorithm is based on the creation of redundant packets and transmitting them through two different non-intersecting paths. This guarantees their good deliverance despite the presence of transient faults. Obviously, "RRPID" uses control mechanism to check the two packets at the destination node. For Vitkovskiy et al. [106], faulty links could be bypassed by re-routing packets in a U-shaped path around faulty regions. This idea is illustrated in "FTLR" routing protocol which deals with deadlock and livelock by using two virtual channels.

Chen and Cotofana [107], in "OFLT", use the message and signal exchange to detect faulty routers and decide the links to isolate before looking for another path around the faulty links. In "OFLT", the use of some basic conditions guarantees livelock avoidance, and VCs eliminate deadlock.

In order to distinguish link fault from channel fault, Zhang et al. [108] propose a very fine-grained routing algorithm named "VFFRA-BR", using buffer reuse to tolerate faults, OE turn model to avoid deadlock and minimal paths to avoid livelock. Recently, "ZoneDefense" routing [109] is proposed, based on defense zone fault model, which is the detection of different faults as long as they are planned before the launch of routing process. "ZoneDefense" is minimal and its network CDG is acyclic, what make it respectively livelock free and deadlock free.

Behrouz et al. [110] propose "FaulToleReR" routing protocol based on two phases. The first one consists of looking for the set of available paths in the network including faults. The second one

Table 13
Deadlock free, livelock free and congestion-aware NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Network	Path length	Based on	Virtual channel
PFNF	[88]	1997	Fully Adaptive	Wormhole	2D	Static	Minimal	–	Yes
DyAD / DyAD-OE	[89]	2004	Deterministic & Adaptive	Wormhole	2D	Static	Non minimal	Odd-Even	No
DyXY	[90]	2006	Fully Adaptive	–	2D	Static	Minimal	XY	Yes
AntNet	[91]	2006	Adaptive	Wormhole	2D	Static	Minimal	ACO	No
Adaptive XY	[92]	2009	Adaptive & Deterministic	–	2D	Static	–	XY	No
Adaptive congestion aware	[93]	2009	Adaptive	–	2D	Static	Minimal / Non Minimal	Odd-Even/Turn Model	No
C-Routing	[94]	2011	Partially Adaptive & Deterministic	Wormhole	2D	Static	Non Minimal	–	Yes
LEAR	[95]	2012	Adaptive	Wormhole	2D	Static	Minimal / Non Minimal	Mad-Y	Yes
GCA	[96]	2013	Partially Adaptive	Wormhole	2D	Static	Minimal	–	Yes
KSLA	[97]	2011	Adaptive	Wormhole	2D	Dynamic	Minimal	DP	No
3D Deflection	[98]	2013	Adaptive	Wormhole	3D	Static	Non minimal	Bufferless router	Yes
MAR	[30]	2014	Partially Adaptive	Wormhole	3D	Static	Minimal	–	No

selects those to use between each source and destination nodes, taking into consideration the information stored in routing tables and the importance of guaranteeing the deadlock freedom. With “FaulToleReR”, the network is always connected. The problem of livelock is thus avoided.

In [134], Zhang et al. present a new mechanism called “DMT” which is able to deliver packets over different output channels using non-minimal paths. Thanks to this, “DMT” ignores detected faults and avoids deadlock and livelock.

In the case of reconfigurable networks, “BRS” [103] is used as a base to develop a new fault tolerant, deadlock free and livelock free routing protocol called “VICIS” [111]. It is associated to a new routing architecture which is reconfigured whenever necessary. Kumar et al. [112] propose a deterministic routing protocol for irregular topologies called “M-LBDR”. The algorithm uses routing and connectivity bits between routers and links to detect faulty links and then re-configure the topology by computing new next hops. “M-LBDR” does not use routing tables and it is based on turn model to avoid deadlock. Huang et al. [135] design a new reconfigurable router and develop the “TARRA” routing algorithm to keep the NoC connected despite of the presence of intermediate routers under test. To ensure deadlock freedom and livelock freedom, sub-networks are used and channel assignment rules are applied to prevent packets to switch from one subnetwork to another which is already visited.

Some solutions are applied on 3D topology such as “4NP-First” where Pasricha and Zou [113] combine two algorithms based on turn model and adapted for 3D architecture: 4N-First and 4P-First. They avoid fault by introducing some turn restriction checks. Since “4NP-First” is based on 3D turn model, it is deadlock free and livelock free. Feng et al. [114] present “Deflection Routing” which uses layer routing tables instead of global routing tables. This allows to perform routing first on the same layer, then across layers. The algorithm is deadlock free because it never leaves packets waiting on switches, and it is livelock free because it limits the number of misrouting. “AFRA” [115] uses a deterministic mode to avoid faulty vertical links. It executes ZXY in the case of no faulty path, and XZXY otherwise. This makes it deadlock free and livelock free. “HamFa” [116] modifies Hamiltonian path strategy to allow more efficiency in fault tolerance and ensure deadlock and livelock freedom. Finally, “3DFAR”[54] creates sub-networks to facilitate distribution of fault information in the network while maintaining the NoC deadlock free and livelock free.

According to Table 14 which lists the protocols detailed in Subsection 3.3.2, it is noticed that these protocols use certainly complex strategies to meet three goals at a time, but succeed in avoiding an unlimited number of faults better than those developed specially to be fault tolerant.

3.3.3. Deadlock free, congestion-aware and fault tolerant routing protocols

This category includes NoC routing protocols that satisfy simultaneously deadlock avoidance, congestion avoidance and fault tolerance. In this context, Valinataj et al. [117] propose “RAFT” where congestion information are collected and the path with the smaller congestion factor is selected. Two VCs are used to avoid deadlock. To guarantee fault tolerance, the algorithm maintains configuration register to check whether the path contains faulty links/router or not.

“MAFA” [118] develops its degree of adaptiveness to route packets through shortest path in spite of the presence of faulty links. Path selection is based on congestion value parameter, then on turn model and VCs to avoid deadlock.

“HipFar” presented by Ebrahimi et al. [119] has the particularity to ensure high network performance while being fault tolerant, congestion-aware and deadlock free. It is based on turn model and congestion information in the process of fault tolerance. Moreover, by allowing two additional turns, “HipFar” appears to be deadlock free.

Lin et al. [120] present an approach based on ACO, called “ACO-FAR”. It is composed of three steps corresponding to: propagating fault information over the network, searching for all possible existing paths except those containing faulty links and finally, selecting the best path free of faulty nodes and avoiding congestion around faulty region. As per ACO-DAR, “ACO-FAR” uses ant packets to avoid deadlock by considering it as an obstacle.

“FTA-ASN”, proposed by Khoroush and Reshadi [121], is also an approach favoring minimal paths with least congestion. This is done by the use of routing tables, when possible, where deadlock is avoided and faults are detected. In fact, the absence of minimal path between two nodes reveals the presence of faulty links.

“RR-2D” [122] rises the idea maintaining packets adaptivity as long as possible. This is done by selecting the next hop according to the number of alternative paths. “RR-2D” ensures fault tolerance and congestion avoidance by observing fault and congestion information respectively. It is proved that no cycle is formed with this method, and “RR-2D” is thus deadlock free.

For 3D topologies, Ebrahimi proposes “RR-3D” [122] which is similar to the previously presented RR-2D protocol with some modification in the communication inter-layers. Salamat et al. [136] address the problem of partially connected 3D-NoC by presenting the “ETW” routing algorithm which allows intermediate

Table 14
Deadlock free, livelock free and fault tolerant NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Failure type/number	Path length	Based on	Virtual channel
Negative First	[23]	1992	Partially adaptive	Wormhole	2D	–	Minimal / Non Minimal	Turn Model	No
F4	[99]	2000	Adaptive	Wormhole	2D	Any number of faults	–	e-cube	Yes
F3	[99]	2000	Adaptive	Wormhole	2D	Any number of faults	–	e-cube	Yes
SDR, DDR, Mixed-Approach Routing	[100]	2000	Adaptive	–	2D	Important number of faults	Minimal	–	Yes
Extended-XY	[101]	2003	Deterministic	Wormhole	2D	Any number of faults	–	XY & OE	No
Extended XY/Extended MCC	[102]	2005	Deterministic	Wormhole	2D	Any number of faults	–	Extended XY	No
BRS	[103]	2009	Deterministic	Wormhole	2D	Any number of link failures	–	Turn Model	No
FTDR & FTDR-H	[104]	2010	Adaptive	–	2D	Faulty links	Minimal	Q-learning	No
ADBR	[6]	2011	Fully Adaptive	Virtual cut-through	2D	Faulty links	Minimal	–	No
RRPID	[105]	2012	–	Wormhole	2D	Transient faults	–	XY & YX	Yes
FTLR	[106]	2012	Adaptive	Wormhole	2D	Faulty links	Minimal	–	Yes
OFLT	[107]	2013	–	Wormhole	2D	Any number of faults	Minimal	–	Yes
VFFRA-BR	[108]	2013	–	Wormhole	2D	Routers internal channels faults	Minimal	Odd-even Turn Model	No
ZoneDefense	[109]	2014	Adaptive	Wormhole	2D	Many faulty nodes	Minimal	Defense zone fault model	No
FaulToleReR	[110]	2014	Adaptive	Wormhole	2D	All faulty links	Minimal	–	Yes
VICIS	[111]	2012	Deterministic	Wormhole	Reconfigurable 2D	Links & routers failures	–	BRS	No
M-LBDR	[112]	2013	Deterministic	Wormhole	Irregular	Any single links faults	Minimal / Non Minimal	Turn Model/XY	No
4NP-First	[113]	2011	Adaptive	Wormhole	3D	Any number of faults in any location	Priority to minimal paths	Negative First	Yes
Deflection Routing	[114]	2011	Adaptive	–	3D	Permanent faults	Non Minimal	–	No
AFRA	[115]	2012	Deterministic	Wormhole	3D	Faulty vertical links	Minimal / Non Minimal	ZXY, XZXY	Yes
HamFa	[116]	2013	Partially Adaptive	Wormhole	2D & 3D	Almost all one-faulty unidirectional links	Minimal	Hamiltonian path strategy	Yes
3DFAR	[[54]	2013	Fully Adaptive	Wormhole	3D	Faulty routers and links	Minimal	–	Yes

Table 15
Deadlock free, congestion-aware and fault tolerant NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Failure type/number	Path length	Based on	Virtual channel
RAFT	[117]	2011	Adaptive	Wormhole	2D & Irregular	Links and routers failures	Non Minimal	OFLT	Yes
MAFA/Enhanced MAFA	[118]	2012	Adaptive	Wormhole	2D	Up to 6 faulty links	Minimal / Non Minimal	Turn Model	Yes
HipFar	[119]	2013	Fully adaptive	Wormhole	2D	Up to 6 faulty nodes	Non Minimal	Turn Model	Yes
ACO-FAR	[120]	2013	Adaptive	Wormhole	2D	Up to 4 faulty nodes	Minimal / Non Minimal	ACO	No
FTA-ASN	[121]	2013	-	-	2D	Any number of faulty link	Minimal / Non Minimal	-	No
RR-2D	[122]	2014	Fully Adaptive	Wormhole	2D	Faulty links/routers	Minimal / Non Minimal	-	Yes
RR-3D	[122]	2014	Fully Adaptive	Wormhole	3D	Faulty links/routers	Minimal / Non Minimal	RR-2D	Yes

Table 16
Deadlock free, livelock free, congestion-aware and fault tolerant NoC routing protocols.

Algorithm	Ref.	Year	Path definition	Switching technique	Topology	Failure type/number	Path length	Based on	Virtual channel
DF-NARCO	[123]	2012	Deterministic	Wormhole	2D	Faulty nodes	Non Minimal	NARCO, FTXY, OE, XY	Yes
MD	[124]	2013	Deterministic & Fully Adaptive	Wormhole	2D	Up to 2 faults	Minimal	DyXY	Yes
LAFT	[125]	2013	Partially adaptive	Wormhole	3D	Faulty links	Minimal	LA-XYZ	No

routers to select another TSV if the vertical link at the router's location is faulty. "ETW" is deadlock free by using only one virtual channel in the Y-dimension.

Table 16 summarizes the protocols described in the Subsection 3.3.3. They mainly use virtual channels, which requires more memory resources. However, they deal robustly with the two important objectives: congestion-awarness and fault tolerance.

3.3.4. Deadlock free, livelock free, congestion-aware and fault tolerant routing protocols

In spite of the problem complexity due to the diversity of constraints to be considered, the area of routing algorithms aiming at satisfying the four objectives at the same time is not fertile. In fact, the literature has a couple of papers that meet this need. Zinzuwadia et al. [123] propose "DF-NARCO" based on NARCO where two

Table 17
Weaknesses of proposed solutions.

Used solutions	Weaknesses
Deterministic routing	Causes congestion in the network
CDG dependency	Needs a proof
Virtual channels	Need more buffer space
Prohibited turns	Few links ⇒ low path number
Minimal path	Limits the number of alternative paths
Use of routing tables	Needs more buffer space and it is not scalable
Adaptive routing	Generates high latency
Q-learning	Needs more buffer space
ACO (metaheuristic)	High energy consumption
Reuse / alternative buffers	New architecture and rulemaking needed
Rerouting around faulty regions	Congestion around region and high latency

parameters “fault rate” and “congestion rate” are used with fixed threshold values. Depending on the case, the algorithm chooses among XY, FTXY and OE the most appropriate one to bypass faulty and congestion problems. To avoid deadlock, “DF-NARCO” uses two VCs and since it is deterministic, it is then livelock free. Ebrahimi et al. [124] study the selection of minimal paths when available, and propose “MD” routing algorithm taking advantage of the fully adaptive characteristics to obtain fault information and some congestion conditions. “MD” uses two VCs to avoid deadlock.

Ben Ahmed and Ben Abdallah [125] describe “LAFT” which handles faulty links and combines fault tolerance with look-ahead routing (LA-XYZ) to detect faults. They select the next hop according to the number of choices amongst different directions in order to find the least congested path. As it is shown in Table 17 which gives more details, “LAFT” is minimal, and is therefore deadlock free and livelock free.

3.3.5. Discussion

One can assume that when congested and faulty nodes are avoided and when deadlock is removed in the NoC, packets have no reason to be blocked or lost. To verify this, we analyze protocols meeting three and four objectives at a time, and several observations are noted.

First of all, we remark that algorithms meeting N-objectives are often compared to those meeting (N-1)-objectives, which is a good practice to appreciate the improvement brought by the new added objective.

Tests carried out on congestion-aware algorithms show that the throughput and the load distribution are improved every time, whereas low latencies are obtained only with realistic traffics, random or hotspot. However, under the uniform, traffic XY latency outperforms all the other protocols.

On the other hand, many fault tolerant techniques enhance throughput compared to equivalent bi-objective algorithms and come at latencies less or equal to that obtained by XY.

Though, there are a few work about power consumption, but the results show that all methods avoiding congestion are greedy in energy since they are often adaptive, when it is rational in the case of avoiding failures.

Similarly, area overhead test is done especially in fault tolerant approaches where we observe that the values obtained are higher than XY area but remain still insignificant. This is expected since solutions used to avoid congestion and failures require more network resources as it is detailed in Section 4.2.

4. Summary

In spite of the analysis provided in the discussion of each protocols family, some results are common for all the approaches independently of the number of objectives they meet. In fact, in addition to the NoC routing classification proposed in this paper, the present study allows us to make a comparison of the surveyed algorithms from several levels in order to distinguish between the most used practices from the less used ones.

In what follows, we summarize a number of results deduced from the studied algorithms in order to give a clear idea about elementary questions which might be asked about the development of a routing protocol such as: the most addressed issue, the most used techniques to solve the different problems, tools employed to evaluate new approaches, the most used topology, the traffic frequently used in data transmission through the network and metrics that are evaluated according to the objective to achieve.

4.1. Studied objectives

The number of algorithms classified in this article reveals that the NoC routing field is much studied due to the great importance given to a data transmission. As we see throughout the present survey, there are several types of protocols treating different objectives. However, the interest given toward each of these objectives is usually not equal.

We observe that the deadlock freedom is the most studied, almost 85% of algorithms concern the issue of deadlock because of the harmful consequences it causes on the NoC when it occurs. The livelock arrives in second position with 60% of papers. This includes approaches based on minimal paths even if the livelock freedom is not explicitly expressed by the authors. 50% deal with failures and 35% with congestion.

4.2. Proposed solutions

In order to avoid or remove some routing problems, the literature presents several solutions. Some of them are more appropriate for one problem than for another. The set of those solutions could be summarized according to the problem that each of them solves.

To avoid deadlock, most researches use virtual channels, deterministic strategies, CDG dependency and techniques based on prohibited turns, whereas to avoid livelock it is recommended to use minimal paths, deterministic routing or limit the number of hops. As regards the congestion, adaptive strategies are the most common solutions which are resulted from the use of Q-learning methods or metaheuristics like ACO, but routing tables could also help to avoid congested regions. Finally, the solutions proposed to avoid failures are adaptive strategies, routing tables, reuse/alternative buffers, re-routing around a faulty regions and in some papers the use of ACO.

To give a close idea about the utilization ratio of each problem solution, we provide in Fig. 3 the number of algorithms that solve each problem by using a given solution.

We can see that VCs with prohibited turns, minimal path, Q-learning and fault models are respectively the most used techniques to overcome deadlock, livelock, congestion and failures.

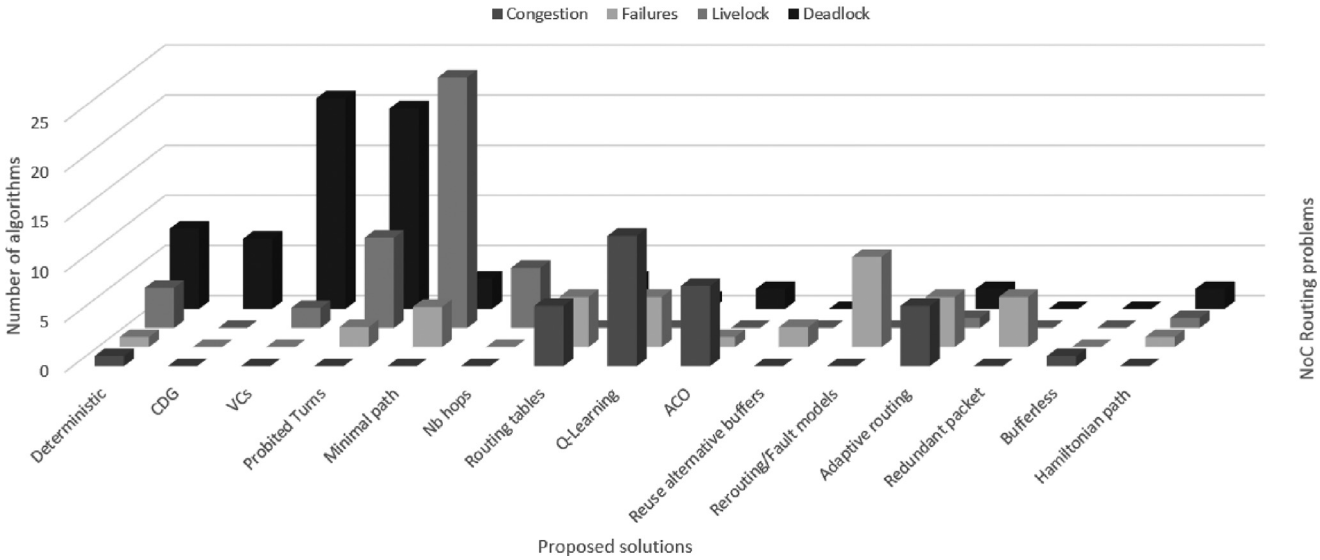

Fig. 3. Utilization ratio of proposed solutions for each routing problem.

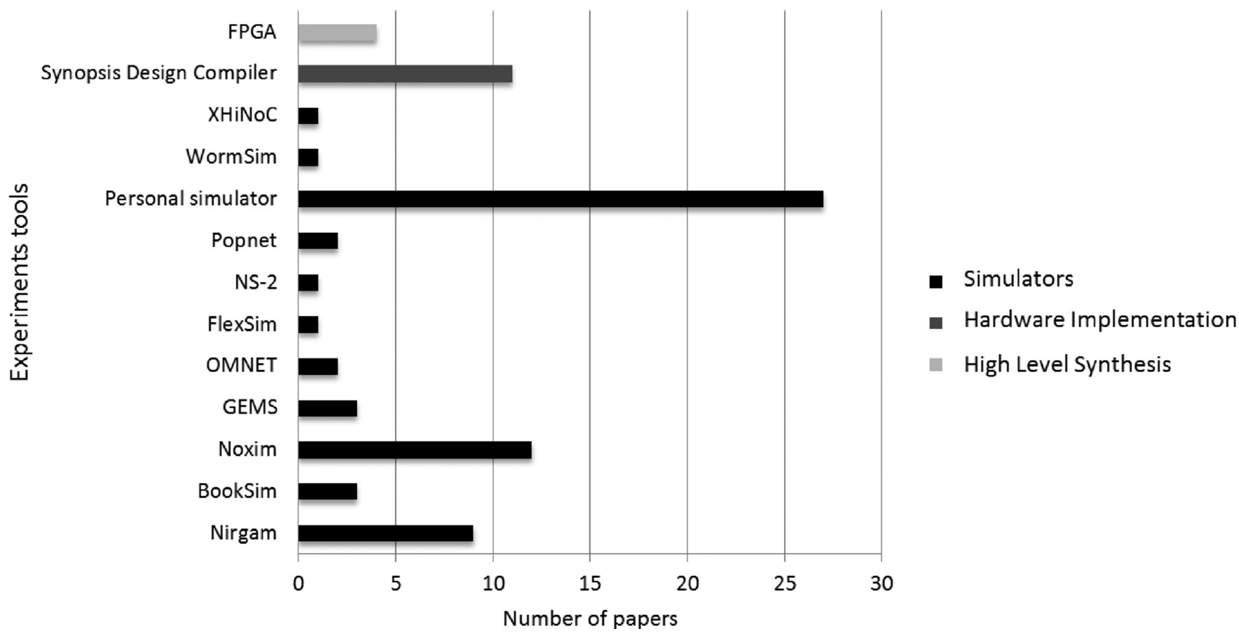

Fig. 4. The experiments tools used in the surveyed algorithms.

Even if these solutions improve the reliability of the NoC and keep it connected, they remain nevertheless limited and may present drawbacks either by causing other problems or by generating negative impact on the NoC performance as it is shown in Table 17.

4.3. Topologies

Proposed solutions are generally tested on a classical 2D mesh topology. 67% of the studied algorithms use it on a static network because of its simple implementation, whereas only 3% use the irregular 2D topology and 7% the reconfigurable one. On the other side, there are about 21% of strategies based on regular 3D mesh topology, but only 3% use the irregular 3D architecture. The interest on 3D architecture is due to the number of additional alternative paths it offers which increases a degree of adaptivity. Moreover, with a 3D architecture, a large amount of bandwidth could be offered which is advantageous for multimedia applications when the algorithm used is well optimized. We find also a couple of strategies using hierarchical network, dynamic 2D and irregular reconfigurable network.

From these statistics, we can see that the irregular topologies are not commonly employed. They are generally exploited in fault tolerance studies since different faults transform the initial regular topology to an irregular one.

4.4. Tests

Tools used for testing the existent approaches are also compared. Obtained results reveal that most of the experiments are simulated. There are several NoC simulators in the literature. Two of them are popular and are employed in many works: Noxim [127] and Nirgam [128]. However, we observe that in most cases authors opt for their own simulators developed in different languages such as C++ and VHDL.

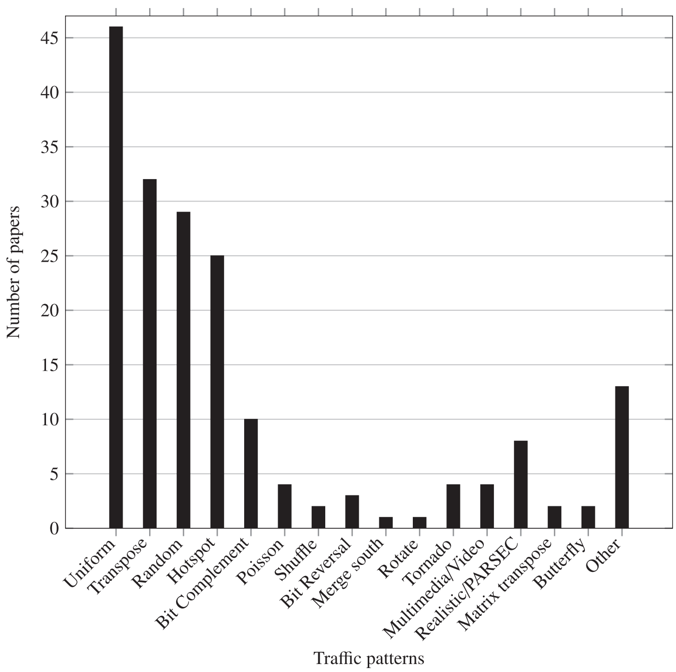

Fig. 5. Utilization ratio of traffic patterns in the surveyed algorithms.

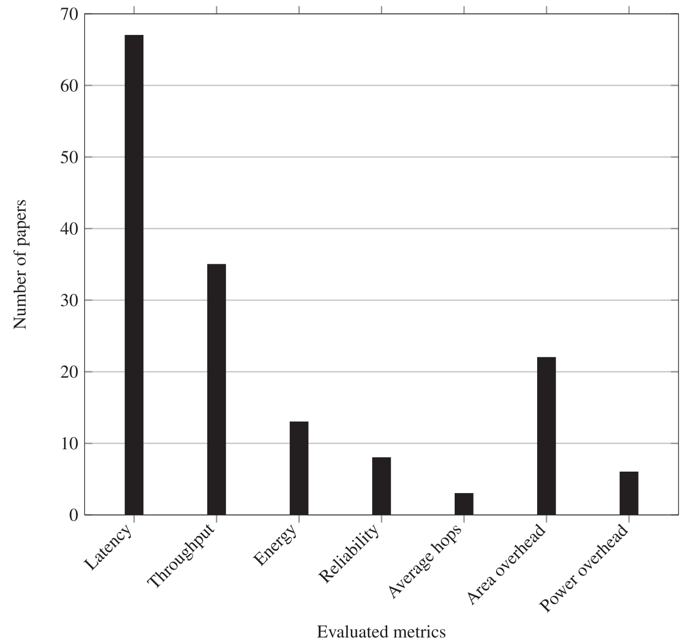

Fig. 6. Evaluated metrics in the surveyed algorithms.

As it is shown in Fig. 4, there are nevertheless some algorithms for which a physical implementation is done under Synopsis Design Compiler and some others for which a synthesis on FPGA cards is made.

4.5. Traffic

In order to provide an idea about the amount of data transmitted on the NoC before evaluating its performance, we summarize here the different types of traffic used in the literature. Our study reports that the synthetic uniform traffic pattern is the most widely used, followed by transpose, random and hotspot models. Very few approaches are tested under video or multimedia applications. Similarly, only 8% of surveyed algorithms are tested on realistic traffic including PARSEC.

The detailed list of traffic patterns used in the defined protocols and the proportion of their utilization are shown in Fig. 5. We note that the rest of traffic patterns mentioned by "Other" gathers the number of algorithms which tested on bursty traffic model, CBR, worst-case, destination fixed, GSM, MMS, mixed traffic, local application and on ten benchmarks as it is the case in [110].

4.6. Evaluated metrics

The last point we analyze from the studied algorithms is the metrics that are frequently evaluated in order to get an estimation about NoC performances. In fact, a good routing algorithm should ensure low latency, high throughput and low energy consumption. From the existing work, we observe that most of the experiments estimate the latency of the concerned algorithm. In contrast, less attention is given to the energy consumption while it is an important parameter since it is directly related to the chip technology size which is in continual decrease. Consequently, it is strongly recommended to maintain a moderate power consumption on the chip in order to avoid overheating.

Thanks to the area overhead metric, it is possible to estimate the surface required by a developed NoC routing algorithm which helps to make prediction about the necessity to supply or not the number of devices on the chip. The majority of researches providing it are those where the physical implementation is done. This observation is also valid to power overhead.

Fig. 6 gathers all the metrics evaluated in the surveyed algorithms with the number of papers discussing each of them.

5. Conclusions and perspectives

This paper discusses the main issues of routing in NoCs and enumerates a non-exhaustive set of routing protocols classified in two main groups: mono-objective and multi-objectives algorithms. The objectives are set according to the number of issues the protocol fixes. Three classes raise: mono-objective, two-objectives and three and four objectives protocols.

This classification highlights, for each routing strategy: the principle, the main features, the technique used to achieve one or several objectives. Each section ends with a discussion of the impact of each method on the NoC performance. The required resources and the improvements involved by meeting more than one objective at a time, are also described.

The summary synthesizes the general properties of all the defined protocols. Details are given about the most used topologies, the test tools, the most used traffic patterns, the most studied objectives and the most common solutions used to solve each problem.

Despite the great number of works in the literature, many key research directions could be suggested. For example, the literature shows that buffer-less methods reduce power consumption. However, congestion might occur. To overcome this situation, a solution consists of using metaheuristics like ACO to balance the traffic on the network and increase throughput saturation. In the same time, metaheuristics can be useful to detect and avoid faults.

Similarly, RNoCs (Reconfigurable Network on Chip) could be used to effectively distribute the heat in the NoC. The reason is that they can improve resource usage and/or alter protocols and mechanisms in realtime NoC.

The Kth shortest path technique is also an interesting direction to follow. It could increase the probability of selecting the path satisfying a maximum of constraints. This solution may be computationally intensive and could consume a large amount of resources.

However, by integrating heuristics, these drawbacks could be overcome, as it is the case in conventional networks.

Considering the large number of constraints in NoC routing is complex problem which requires a solution based on optimization methods. This could be a good way to fulfill the four objectives defined in this paper (deadlock and livelock freedom, congestion-awareness and fault tolerance). It also could also improve performance (low power consumption, low latency, low buffer consumption and high throughput). This idea is very interesting since it allows exploring more efficiently the solution space, trying to find the best compromise, according to the selected cost parameters.

Eventually, we note that the development of routing protocols is not the only solution to address the routing problem. In fact, several contributions propose new router architectures that provide reasonable performance to the network while guaranteeing different routing objectives [129–133].

References

[1] F.G. Moraes, A. Mello, L. Möller, L. Ost, N.L.V. Calazans, A low area overhead packet-switched network on chip: Architecture and Prototyping., in: VLSI-SOC, 2003, pp. 318–323. http://www.academia.edu/download/30279426/2003_vlsi_noc.pdf

[2] S.-J. Chen, Y.-C. Lan, W.-C. Tsai, Y.-H. Hu, Reconfigurable Networks-on-Chip, 1 edition, Springer-Verlag New York, 2011.pp. XIV, 206, ISBN 978-1-4419-9341-0.

[3] A. Agarwal, C. Iskander, R. Shankar, Survey of network on chip (noc) architectures & contributions, J.Eng. Comput. Arch. 3 (1) (2009) 21–27. http://www.scientificjournals.org/journals2009/articles/1423.pdf

[4] K.M. Al-Tawil, M. Abd-El-Barr, F. Ashraf, A survey and comparison of wormhole routing techniques in a mesh networks, Netw. IEEE 11 (2) (1997) 38–45. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=580917

[5] A. Pullini, F. Angiolini, D. Bertozzi, L. Benini, Fault tolerance overhead in network-on-chip flow control schemes, in: Integrated Circuits and Systems Design, eighteenth Symposium on, IEEE, 2005, pp. 224–229. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4286861

[6] W. Yongqing, Z. Minxuan, X. CanWen, A fault tolerant adaptive routing algorithm in 2D mesh network on chip, in: Communication Software and Networks (ICCSN), 2011 IEEE third International Conference on, IEEE, 2011, pp. 140–144. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6013681

[7] M. Atagoziyev, Routing algorithms for on chip networks, M. Sc. Thesis Middle East Technical University, 2007 Ph.D. thesis. http://etd.lib.metu.edu.tr/upload/12609136/index.pdf

[8] J. Delorme, Méthodologie de modélisation et d'exploration d'architecture de réseaux sur puce appliquée aux télécommunications, INSA de Rennes, 2007 Ph.D. thesis. https://tel.archives-ouvertes.fr/tel-00266880/

[9] L. Ni, P. McKinley, A survey of wormhole routing techniques in direct networks, Comput. 26 (2) (1993) 62–76.

[10] R.V. Boppana, S. Chalasani, A comparison of adaptive wormhole routing algorithms, ACM SIGARCH Comput. Arch. News 21 (2) (1993) 351–360. http://dl.acm.org/citation.cfm?id=165177

[11] G.-M. Chiu, The odd-even turn model for adaptive routing, Parallel Distributed Syst. IEEE Trans. 11 (7) (2000) 729–738. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=877831

[12] V. Rantala, T. Lehtonen, J. Plosila, Network on Chip Routing Algorithms, Technical Report, 2006.

[13] T. Bjerregaard, S. Mahadevan, A survey of research and practices of Network-on-chip, ACM Comput. Surv. 38 (1) (2006) 1–es, doi:10.1145/1132952.1132953. http://portal.acm.org/citation.cfm?doid=1132952.1132953

[14] E. Bolotin, I. Cidon, R. Ginosar, A. Kolodny, Routing table minimization for irregular mesh NoCs, in: Proceedings of the conference on Design, automation and test in Europe, EDA Consortium, 2007, pp. 942–947. http://dl.acm.org/citation.cfm?id=1266570

[15] P. Gratz, B. Grot, S.W. Keckler, Regional congestion awareness for load balance in networks-on-chip, in: High Performance Computer Architecture, 2008. HPCA 2008. IEEE fourteenth International Symposium on, IEEE, 2008, pp. 203–214. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4658640

[16] J.M. Montanana, D. de Andres, F. Tirado, Fault Tolerance on NoCs, IEEE, 2013, pp. 138–143, doi:10.1109/WAINA.2013.221. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6550386

[17] J. Flich, T. Skeie, A. Mejia, O. Lysne, P. Lopez, A. Robles, J. Duato, M. Koibuchi, T. Rokicki, J.C. Sancho, A survey and evaluation of topology-agnostic deterministic routing algorithms, IEEE Trans. Parallel Distributed Syst. 23 (3) (2012) 405–425, doi:10.1109/TPDS.2011.190. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5953590

[18] M. Ebrahimi, Fully adaptive routing algorithms and region-based approaches for two-dimensional and three-dimensional networks-on-chip, IET Comput. Digit. Tech. 7 (6) (2013) 264–273, doi:10.1049/iet-cdt.2013.0034. http://digital-library.theiet.org/content/journals/10.1049/iet-cdt.2013.0034

[19] M. Ebrahimi, M. Daneshtaleb, Learning-based routing algorithms for on-chip networks, Routing Algorithms in Networks-on-Chip, springer, Palesi, Maurizio, Daneshtalab, Masoud, 2014.

[20] A.E. Kiasari, A. Jantsch, Z. Lu, A heuristic framework for designing and exploring deterministic routing algorithm for NoCs, in: Routing Algorithms in Networks-on-Chip, Springer, 2014, pp. 21–39. http://link.springer.com/chapter/10.1007/978-1-4614-8274-1_2

[21] W. Dally, C. Seitz, Deadlock-free message routing in multiprocessor interconnection networks, Comput. IEEE Trans. C-36 (5) (1987) 547–553. http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=1676939&tag=1

[22] C.R. Jesshope, P. Miller, HIGH PERFORMANCE COMMUNICATIONS IN PROCESSOR, Computer Architecture, 1989. The sixteenth Annual International Symposium on (1989) 150–157, doi:10.1109/ISCA.1989.714549. http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=714549

[23] C.J. Glass, L.M. Ni, The turn model for adaptive routing, J. ACM (JACM) 41 (5) (1994) 874–902. http://dl.acm.org/citation.cfm?id=185682

[24] J. Duato, A new theory of deadlock-free adaptive routing in wormhole networks, Parallel Distributed Syst. IEEE Trans. 4 (12) (1993) 1320–1331. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=250114

[25] J. Duato, A necessary and sufficient condition for deadlock-free adaptive routing in wormhole networks, Parallel Distributed Syst. IEEE Trans. 6 (10) (1995) 1055–1067. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=473515

[26] J. Duato, A necessary and sufficient condition for deadlock-free routing in cut-through and store-and-forward networks, Parallel Distributed Syst. IEEE Trans. 7 (8) (1996) 841–854. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=532115

[27] W.J. Dally, H. Aoki, Deadlock-free adaptive routing in multicomputer networks using virtual channels, Parallel Distributed Syst. IEEE Trans. 4 (4) (1993) 466–475. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=219761

[28] X. Lin, P.K. McKinley, L.M. Ni, The message flow model for routing in wormhole-routed networks, Parallel Distributed Syst. IEEE Trans. 6 (7) (1995) 755–760. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=395404

[29] L. Schwiebert, D.N. Jayasimha, A necessary and sufficient condition for deadlock-free wormhole routing, J.Parallel Distributed Comput. 32 (1) (1996) 103–117. http://www.sciencedirect.com/science/article/pii/S0743731596900088

[30] M. Ebrahimi, M. Daneshtalab, P. Liljeberg, J. Plosila, J. Flich, H. Tenhunen, Path-based partitioning methods for 3D networks-on-chip with minimal adaptive routing, IEEE Trans. Comput. 63 (3) (2014) 718–733, doi:10.1109/TC.2012.255. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6338924

[31] C. Jackson, S.J. Hollis, A deadlock-free routing algorithm for dynamically reconfigurable networks-on-c, Microprocess. Microsyst. 35 (2) (2011) 139–151. http://www.sciencedirect.com/science/article/pii/S0141933110000645

[32] C.J.C.H. Watkins, Learning from Delayed Rewards, King's College, Cambridge, 1989 Ph.D. thesis.

[33] D. Xiang, Y. Zhang, Y. Pan, Practical deadlock-Free fault-tolerant routing in meshes based on the planar network fault model, IEEE Trans. Comput. 58 (5) (2009) 620–633, doi:10.1109/TC.2008.211. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4674344

[34] A.A. Chien, J.H. Kim, Planar-adaptive routing: Low-cost adaptive networks for multiprocessors, J. ACM (JACM) (1995) 91–123. http://dl.acm.org/citation.cfm?id=200856

[35] R.V. Boppana, S. Chalasani, Fault-tolerant wormhole routing algorithms for mesh networks, Comput. IEEE Trans. 44 (7) (1995) 848–864. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=392844

[36] D. Wang, A rectilinear-monotone polygonal fault block model for fault-tolerant minimal routing in mesh, Comput. IEEE Trans. 52 (3) (2003) 310–320. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1183946

[37] Z. Jiang, J. Wu, D. Wang, A new fault information model for fault-tolerant adaptive and minimal routing in 3-D meshes, IEEE, 2005, pp. 500–507, doi:10.1109/ICPP.2005.9.

[38] R. Holsmark, S. Kumar, Design issues and performance evaluation of mesh NoC with regions, in: NORCHIP Conference, 2005. 23rd, IEEE, 2005, pp. 40–43. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1596984

[39] M. Radetzki, C. Feng, X. Zhao, A. Jantsch, Methods for fault tolerance in networks-on-chip, ACM Comput. Surv. 46 (1) (2013) 1–38, doi:10.1145/2522968.2522976. http://dl.acm.org/citation.cfm?doid=2522968.2522976

[40] Su Hu, Xiaola Lin, A symmetric odd-even routing model in network-on-chip, IEEE Computer Society, Shanghai, (Volume: 1), 2012, pp. 457–462, doi:10.1109/ICIS.2012.20. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6211138

[41] Z. Yu, X. Zeng, L. Zhou, others, Time-division-multiplexer based routing algorithm for NoC system, in: Circuits and Systems (ISCAS), 2013 IEEE International Symposium on, IEEE, 2013, pp. 1652–1655. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6572180

[42] R.S. Ramanujam, B. Lin, Near-optimal oblivious routing on three-dimensional mesh networks, in: Computer Design, 2008. ICCD 2008. IEEE International Conference on, IEEE, 2008, pp. 134–141. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4751852

[43] R.S. Ramanujam, B. Lin, Randomized partially-minimal routing: Near-optimal oblivious routing for 3-D mesh networks, IEEE Trans. Very Large Scale Integration (VLSI) Syst. 20 (11) (2012) 2080–2093, doi:10.1109/TVLSI.2011.2167361. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6087301

[44] H. Ying, A. Jaiswal, K. Hofmann, Deadlock-free routing algorithms for 3-D networks-on-chip with reduced vertical channel density topologies, in: High Performance Computing and Simulation (HPCS), 2012 International Conference on, IEEE, 2012, pp. 268–274. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6266923
[45] J. Lee, K. Choi, A deadlock-free routing algorithm requiring no virtual channel on 3D-NoCs with partial vertical connections, IEEE, Tempe, AZ, 2013, pp. 1–2, doi:10.1109/NoCS.2013.6558407.
[46] C.-H. Chao, K.-C. Chen, A.-Y. Wu, Routing-based traffic migration and buffer allocation schemes for 3-D network-on-chip systems with thermal limit, IEEE Trans. Very Large Scale Integration (VLSI) Syst. 21 (11) (2013) 2118–2131, doi:10.1109/TVLSI.2012.2227852. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6428725
[47] M. Ebrahimi, M. Daneshtalab, F. Farahnakian, J. Plosila, P. Liljeberg, M. Palesi, H. Tenhunen, HARAQ: Congestion-aware learning model for highly adaptive routing algorithm in on-chip networks, IEEE, 2012, pp. 19–26, doi:10.1109/NOCS.2012.10. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6209258
[48] F. Farahnakian, M. Ebrahimi, M. Daneshtalab, J. Plosila, P. Liljeberg, Adaptive reinforcement learning method for networks-on-chip, in: 2012 International Conference on Embedded Computer Systems (SAMOS), 2012, pp. 236–243, doi:10.1109/SAMOS.2012.6404180.
[49] Yu-Hsin Kuo, Po-An Tsai, Hao-Ping Ho, En-Jui Chang, Hsien-Kai Hsin, An-Yeu Wu, Path-diversity-aware adaptive routing in network-on-chip systems, IEEE, 2012, pp. 175–182, doi:10.1109/MCSoC.2012.20. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6354696
[50] L. Silva, N. Nedjah, L. de Macedo Mourelle, ACO approach in static routing for network-on-chips with 3D mesh topology, in: Circuits and Systems (LASCAS), 2013 IEEE Fourth Latin American Symposium on, IEEE, 2013, pp. 1–4. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6519038
[51] L. Silva˜Junior, N. Nedjah, L. de Macedo Mourelle, Routing for applications in NoC using ACO-based algorithms, Appl. Soft Comput. 13 (5) (2013) 2224–2231, doi:10.1016/j.asoc.2013.01.009. http://linkinghub.elsevier.com/retrieve/pii/S1568494613000264
[52] K.-H. Chen, G.-M. Chiu, Fault-tolerant routing algorithm for meshes without using virtual channels, J. Inf. Sci. Eng. 14 (4) (1998) 765–783. http://www.iis.sinica.edu.tw/JISE/1998/199812_04.pdf
[53] G. Xu, K. Ren, N. Gu, Stochastic Prefix-based fault tolerant source routing algorithm for Network on Chip, in: Computer & Information Science (ICCIS), 2012 International Conference on, 2, IEEE, 2012, pp. 712–717. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6297120
[54] M. Ebrahimi, M. Daneshtalab, P. Liljeberg, H. Tenhunen, Fault-tolerant method with distributed monitoring and management technique for 3D stacked meshes, in: Computer Architecture and Digital Systems (CADS), 2013 Seventeenth CSI International Symposium on, IEEE, 2013, pp. 93–98. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6714243 http://dl.acm.org/citation.cfm?id=2485668
[55] L.F. Bic, A.C. Shaw, Operating Systems Principles, 1 edition, ISBN-10: 0130266116, ISBN-13: 978-0130266118, Prentice Hall, New Jersey, 2002.
[56] Lee [Online; accessed April-2015]. http://users.eecs.northwestern.edu/~haizhou/357/lec6.pdf
[57] J.A. Boyan, M.L. Littman, Packet routing in dynamically changing networks: a reinforcement learning approach, Adv.Neural Inf. Process. Syst. (1994).671–671. https://www.cs.rutgers.edu/mlittman/papers/routing-nips.pdf
[58] R. Holsmark, S. Kumar, Corrections to Chen and Chiu's fault tolerant routing algorithm for mesh networks, J. Inf. Sci. Eng. 23 (6) (2007) 1649–1662. http://www.iis.sinica.edu.tw/page/jise/2007/200711_01.pdf
[59] L. Schwiebert, D.N. Jayasimha, Optimal fully adaptive minimal wormhole routing for meshes, J. Parallel Distributed Comput. 27 (1) (1995) 56–70. http://www.sciencedirect.com/science/article/pii/S0743731585710714
[60] D. Seo, A. Ali, W.-T. Lim, N. Rafique, M. Thottethodi, Near-optimal worst-case throughput routing for two-dimensional mesh networks, in: ACM SIGARCH Computer Architecture News, 33, IEEE Computer Society, 2005, pp. 432–443. http://dl.acm.org/citation.cfm?id=1070006
[61] A.M. Shafiee, M. Montazeri, M. Nikdast, An innovational intermittent algorithm in networks-on-chip (NOC), World Acad. Sci. Eng. Technol. 45 (2008) 145–147. http://www.waset.org/publications/7095
[62] P. Ghosal, S. Choudhuri, H. Rahaman, Diametric mesh of tree (DiaMoT) routing framework for high performance NoCs: a hierarchical approach, IEEE, 2012, pp. 532–537, doi:10.1109/HPCC.2012.78. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6332217
[63] J. Sebastian, G. Sharma, The poure zigzag model for routing in a NoC, in: Computing, Electronics and Electrical Technologies (ICCEET), 2012 International Conference on, IEEE, 2012, pp. 922–926. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6203774
[64] K. Bhardwaj, K. Chakraborty, S. Roy, An MILP-based aging-aware routing algorithm for NoCs, in: Proceedings of the Conference on Design, Automation and Test in Europe, EDA Consortium, 2012, pp. 326–331. http://dl.acm.org/citation.cfm?id=2492790
[65] B. Fu, Y. Han, J. Ma, H. Li, X. Li, An abacus turn model for time/space-efficient reconfigurable routing, in: Computer Architecture (ISCA), 2011 Thirtyeighth Annual International Symposium on, IEEE, 2011, pp. 259–270. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6307293
[66] A. Ben˜Ahmed, A. Ben Abdallah, LA-XYZ: Low latency, high throughput look-ahead routing algorithm for 3D network-on-chip (3D-NoC) architecture, IEEE, 2012, pp. 167–174, doi:10.1109/MCSoC.2012.24. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6354695
[67] N. Dahir, A. Yakovlev, R. Al-Dujaily, T. Mak, Highly adaptive and deadlock-free routing for three-dimensional networks-on-chip, IET Comput. Digit. Tech. 7 (6) (2013) 255–263, doi:10.1049/iet-cdt.2013.0029. http://digital-library.theiet.org/content/journals/10.1049/iet-cdt.2013.0029
[68] F. Dubois, A. Sheibanyrad, F. Petrot, M. Bahmani, Elevator-First: a deadlock-free distributed routing algorithm for vertically partially connected 3D-NoCs, Comput. IEEE Trans. 62 (3) (2013) 609–615. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6109239
[69] Kuan-Yu Su, Hsien-Kai Hsin, En-Jui Chang, An-Yeu Wu, ACO-based deadlock-aware fully-adaptive routing in network-on-chip systems, IEEE, 2012, pp. 209–214, doi:10.1109/SiPS.2012.14. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6363208
[70] K.-C. Chen, C.-C. Kuo, H.-S. Hung, A.-Y. Wu, Traffic-and thermal-aware adaptive beltway routing for three dimensional network-on-chip systems, in: Circuits and Systems (ISCAS), 2013 IEEE International Symposium on, IEEE, 2013, pp. 1660–1663. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6572182
[71] M. Ebrahimi, Xin Chang, M. Daneshtalab, J. Plosila, P. Liljeberg, H. Tenhunen, DyXYZ: Fully adaptive routing algorithm for 3D NoCs, IEEE, 2013, pp. 499–503, doi:10.1109/PDP.2013.80. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6498596
[72] K.-C. Chen, S.-Y. Lin, H.-S. Hung, A.-Y. A. Wu, Topology-aware adaptive routing for nonstationary irregular mesh in throttled 3D NoC systems, IEEE Trans. Parallel Distributed Syst. 24 (10) (2013) 2109–2120, doi:10.1109/TPDS.2012.291. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6327188
[73] A. Patooghy, S.G. Miremadi, XYX: a Power & performance efficient fault-tolerant routing algorithm for network on chip, IEEE, 2009, pp. 245–251, doi:10.1109/PDP.2009.30. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=4912940
[74] Y. Zou, S. Pasricha, NARCO: Neighbor aware turn model-based fault tolerant routing for NoCs, IEEE Embed. Syst. Lett. 2 (3) (2010) 85–89, doi:10.1109/LES.2010.2063415. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5535111
[75] F. Chaix, D. Avresky, N.-E. Zergainoh, M. Nicolaidis, Fault-tolerant deadlock-free adaptive routing for any set of link and node failures in multi-core systems, IEEE, 2010, pp. 52–59, doi:10.1109/NCA.2010.14. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5598232
[76] F. Chaix, D. Avresky, N.-E. Zergainoh, M. Nicolaidis, A fault-tolerant deadlock-free adaptive routing for on chip interconnects, in: Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011, IEEE, 2011, pp. 1–4. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5763303
[77] Y. Chen, L. Xie, J. Li, Z. Lu, A deadlock-free fault-tolerant routing algorithm based on pseudo-receiving mechanism for Networks-on-Chip of CMP, in: Multimedia Technology (ICMT), 2011 International Conference on, IEEE, 2011, pp. 2825–2828. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6002067
[78] Z. Zhang, A. Greiner, S. Taktak, A reconfigurable routing algorithm for a fault-tolerant 2d-Mesh Network-on-Chip, in: Design Automation Conference, 2008. DAC 2008. Fortyfifth ACM/IEEE, IEEE, 2008, pp. 441–446. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4555858
[79] S. Jovanovic, C. Tanougast, S. Weber, C. Bobda, A new deadlock-free fault-tolerant routing algorithm for NoC interconnections, in: Field Programmable Logic and Applications, 2009. FPL 2009. International Conference on, IEEE, 2009, pp. 326–331. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5272274
[80] H.-C. Chi, Y.-H. Jhang, W.-S. Chen, Tree-based routing for faulty on-chip networks with mesh topology, IEEE, 2010, pp. 321–326, doi:10.1109/ISVLSI.2010.72. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5572794
[81] E.-J. Chang, C.-H. Chao, K.-Y. Jheng, H.-K. Hsin, A.-Y. Wu, ACO-based cascaded adaptive routing for traffic balancing in NoC systems, in: Green Circuits and Systems (ICGCS), 2010 International Conference on, IEEE, 2010, pp. 317–322. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5543045
[82] H.-K. Hsin, E.-J. Chang, C.-H. Chao, A.-Y. Wu, Regional ACO-based routing for load-balancing in NoC systems, in: Nature and Biologically Inspired Computing (NaBIC), 2010 Second World Congress on, IEEE, 2010, pp. 370–376. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5716323
[83] F. Farahnakian, M. Ebrahimi, M. Daneshtalab, P. Liljeberg, J. Plosila, Bi-LCQ: a low-weight clustering-based Q-learning approach for NoCs, Microprocess. Microsyst. 38 (1) (2014) 64–75, doi:10.1016/j.micpro.2013.11.008. http://linkinghub.elsevier.com/retrieve/pii/S0141933113001944
[84] H.-K. Hsin, E.-J. Chang, A.-Y. Wu, Implementation of ACO-based selection with backward-ant mechanism for adaptive routing in network-on-chip systems, IEEE Embed. Syst. Lett. 5 (3) (2013) 46–49, doi:10.1109/LES.2013.2276211. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6574224
[85] M. Ali, M. Welzl, S. Hellebrand, A dynamic routing mechanism for network on chip, in: NORCHIP Conference, 2005. Twentythird, IEEE, 2005, pp. 70–73. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1596991
[86] M. Ebrahimi, M. Daneshtalab, J. Plosila, H. Tenhunen, Minimal-path fault-tolerant approach using connection-retaining structure in networks-on-chip, in: Networks on Chip (NoCS), 2013 Seventh IEEE/ACM International Symposium on, IEEE, 2013, pp. 1–8. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6558401
[87] N. Nikitin, S. Chatterjee, J. Cortadella, M. Kishinevsky, U. Ogras, Physical-aware link allocation and route assignment for chip multiprocessing, IEEE, 2010, pp. 125–134, doi:10.1109/NOCS.2010.22. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5507555

[88] J. Upadhyay, V. Varavithya, P. Mohapatra, A traffic-balanced adaptive wormhole routing scheme for two-dimensional meshes, Comput. IEEE Trans. 46 (2) (1997) 190–197. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=565594
[89] J. Hu, R. Marculescu, DyAD - smart routing for networks-on-chip, Design Autom. Conf. 2004. Proc. Fortyfirst (2004) 260–263. http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=1322482
[90] M. Li, Q.-A. Zeng, W.-B. Jone, DyXY: a proximity congestion-aware deadlock-free dynamic routing method for network on chip, in: Proceedings of the 4Fortythird annual Design Automation Conference, ACM, 2006, pp. 849–852. http://dl.acm.org/citation.cfm?id=1147125
[91] M. Daneshtalab, A. Sobhani, A. Afzali-Kusha, O. Fatemi, Z. Navabi, NoC hot spot minimization using AntNet dynamic routing algorithm, in: Application-specific Systems, Architectures and Processors, 2006. ASAP'06. International Conference on, IEEE, 2006, pp. 33–38. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=4019488
[92] M. Nickray, M. Dehyadgari, A. Afzali-Kusha, Adaptive routing using context-aware agents for networks on chips, in: Design and Test Workshop (IDT), 2009 4th International, IEEE, 2009, pp. 1–6. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5404108
[93] P.-T. Huang, W. Hwang, An adaptive congestion-aware routing algorithm for mesh network-on-chip platform, in: SOC Conference, 2009. SOCC 2009. IEEE International, IEEE, 2009, pp. 375–378. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5398015
[94] M.K. Puthal, V. Singh, M.S. Gaur, V. Laxmi, C-Routing: an adaptive hierarchical NoC routing methodology, in: VLSI and System-on-Chip (VLSI-SoC), 2011 IEEE/IFIP 19th International Conference on, IEEE, 2011, pp. 392–397. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6081616
[95] M. Ebrahimi, M. Daneshtalab, P. Liljeberg, J. Plosila, H. Tenhunen, LEAR - a low-weight and highly adaptive routing method for distributing congestions in on-chip networks, IEEE, 2012, pp. 520–524, doi:10.1109/PDP.2012.52. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6169630
[96] M. Ramakrishna, P.V. Gratz, A. Sprintson, GCA: Global congestion awareness for load balance in networks-on-chip, in: Networks on Chip (NoCS), 2013 Seventh IEEE/ACM International Symposium on, IEEE, 2013, pp. 1–8. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6558405
[97] T. Mak, P.Y.K. Cheung, K.-P. Lam, W. Luk, Adaptive routing in network-on-chips using a dynamic-programming network, IEEE Trans. Ind. Electron. 58 (8) (2011) 3701–3716, doi:10.1109/TIE.2010.2081953. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5590290
[98] J. Lee, D. Lee, S. Kim, K. Choi, Deflection routing in 3d network-on-chip with TSV serialization, in: Design Automation Conference (ASP-DAC), 2013 Eighteenth Asia and South Pacific, IEEE, 2013, pp. 29–34. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6509554
[99] S. Park, J.-H. Youn, B. Bose, Fault-tolerant wormhole routing algorithms in meshes in the presence of concave faults, in: Parallel and Distributed Processing Symposium, 2000. IPDPS 2000. Proceedings. Fourteenth International, IEEE, 2000, pp. 633–638. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=846045
[100] J. Wu, Fault-tolerant adaptive and minimal routing in mesh-connected multicomputers using extended safety levels, Parallel Distributed Syst. IEEE Trans.n 11 (2) (2000) 149–159. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=841751
[101] J. Wu, A fault-tolerant and deadlock-free routing protocol in 2D meshes based on odd-even turn model, Comput. IEEE Trans. 52 (9) (2003) 1154–1169. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=1228511
[102] J. Wu, D. Wang, Fault-tolerant and deadlock-free routing in 2-D meshes using rectilinear-monotone polygonal fault blocks, Int. J. Parallel, Emergent Distributed Syst. 20 (2) (2005) 99–111, doi:10.1080/17445760500033341. http://www.tandfonline.com/doi/abs/10.1080/17445760500033341
[103] D. Fick, A. DeOrio, G. Chen, V. Bertacco, D. Sylvester, D. Blaauw, A highly resilient routing algorithm for fault-tolerant NoCs, in: Proceedings of the Conference on Design, Automation and Test in Europe, European Design and Automation Association, 2009, pp. 21–26. http://dl.acm.org/citation.cfm?id=1874628
[104] C. Feng, Z. Lu, A. Jantsch, J. Li, M. Zhang, A reconfigurable fault-tolerant deflection routing algorithm based on reinforcement learning for network-on-chip, in: Proceedings of the Third International Workshop on Network on Chip Architectures, ACM, 2010, pp. 11–16. http://dl.acm.org/citation.cfm?id=1921254
[105] S. Xiangming, Configurable redundant routing for network on chip, IEEE, 2012, pp. 477–479, doi:10.1109/CICN.2012.70. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6375159
[106] V. Soteriou, C. Nicopoulos, A. Vitkovskiy, Dynamic fault-tolerant routing algorithm for networks-on-chip based on localised detouring paths, IET Comput.Digit. Tech. 7 (2) (2013) 93–103, doi:10.1049/iet-cdt.2012.0054. http://digital-library.theiet.org/content/journals/10.1049/iet-cdt.2012.0054
[107] C. Chen, S.D. Cotofana, An effective routing algorithm to avoid unnecessary link abandon in 2D mesh NoCs, IEEE, 2013, pp. 311–318, doi:10.1109/DSD.2013.42. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6628295
[108] S. Zhang, G. Han, F. Zhang, Very fine-grained fault-tolerant routing algorithm of NoC based on buffer reuse, in: Software Engineering and Service Science (ICSESS), 2013 Fourth IEEE International Conference on, IEEE, 2013, pp. 758–762. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6615416
[109] B. Fu, Y. Han, H. Li, X. Li, ZoneDefense: a fault-tolerant routing for 2-D meshes without virtual channels, IEEE Trans. Very Large Scale Integration (VLSI) Syst. 22 (1) (2014) 113–126, doi:10.1109/TVLSI.2012.2235188. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6475199
[110] R.J. Behrouz, M. Modarressi, H. Sarbazi-Azad, Fault-tolerant routing algorithms in networks on-chip, in: Routing Algorithms in Networks-on-Chip, Springer, 2014, pp. 193–210. http://link.springer.com/chapter/10.1007/978-1-4614-8274-1_8
[111] A. DeOrio, D. Fick, V. Bertacco, D. Sylvester, D. Blaauw, J. Hu, G. Chen, A reliable routing architecture and algorithm for NoCs, IEEE Trans. Comput. Aided Design Integrated Circuits Syst. 31 (5) (2012) 726–739, doi:10.1109/TCAD.2011.2181509. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6186857
[112] M. Kumar, V. Laxmi, M.S. Gaur, S.-B. Ko, others, Reconfigurable distributed fault tolerant routing algorithm for on-chip networks, in: Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), 2013 IEEE International Symposium on, IEEE, 2013, pp. 290–295. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6653621
[113] S. Pasricha, Y. Zou, A low overhead fault tolerant routing scheme for 3D networks-on-chip, IEEE, Santa Clara, CA, 2011, pp. 1–8, doi:10.1109/ISQED.2011.5770726.
[114] C. Feng, M. Zhang, J. Li, J. Jiang, Z. Lu, A. Jantsch, A low-overhead fault-aware deflection routing algorithm for 3D network-on-chip, IEEE, 2011, pp. 19–24, doi:10.1109/ISVLSI.2011.42. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=5992473
[115] S. Akbari, A. Shafiee, M. Fathy, R. Berangi, AFRA: a low cost high performance reliable routing for 3D mesh NoCs, in: Design, Automation & Test in Europe Conference & Exhibition (DATE), 2012, IEEE, 2012, pp. 332–337. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6176490
[116] M. Ebrahimi, M. Daneshtalab, J. Plosila, Fault-tolerant routing algorithm for 3D NoC using Hamiltonian path strategy, in: Proceedings of the Conference on Design, Automation and Test in Europe, EDA Consortium, 2013, pp. 1601–1604.
[117] M. Valinataj, S. Mohammadi, J. Plosila, P. Liljeberg, H. Tenhunen, A reconfigurable and adaptive routing method for fault-tolerant mesh-based networks-on-chip, AEU - Int. J. Electron. Commun. 65 (7) (2011) 630–640, doi:10.1016/j.aeue.2010.09.002. http://linkinghub.elsevier.com/retrieve/pii/S1434841110002141
[118] M. Ebrahimi, M. Daneshtalab, J. Plosila, H. Tenhunen, MAFA: Adaptive fault-tolerant routing algorithm for networks-on-chip, IEEE, 2012, pp. 201–207, doi:10.1109/DSD.2012.82. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6395726
[119] M. Ebrahimi, M. Daneshtalab, J. Plosila, High performance fault-tolerant routing algorithm for NoC-based many-core systems, IEEE, 2013, pp. 462–469, doi:10.1109/PDP.2013.75. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6498591
[120] C.-A. Lin, H.-K. Hsin, E.-J. Chang, A.-Y. Wu, ACO-based fault-aware routing algorithm for network-on-chip systems, in: Signal Processing Systems (SiPS), 2013 IEEE Workshop on, IEEE, 2013, pp. 342–347. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6674530
[121] S. Khoroush, M. Reshadi, A fault tolerant approach for application-specific network-on-chip, IEEE, Vilnius, 2013, pp. 1–6, doi:10.1109/NORCHIP.2013.6702014.
[122] M. Ebrahimi, Reliable and adaptive routing algorithms for 2D and 3D networks-on-chip, in: Routing Algorithms in Networks-on-Chip, Springer, 2014, pp. 211–237. http://link.springer.com/chapter/10.1007/978-1-4614-8274-1_9
[123] A. ˜ Zinzuwadia, P. Parandkar, R. Verma, S. Katiyal, An efficient deadlock-free NARCO based fault tolerant routing algorithm in NoC architecturehttp://www.ijetae.com/files/Volume2Issue2/IJETAE_0212_38.pdf
[124] M. Ebrahimi, M. Daneshtalab, J. Plosila, F. Mehdipour, MD: Minimal path-based fault-tolerant routing in on-chip networks, in: Design Automation Conference (ASP-DAC), 2013 18th Asia and South Pacific, IEEE, 2013, pp. 35–40. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6509555
[125] A. Ben˜Ahmed, A. Ben Abdallah, Architecture and design of high-throughput, low-latency, and fault-tolerant routing algorithm for 3D-network-on-chip (3d-NoC), J. Supercomput. 66 (3) (2013) 1507–1532, doi:10.1007/s11227-013-0940-9. http://link.springer.com/10.1007/s11227-013-0940-9
[126] C.J. Glass, L.M. Ni, Maximally fully adaptive routing in 2d meshes, In Proceedings of the 1992 International Conference on Parallel Processing, (Volume: 1), 1992, pp. 101–104.
[127] V. Catania, A. Mineo, S. Monteleone, M. Palesi, D. Patti, Noxim: an open, extensible and cycle-accurate network on chip simulator, in: 2015 IEEE 26th International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2015, pp. 162–163, doi:10.1109/ASAP.2015.7245728.
[128] Nirgam,[Online; accessed March-2015]. http://www.nirgam.ecs.soton.ac.uk
[129] M. Bahmani, A. Sheibanyrad, F. Petrot, F. Dubois, P. Durante, A 3D-NoC router implementation exploiting vertically-partially-connected topologies, IEEE, 2012, pp. 9–14, doi:10.1109/ISVLSI.2012.19. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6296440
[130] H.S. Castro, O.A. de Lima, A fault tolerant NOC architecture based upon external router backup paths, in: New Circuits and Systems Conference (NEWCAS), 2013 IEEE Eleventh International, IEEE, 2013, pp. 1–4. http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=6573562
[131] Y. He, H. Sasaki, S. Miwa, H. Nakamura, Predict-More router: a low latency NoC router with more route predictions, IEEE, 2013, pp. 842–850, doi:10.1109/IPDPSW.2013.40. http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=6650963

[132] M. Neishaburi, Z. Zilic, NISHA: a fault-tolerant NoC router enabling deadlock--free Interconnection of Subnets in Hierarchical Architectures, J. Syst. Arch. 59 (7) (2013) 551–569.
[133] W.-C. Tsai, D.-Y. Zheng, S.-J. Chen, Y.-H. Hu, A fault-tolerant NoC scheme using bidirectional channel, in: Proceedings of the Fortyeighth Design Automation Conference, ACM, 2011, pp. 918–923. http://dl.acm.org/citation.cfm?id=2024929
[134] X. Zhang, M. Ebrahimi, L. Huang, G. Li, A. Jantsch, A Routing-Level Solution for Fault Detection, Masking, and Tolerance in NoCs, in: 2015 23rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing, 2015, pp. 365–369.doi: 10.1109/PDP.2015.87
[135] L. Huang, J. Wang, M. Ebrahimi, M. Daneshtalab, X. Zhang, G. Li, A. Jantsch, Non-Blocking Testing for Network-on-Chip, IEEE Transactions on Computers 65 (3) (2016) 679–692, doi:10.1109/TC.2015.2489216.
[136] R. Salamat, M. Khayambashi, M. Ebrahimi, N. Bagherzadeh, A Resilient Routing Algorithm with Formal Reliability Analysis for Partially Connected 3D-NoCs, IEEE Transactions on Computers PP (99) (2016) 1, doi:10.1109/TC.2016.2532871.

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