Possible Measures to Enhance the Performance of Metal–Oxide Arresters in the EHV Network Under Very Fast Transients

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Abstract—It is well known that metal–oxide arresters (MOAs) do not have the capability of protecting the equipment in extra-high voltage networks, when they face the threats from very fast transients (VFTs). This "inaction" on the part of MOA is mainly brought by stray capacitance, which not only delays the conduction of MOA under VFTs but also brings a nonuniform voltage distribution across its structure and thereby impacts its life, especially, that of its top unit. This phenomenon prompts an urgent take on the factors that threaten the functioning of MOA under VFTs. After performing a thorough review of the studies made earlier, this study focuses on the further improvements required. This paper mainly deals with the accurate calculation of stray capacitance, its adverse impacts on MOA during its conduction phase, voltage distribution across the arrester with the aid of a finite-element method (FEM) and the Electromagnetic Transient Program (EMTP), and, finally, it explores the modifications required to get adequate protection for the equipment exposed to VFTs.

Index Terms—Arrester, conduction mode, residual voltage, voltage distribution and very fast transients.

I. INTRODUCTION

PRESENTLY, metal–oxide arresters (MOAs) find wide applications in extra-high voltage (EHV) networks. This modern overvoltage protective device has excellent nonlinear V-I characteristics [1], [2] and consists of zinc–oxide (ZnO) discs stacked in a porcelain/polymer insulator housing. This arrangement leads to the presence of a large capacitive component and small resistive component in the leakage current during its nonconduction phase. Thus, arrester capacitances that include stray capacitances play a prominent role in the arrester operation and govern the voltage distribution across the arrester units. Several other factors, such as height of the arrester structure; rise-time characteristics of the incoming current surges; and the presence of capacitive elements, such as capacitive voltage transformer (CVT) and underground (UG) cables in the system also, influence its performance [3]. On delving deep, it is observed that the stray capacitance and invading very fast current surges (with nanosecond front

time) have a strong influence on the operating behavior of MOA in EHV networks. In addition, stray capacitance brings nonuniform potential distribution across the entire arrester structure during its operation mode, thereby impacting its life span especially that of its top unit. All of these bring the present study on the conduction-mode performance of MOAs under VFT to the center stage.

On making a quick glimpse of the earlier works, it can be seen that these studies laid a lot of focus on the performance of the arrester during its nonconduction mode only [4]–[14]. Moreover, these studies reveal that the finite-element method (FEM) of computing the arrester stray capacitance and voltage distribution across the structure is one of the reliable and accurate methods, and geometrical and electrical properties of the arrester have a strong influence on its function, and provision of grading rings and internal parallel capacitors to the arresters are among the effective methods to achieve the uniform potential distribution across the arrester units.

Among other things, this study attempts to provide answers to the critical questions, such as how to balance the tradeoff involving stray capacitance and MOA on one hand, and fast fronted nanosecond current surges and the MOA on the other hand, and how to bring the voltage distribution experienced by the arrester during its conduction under VFTs to a level close to uniform; and, finally, what are the effective options available to attain the smooth functioning of MOAs under VFTs?

II. PROBLEM STATEMENT

It is well known that the overvoltage spectrum contains surges with the duration of nanoseconds to seconds. The epicenter of VFTs, which have the front time of several nanoseconds, lies in the switching operations of gas-insulated substations (GIS). There are instances to show that it originates during the switching operations of vacuum circuit breakers (CBs) and switches. Reports are also to the effect that lightning currents with nanosecond rising times are noticed in the substations [15]–[18]. The maximum value of the VFTs thus observed is reported to be on the order of 2.7 p.u. [19]. Among the factors that influence the amplitude of these steep fronted transients are the types of switch/breakers employed and certain specific system conditions. Higher amplitude VFTs are generally produced during the switching operations in the vacuum.

VFTs normally produce gradual but progressive degradation of the insulation of the equipment in a network. Among the
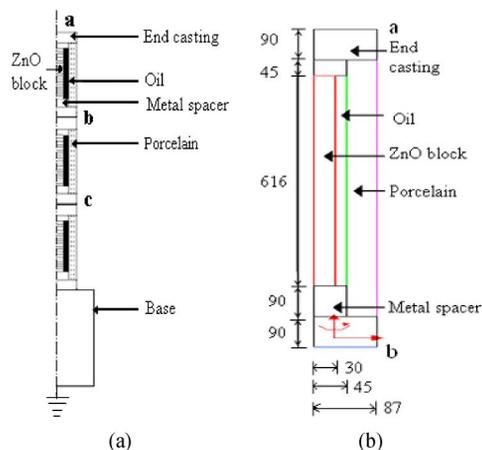
Fig. 1. (a) Cross-sectional view of the 198-kV arrester **a**, **b**, and **c**: metal flanges. (b) Dimensions of the 66-kV arrester (in millimeters).

equipment that faces such high risks are transformers, CBs, and arresters. In general, the nonuniform voltage distribution faced by the arrester during its operation is one of the causative factors for its failure.

This nonuniformity of the potential gradient across the arrester increases in direct proportion to the steepness of the intruding current surges. Thus, VFTs place all of the connected equipment in an EHV network including MOA, when it enters the network. But the protection afforded to them at present is not adequate; MOAs are unable to come to their rescue, when the equipment are experiencing threats from VFTs. This inaction on the part of MOAs is always a puzzle and it needs an early solution.

Several solutions that involve the suppression of VFTs by terminal components, provision of capacitive components, ferromagnetic rings, and resistor-fitted disconnectors have been suggested for the moderation of adverse effects of VFTs and the suppression of related resonances at the connected transformers. Reduction in the stray capacitance faced by the arresters and the slowdown of the invading very fast current surges are among the other mitigation measures recommended. Despite these measures, the stated problem still comes up short of an effective solution. Thus, the urgency of finding solutions to this long-pending problem brings this study to the center stage. This paper aims at the enhancement of the operating capability of MOAs and suggests various measures for it.

III. ARRESTER UNDER STUDY

A typical 198-kV metal–oxide surge arrester with three stacks of 66-kV rating is considered for the analysis. Fig. 1(a) and (b) shows the cross-sectional view (three stack: 198 kV) and dimensions (single stack: 66 kV) of the arrester.

Each stack of the 66-kV rating is comprised of 22, 3-kV arrester blocks. The dimension V-I characteristics, and other details are obtained from the arrester manufacturer. The arrester elements behave like several capacitors connected in series. In general, the capacitance and voltage distribution across the arrester units are controlled by the geometry of the arrester units and the properties of the constituent materials as well. Since the

arrester capacitances influence the nonuniform voltage distribution across the arrester structure, the determination of stray capacitance and its impact on the performance of the arrester assume greater significance.

A. Determination of Arrester Capacitance

Several techniques are available for the calculation of arrester capacitances that cover block and stray capacitances. Among them are the charge simulation method (CSM), surface charge method (SCM), boundary element method (BEM), and finite-element method (FEM). The first three techniques rely upon the reformation of the problem as an integral equation. CSM and BEM are useful to extract stray parameters of surge arresters. But they are not preferred for the complicated structures, such as ZnO arresters. SCM is accurate only for the objects of simple shapes, and its computational time is comparatively large. FEM solves the related differential equations directly and is found to be more suitable for the applications to the complex insulation structures, such as MOAs. Further results obtained by this technique are comparatively accurate and eliminate the need for further experimental methods [20]–[22]. Owing to its attractive features and merits, present FEM software packages are widely used for the works connected with the computation of stray inductances and capacitances and for the potential distribution across the arresters. The author is no exemption to this practice. The limited availability of testing facilities is another factor that forces the author to go for the Maxwell FEM package for this study.

1) Adoption of FEM for the Determination of Stray Capacitance: An FEM package is used to compute the capacitance distribution (block and stray) of the arrester. The 2-D axisymmetry electrostatic field solver of Maxwell's FEM package is used to compute the arrester block and stray capacitance. By solving the Laplace equation $\varepsilon \nabla^2 V(r, z) = 0$ with appropriate boundary conditions, the block capacitance and the stray capacitance are computed from the energy stored in the system. In order to show the variation of stray capacitance with voltage rating, the values of stray capacitance are computed for different voltage ratings of the arrester. For this study, an appropriate number of 66-kV stacks is stacked to obtain the desired voltage rating since the height of the arrester increases with voltage rating. Different voltage ratings are obtained by multiplying the number of stacks and the rating of a single stack (66 kV). For instance, for the 396-kV (6 × 66 kV) arrester, six 66-kV stacks are taken. The arrester stacks are mounted over a 1.5-m pillar above ground level. The total stray capacitance values for 66-, 132-, 198-, 264-, 330-, and 396-kV arresters are obtained and given in Table I.

B. Potential Distribution Across the Arrester Units

The surge arrester is a device to protect the system against overvoltages and facilitates insulation coordination. The residual voltage waveform of the arrester changes with respect to front time of the current surge, but not with its tail time. The tail times of the current surge do not influence the initial response of the arrester, and the drop in the tail of the voltage curve is not important for an insulation coordination study [3]. So in this analysis, the voltage distribution studies are made

TABLE I
STRAY CAPACITANCES FOR DIFFERENT HEIGHTS

Sl. No	Voltage rating of arrester (kV)		Height (mm)	Stray Capacitance Using FEM (pF)
1	66		2116	2.10
2	132		2732	4.58
3	198		3348	6.78
	198	1 gr	3348	5.43
	198	2 gr	3348	4.11
4	264		3964	8.86
5	330		4580	10.78
6	396		5196	14.61
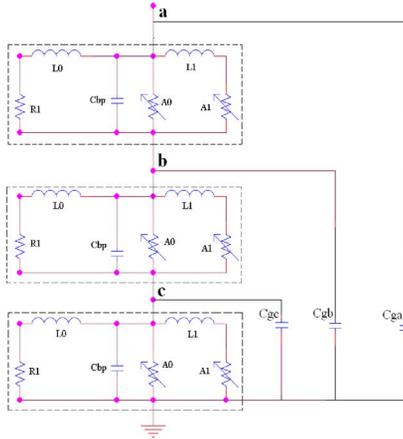
Fig. 2. Equivalent circuit of the complete arrester (198 kV) per IEC 60099-4. (All of the parameters within the dotted box are for the 66-kV arrester.)

based on current surges only with different front times, but not with tail times. For computing residual voltage (V_r) under VFTs, the surge arrester is modeled with an accurate value of block and stray capacitances.

1) Modeling of Arrester for VFTO: It is used to determine the voltage distribution across the arrester blocks during VFTs. To determine dynamic performance, an equivalent circuit, as prescribed in IEC 60099-4 [23], is used. The MOA is modeled as a distributed parameter with inclusion of accurately calculated arrester capacitances. Fig. 2 shows the IEC model for the three stack arrester (198 kV) with block and stray capacitances.

A0 and A1 are the nonlinear characteristic parameters of the arrester, represented with the two sections and are separated by L1. L0 is associated with magnetic fields in the vicinity of the arrester. The values of inductance, L0 and L1, are computed using the Margo *et al.* model [24]. Formulae used for the computation of arrester capacitances are as follows:

$$Lo = \frac{1}{12} \frac{[V_{r(1/T_2)} - V_{r(8/20)}]}{V_{r(8/20)}} V_n \qquad (1)$$

TABLE II
COMPARISON OF THE EXPERIMENTAL AND SIMULATED RESIDUAL VOLTAGE VALUES

Type of surge	Lightning surge 8/20 µs		Steep front surges 1/10 µs		VFT 0.1/10 µs
Current (kAp)	5	10	5	10	5
V_{re} (kVp)	520.08	551.76	573.54	614.46	640.00
V_{rs} (kVp)	522.06	553.80	575.52	611.16	616.00
Error (%)	-0.38	-0.36	-0.35	0.54	3.75

$$L1 = \frac{1}{4} \frac{[V_{r(1/T_2)} - V_{r(8/20)}]}{V_{r(8/20)}} V_n \qquad (2)$$

where $V_{r(1/T2)}$ is the residual voltage for a 1/T2 10-kA lightning current, $V_{r(8/20)}$ is the residual voltage for an 8/20 10-kA lightning current, and V_n is the arrester's rated voltage.

R1 (1 MΩ) is the resistance used to stabilize the numerical integration when the model is implemented on a digital computer program. C_{ga}, C_{gb}, and C_{gc} are the stray capacitances (C_{ga} can be neglected) and C_{bp} is the block capacitance of the arrester (here 66 kV) computed using FEM. It is found to be 45 pF. This model can be used for transient studies with current surges of front time from seconds to nanoseconds. The individual capacitance of the ZnO elements is also at the notable level. The measured capacitance of one 3-kV arrester block is 903 pF and total block capacitance for the 198-kV arrester is 15 pF. The total stray capacitance value is 6.78 pF.

The modeling procedure for the complete arrester assembly is presented in [25]. This study is limited to modeling of MOA only. Other system parameters, such as arrester leads and separation distances, are also important in the studies with lightning and other fast front overvoltage surges. For the investigations of the protective behavior of arresters in substations, the actual length of connecting leads with their inductances is to be taken into account. This model is used for computing voltage distribution while conducting current surges of different front times—microsecond to nanosecond level. The V_r values for the 198-kV arrester are determined using the Electromagnetic Transient Program (EMTP) for current surges of 8/20, 1/10, and 0.1/10 µs with different peak values.

2) Validation of the Model: The experimental (V_{re}) and simulated (V_{rs}) values of the residual voltage for the 198-kV arrester with different current surges, 8/20, 1/10, and 0.1/10 µs are compared. The percentage error between V_{re} and V_{rs} values with respect to V_{re} is calculated and shown in Table II. The percentage error noticed is comparatively less. Thus, the validity of the model employed is established.

After validating the accuracy of the arrester model with an experimental value, it is firmly concluded that this model can be used for further very fast transient overvoltage (VFTO) analysis. It is mainly due to the inclusion of calculated capacitance values in this model. Now, the peak value of V_r, with different current surges up to 5 ns are simulated using the aforementioned model and tabulated in Table III. It is found that the value of

TABLE III
PEAK VALUES OF RESIDUAL VOLTAGE–SIMULATED RESULTS

Front time (t_f) of Current surge (ns) Peak : 10 kA	V_r (kV)
8000	553.80
1000	611.16
100	618.00
10	620.40
5	624.60
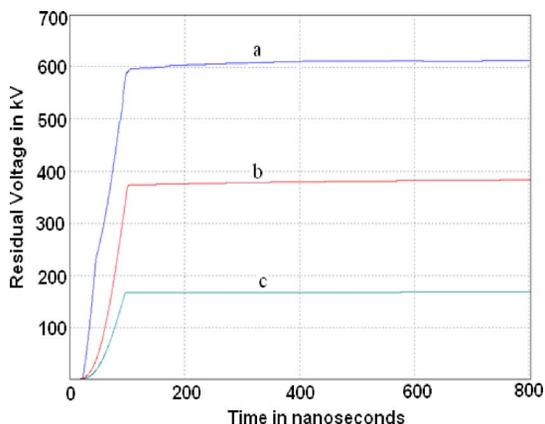
Fig. 3. Residual voltage waveforms for 1/10-μs, 10-kA current surge at metal flanges **a**, **b**, and **c**.

TABLE IV
PEAK VALUES OF RESIDUAL VOLTAGE (kV_p) IN METAL FLANGES AND ACROSS THE TOP UNIT OF THE ARRESTER

Metal flanges	Current surge with peak 10kA and tail time 10 μs				
	t_f: 8 μs	1 μs	0.1 μs	0.01 μs	0.005 μs
a	553.80	611.16	618.00	620.40	624.60
b	360.22	385.70	390.00	390.80	391.80
c	178.40	178.50	178.60	179.90	181.10
Voltage (kV_p) across top unit of the arrester					
(a-b)	193.58	225.46	228.00	229.60	232.80

TABLE V
VOLTAGE DISTRIBUTION ACROSS THE ARRESTER DURING VFTO AND NORMAL POWER FREQUENCY CONDITIONS

Metal flanges	Residual voltage with 8/20μs, 10kA current surge (kV_p)	% of total voltage	Residual voltage under 50Hz current kV_{rms}	% of total voltage
a	554.0	51.0	80.0	60.0
b	360.0	33.0	40.0	30.0
c	178.0	16.0	13.0	10.0

V_r increases with steepness of the current surge and this variation is also verified experimentally as outlined in Section III-C. After finding the peak of V_r, the distribution of voltage in three sections of arrester is computed using the EMTP with current surges of different front times, 8 μs to 5 ns. Thus, the model used for this study gets validated for VFTs.

3) Computation of Residual Voltage in Metal Flanges: Using the aforementioned arrester model for VFTO, the value of V_r at metal flanges (**a**, **b**, and **c**) during conduction of current surges of different front times with a peak of 10 kA is computed, shown in Table IV. Fig. 3 indicates the values of voltage at metal flanges (**a**, **b**, and **c**) for the 198-kV arrester while conducting 1/10 μs, 10-kA current surge. It was observed that the plotted curves (**a**, **b**, and **c**) in Fig. 3 did not change smoothly. It may be due to the limitations of the simulations carried out. The voltage that appears across the stack is found to be nonuniform during conduction mode. The top most unit (between the metal flanges **a** and **b**) is stressed more and the voltage appearing across the top unit of the arrester increases with the steepness of the surge, resulting in higher stress as shown in Table IV. In this context, it may be of interest to learn how the voltage distribution across the arrester occurs under normal power frequency operating conditions. To meet this check, the results of the field tests carried out in the Tamil Nadu Electricity Board (TNEB), India, with the aid of Live line High Pot Bushing and Insulator tester have been obtained and compared with the present study results as shown in Table V. The most highly stressed unit will limit the life of the entire arrester and, so, further analysis is made only on the top unit of the arrester. The stray capacitance causes higher stress in the top unit, which must be reduced by making modifications in the arrester and system that is of concern.

Among the methods to reduce the effect of stray capacitance, the adoption of grading rings finds an important place. It makes voltage distribution more uniform in nonconduction mode [4]–[14]. After placing grading rings, the arrester is re-modeled and voltage across the top unit during conduction mode is computed using EMTP. The voltage across the top unit for current surges of 0.01/10 μs and 0.005/10 μs with a peak value of 10 kA is found as 222.70 and 224.60 kV_p, respectively. It is shown that the grading rings help to make voltage distribution more uniform during conduction mode also.

Even though the effect of grading rings on the voltage distribution is found to be encouraging, the limitations imposed by the higher voltage-rated arresters stand in the way of this choice and restrict the addition of further grading rings. It necessitates the need for other alternatives, such as varying the combinations of arrester constituent materials.

In order to validate the simulated results of residual voltage, an experiment has been conducted on an arrester while conducting current surges of different steepness. The peak value of residual voltage and time at which it occurs are noted.

C. Measurements of Residual Voltage—Experimental Results

A 12-kV arrester is considered for experimental analysis. The residual voltages for this 12-kV arrester are measured when the arrester is conducting current surges of different steepness, with a peak of 5 kA. This experiment is conducted in the High Voltage Laboratory and the waveforms (Fig. 4) are measured using the CRO (TDS 3054B) with a frequency of 500 MHz and a sampling rate of 5 GSamples/s. It is observed that the magnitude of residual voltage increases with the steepness of current surge (Table VI). The trend of this residual voltage varia-
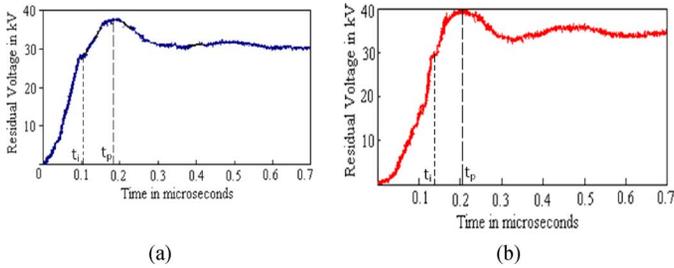
Fig. 4. Residual voltage (peak) waveforms. (a) Current surge $t_f = 180$ ns. t_i: 115.4 ns, t_p: 184.6 ns. (b) Current surge $t_f = 155$ ns, t_i: 138.0 ns, t_p: 215.4 ns.

TABLE VI
PEAK VALUES OF RESIDUAL VOLTAGES–EXPERIMENTAL RESULTS

Front time (t_f) of Current surge (ns) Peak : 5 kA	V_r (kV)
2000	36.1
180	37.9
155	39.9

tion has been compared with the one as obtained by simulation (Table III) using the arrester model for VFTO.

The time taken to reach initial peak t_i for current surges of front time 180 and 155 ns are 115.4 and 138.0 ns, respectively. Also, the time taken to reach final peak t_p for current surges of front time 180 and 155 ns are given by 184.6 and 215.4 ns, respectively. It is observed that the rise time of initial peak and final peak of the residual voltage (delay in its initial response) increase with a higher steepness of the current surge because of the capacitance effect, which causes a higher delay in its response. Experimentally, it is proved that the effect of arrester capacitance is more as the steepness of the current surge is increased and plays a major role under very fast transients, causing significant nonuniformity of voltage distribution especially for higher-rated arresters.

Due to the limitation of the testing facilities, the 12-kV arrester has been selected for this study. However, the study results are extrapolated and used for the 198-kV rated arrester employed in a 230-kV system.

IV. SUGGESTED MODIFICATIONS IN THE ARRESTER

The performance of ZnO elements is mainly dependent on the properties offered by the boundaries between ZnO grains. These are greatly affected by the formation of spinel particles between ZnO grains during the sintering process. The spinel particles have an important role in controlling the size of the ZnO grains by inhibiting ZnO grain growth during the sintering process. However, when there is a large amount of these spinel particles, the boundary area is decreased and the conducting paths through the element become confined. Therefore, the performance of elements can be improved by reducing the formation of spinel particles. The spinel-reduced element has a larger capacitance than normal elements, which is thought to be due to the wide conducting paths through the boundaries. This gives an advantage in the voltage distribution of complete arresters with shields or internal parallel capacitors for compensation. The higher grade ZnO elements make it possible to develop smaller size arresters

TABLE VII
VOLTAGE (kV$_p$) ACROSS THE TOP UNIT WITH HGM

Current surge with peak 10kA				
Type of surge	0.01/10 µs		0.005/10 µs	
Type of arrester	Conventional	with HGM	Conventional	with HGM
Peak voltage kV$_p$	229.60	217.40	232.80	219.20

for higher voltage applications. The use of additives facilitates this reduction in the size of ZnO grains and, hence, the arrester blocks [26]–[29]. Since the overall length of elements is reduced by increasing the voltage gradient, it is possible to obtain fairly uniform voltage distribution.

A. Using High Gradient Arrester Material

One effective method to shorten the arrester length and improve the potential distribution along the arrester column is to increase the voltage gradient of the ZnO arrester for a given rated voltage. The rare earth oxide is added to increase the voltage gradient of the arresters and by adding a suitable amount of oxides of metals Co and Mn, the leakage current can be decreased and the nonlinearity coefficient can be increased [27]. High gradient elements with twice the reference voltage gradient of conventional elements are developed to reduce the size and weight of arresters [28]. With high gradient ZnO material and reduced height, the stray capacitance values are computed using FEM. It is observed that there is a reduction in its stray capacitance values. The internal inductance of the newly developed arrester is also reduced, owing to the reduction in the total height of arrester elements. After remodelling the arrester with new high gradient arrester material, the voltage across the top unit of the arrester is computed using EMTP, and the values are tabulated in Table VII. It is observed that there is a reduction in voltage across the top unit of the arrester because of reduced value of stray capacitance with new arrester material. The addition of grading rings in tandem with high gradient material (HGM) still reduces the stress in the top unit, and this may be considered as a good option for HV-rated arresters. Thus, grading rings and high gradient play important roles in reducing stress in the top unit of the arrester.

V. SUGGESTED MODIFICATIONS IN THE SYSTEM

It was previously shown that the voltage distribution across the arrester units has a close relationship with the steepness of the intruding current surges, especially during the conduction phase of the arrester. This provides an option to restrict the severity of nonuniform voltage distribution experienced during arrester operation. It is nothing but the measures to clamp the steepness of incoming current surges by making certain modifications in the network like the introduction of capacitive elements, such as CVT, UG cable, and internal parallel capacitors in the arrester.

The usefulness of the aforementioned measures is studied by applying them to an in-service 230-kV gas-insulated substation
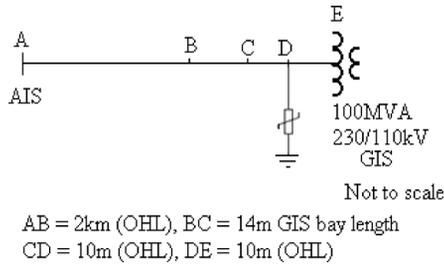
Fig. 5.　Single-line diagram of a 230-kV GIS in TNEB grid, India.

(GIS) in the TNEB grid in India. The details of the modified station per the study are shown in Fig. 5. In this context, it is stated that the arrangements made in a substation are normally based on the needs of the end user. In case of GIS with the rating of 300 kV and below, it is preferable to install the transformers and its related surge arresters in the open space of the air-insulated substation (AIS), just adjacent to the controlling breakers in the GIS portion. In the instant case also, this method is followed.

The nonlinearity index (α) is derived from the V-I characteristics of the arrester as furnished by the manufacturer. The α value is estimated between two desired magnitudes of current and corresponding voltage by

$$\alpha = \frac{\log\left(\frac{I2}{I1}\right)}{\log\left(\frac{V2}{V1}\right)} \quad (3)$$

where V_1 and V_2 are the voltages at current I_1 and I_2 ($I_2 > I_1$).

Surge arresters behave differently for various surge waveforms, depending each time on the magnitude and the rate of rise of the surge.

A. System Modeling

The system components are modeled with distributed parameters because this study is focused for VFTs. The capacitance (C) and inductance (L) of the GIS busbar are given by

$$C = \frac{2\pi\varepsilon_o\varepsilon_r}{\ln\frac{b}{a}} \quad (4)$$

$$L = \frac{\mu\ln\frac{b}{a}}{2\pi} \quad (5)$$

$$z_0 = \sqrt{\frac{L}{C}} \quad (6)$$

$$v = \frac{1}{\sqrt{LC}} \quad (7)$$

where **a** is the outside diameter of the GIS busbar, **b** is the inner diameter of the GIS busbar, z_o is the surge impedance, and **v** is the wave velocity. The surge impedance for the given GIS, overhead line, and cable are calculated as 78, 388, and 28 Ω, respectively. It is assumed that the surge propagates on the overhead line with the velocity of light and in GIS, 0.9 times the speed of velocity of light. The power transformer, which terminates the GIS bus, is represented as lumped capacitance to ground of 4 nF [3]. The other system parameters, such as arrester leads and separation distances, are considered in the studies with lightning and other fast front overvoltage surges. For the investigation of arresters in substations, the actual length of connecting
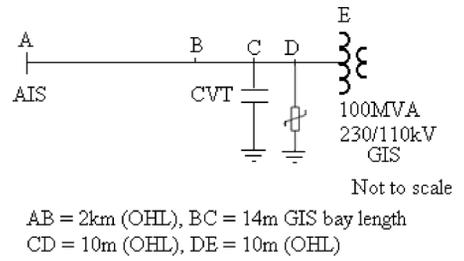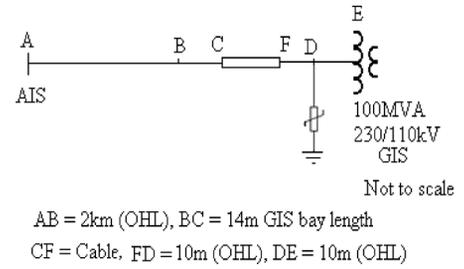
Fig. 6.　(a) The 230-kV system with cable. (b) 230-kV system with CVT.

leads with their inductances (1 μH/m) [1] is to be taken into account. The response of surge arresters to VFTs is not well characterized and the turn-on time of arresters is found to be much longer than the rise times of VFTs. Therefore, these arresters cannot suppress the wave steepness and find it difficult to prevent the switching transients with steep fronts [30]. Generally, capacitors in the substation tend to reduce the steepness of the surges and smooth out the fast changes in the voltage. So the addition of cable and CVTs in the system are suggested to reduce the steepness of the incoming current surges and thereby enhance the protection afforded to the connected equipment.

B. Addition of Cable and CVT

The voltage distribution of the arrester is analyzed with the inclusion of cable and CVT, in the system selected as shown in Fig. 6(a) and (b).

Cable with different lengths of 5 to 30 m is tried for reducing the steepness of the current surge. Not much improvement is found for the length above 10 m. This inference is also supported by Cornick *et al.* [31]. They state that the wavefront duration of the VFT is decreased by the presence of short cables only. It remains the same irrespective of the cable length. The capacitance for the 10-m cable is 1.4 nF (0.14 μF/km). The typical capacitance value for the 230-kV class CVT lies between 3 to 12 nF. The 8.8-nF CVTs are generally employed in 230-kV network for the purpose of relay protection, voltage measurement, and carrier communication. Hence, the CVT capacitance has been taken as 8.8 nF in the present study. After placing the cable and CVT, the voltage across the top unit of the arrester is computed for different current surges and is tabulated in Table VIII. It is observed that the voltage across the top unit is reduced, after placing cable and CVT in the circuit. Thus, the risk faced by the arrester is brought down.

From the aforementioned analysis, it is concluded that by using the ZnO arrester element manufactured with new additives, it is possible to make the arrester with reduced heights. This will lead to the reduction in the stray capacitance and

TABLE VIII
PEAK VALUE OF VOLTAGE ACROSS THE TOP UNIT
OF THE ARRESTER WITH CABLE AND CVT

In 230kV System	Current surge with peak 10kA	
	0.01/10μs	0.005/10μs
Arrester with one grading ring	222.70	224.60
+Cable	220.10	221.10
+CVT	216.90	217.30
+Cable + CVT	215.10	216.90

nonuniform voltage distribution. In addition, it is possible to decrease the voltage stress faced by the top unit of the arrester.

VI. DISCUSSIONS

The stray capacitance is responsible for the nonuniform voltage distribution across the arrester. This nonuniformity increases with the voltage rating (height) of the arrester and with the steepness of the current surges since capacitance plays a major role under VFTs. In order to model the arrester for VFTs, the arrester capacitances are computed accurately using FEM. An arrester rating of 198 kV is chosen for voltage distribution studies which involves the conduction of surges with different front times (from the microsecond to nanosecond level) and under power frequency conditions.

The arrester assembly is modeled with accurately calculated capacitance values. The total block capacitance value of the 198-kV arrester is found to be 15 pF. The total stray capacitance values without and with two grading rings are 6.78 and 4.11 pF, respectively. The residual voltages are simulated using EMTP for different current surges. The peak value of residual voltage increases with steepness of the current surges. The percentage error noticed between experimental and simulated values exhibits good accuracy of the arrester model. The measured residual voltages at the three metal flanges of the arrester in point portray that the top-most unit (stack) of the arrester faces higher voltage stress under VFT and normal power frequency conditions. The provision of grading rings reduces nonuniformity of voltage distribution (Table VIII). Thus, the effect of grading rings on voltage distribution is proved.

Because of the limitation on arresters' height for higher voltage rating, adding a grading ring alone is not sufficient. So arrester elements with new additives are tried for the given voltage rating. The performance of arrester elements is found by reducing the formation of a spinel particle with new high gradient ZnO elements and an optimum firing process. The results obtained are found to be encouraging. The spinel-reduced element has a larger capacitance than normal elements, which is attributed due to the wide conducting paths through the boundaries. This gives an advantage in the voltage distribution of the complete arrester. Moreover, with HGM, height is reduced for the given arrester rating with a corresponding reduction in the stray capacitance. This study shows that the voltage across the top unit is reduced from 232.80 to 219.20 kV_p for a current surge with a front time of 5 ns. This confirms

the reduction in the voltage stress experienced by the top unit of the arrester with HGM. Further, it is observed that the steepness of the incoming current surge is reduced by locating a cable (10 m) and CVT (8.8 nF) in the system. After placing the cable and CVT in the given system, the voltage across the top unit of the arrester (with one grading ring) is reduced from 224.60 to 216.90 kV_p for current surge with a front time of 5 ns. The nonuniformity of the voltage faced by the top unit is also found to decrease with the reduced steepness of the current surge. Thus, the study results validate and confirm the usefulness of the CVT and cable in moderating the front times of invading current surges.

VII. CONCLUSIONS

The voltage distribution studies are conducted on metal–oxide arrester during its conduction mode. The residual voltages at different metal flanges are also computed and it is found that there is higher voltage stress across the top-most unit of the arrester, which increases with the height of the arrester and steepness of the applied current surge as well. The higher stress faced by the top-most unit of the arrester is reduced by using high gradient arrester material and by reducing the steepness of the incoming current surge. The steepness of the current surge is reduced by placing cable and CVT in the system. Using the aforementioned methods, the voltage distribution along the arrester column is made more uniform and so the lifetime of the arrester is enhanced.

The stray capacitance effect is widely experienced in EHV networks and the steepness of the incoming current surges is to be decreased in order to obtain more uniform voltage distribution across the arresters. This will help to improve the lifespan of the metal–oxide arrester. Based on this research work, the metal–oxide arrester can be designed for VFTO applications with an enhanced lifespan.

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