High Performance 14nm FinFET Technology for Low Power Mobile RF Application

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Abstract

RF-CMOS process employing 14nm FinFET technology is introduced for the first time and its RF performance is characterized. Compared with its 28nm planar counterpart, the optimized 14nm RF FinFET consumes 63% of DC power with 53% of device active area and 3.8 times higher intrinsic gain (gm/gds). Based on the 14 nm technology, VNCAP with higher cap density (8%) and Q-factor (23%) is also verified for mobile RF application.

Keywords: FinFETs, current gain cutoff frequency, intrinsic gain, power consumption, gate resistance, VNCAP

Introduction

Scaling of RF SoC CMOS technology has traditionally been driven by planar digital logic in tech nodes down to 20nm with high-k, metal gate, and strain engineering [1]. However, planar devices below 20nm have limitations in logic characteristics due to their short channel effect as well as their negative impact on RF performance (Table I)[2]. We have recently been addressing these market needs with state-of-the-art 14nm FinFET technology. In this paper, it will be presented that RF FinFET and VNCAP using the said 14nm technology are verified to be superior for mobile RF applications compared with 28nm planar counterpart.

Characteristic of 14nm FinFET RF performance

RF performance of the 14nm FinFET is compared to that of 28nm planar, typical RF FET in Fig. 1. The analog parameters' bias condition is at overdrive ($V_{ov}=V_{gs}-V_{th}$ =0.2V), which is ideal for low power analog/RF designs as a good compromise between speed and power consumption [3]. At Vov=0.2V bias condition, the current gain cut-off frequency(f_T) of 14nm FET is 252 GHz and 10% higher than that of 28nm FET as shown in Fig. 2(a), in spite of the higher parasitic capacitance. Figure 2(b) shows that one of the main reasons for the higher f_T is g_m, attributed to the shorter gate length. Especially, g_{ds} is 62% lower compared to 28nm devices. This result is mainly due to fully depleted fins [3]. As Fig. 3 shows, the intrinsic gain (g_m/g_{ds}) of 14nm FinFET is 3.8 times higher than that of 28nm and consumes 37% less DC power than 28nm RF FET at the maximum f_T. Taking into consideration the 3-dimensional structure, 14nm FinFET has much superior layout area effectiveness (-47%), compared to 28nm palnar device from the perspective of footprint width.

For maximum oscillation frequency(f_{MAX}), it is especially crucial in the 14nm FinFET design to minimize parasitic elements, because it has intrinsically higher gate resistance caused by narrow gate length and additional width from the 3-D structure [4, 5]. Due to the effect of vertical resistance as shown in Fig. 4, 14nm FinFET shows a gate resistance trend that is different from the conventional planar devices (Fig. 5). The gate resistance of FinFET decreases as the fin number is increased from 2 to 8, which is contrary to the behavior displayed by planar devices. This fact should be carefully considered for chip design to minimize the parasitic elements and overcome the weakness of FinFETs. For example, the f_{MAX} is improved by 43% when designed with 8 fins, compared to 16 fins, because of the difference in the gate resistance. Additionally, the differences in f_{MAX} and gate resistance between gate double side and single side are also verified, as shown in Fig. 6(a). The f_{MAX} with gate double side is 51% higher than that with gate single side because the former has lower gate resistance than the latter as described in Fig. 6(b).

Furthermore, high quality VNCAP based on the 14 nm technology is analyzed against conventional devices, whose layouts are captured in Fig. 7. Figure 8 shows that VNCAP with 14nm technology has 8% higher unit capacitance because of the 14nm technology's more advanced and superior fabrication capability. In addition, Fig. 9 shows that vias on the fingers of the VNCAP with 14 nm technology induce the Q-factor improvement of as much as 23% at 10 GHz. With adoption of VNCAP with the high unit capacitance and Q-factor, RF mobile chips are successfully designed and operated (Fig. 10) [6].

Conclusion

For low power RF mobile applications, higher intrinsic gain (3.8x), less DC power consumption (-37%), and competitiveness in layout area (-47%) are among the strong advantages offered by the 14nm FinFETs compared to the 28nm planar counterparts. However, the gate resistance should be carefully considered to minimize the parasitic elements, keeping in mind the new gate resistance trend with respect to the number of fins. To provide high quality passive devices, VNCAP with high capacitance (8%) and Q-factor (23%) are also verified. Finally, RF mobile chips are successfully designed and operated employing the aforementioned high quality RFFET and VNCAP with 14 nm technology.

References

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TABLE I
RF CMOS FOM COMPARISION

	FinFET	Planar device
f_T	↑	↑
f_{MAX}	↓	↑
Power Consumption	↑	↓
Chip Area	↑	↓

* Superiority (↑), inferiority (↓)

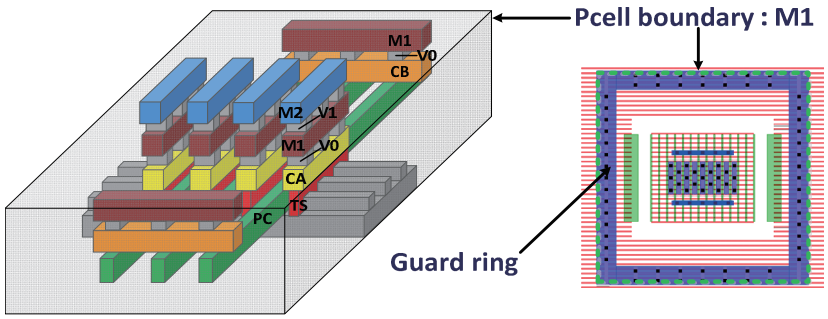

Fig. 1 The structure and pcell layout of 14nm FinFET with pcell boundary and guard ring

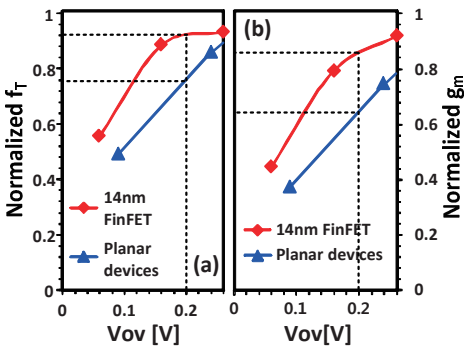

Fig. 2 (a) f_T and (b) g_m versus overdrive voltage for 14nm FinFETs and planar devices

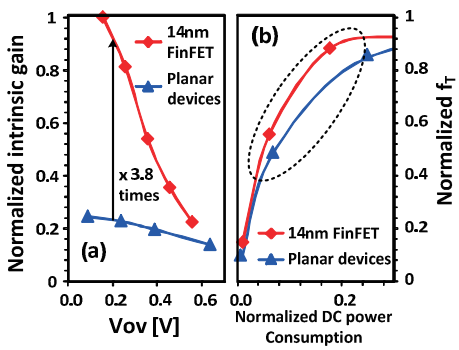

Fig. 3 (a) Intrinsic gain (g_m/g_{ds}) versus overdrive voltage, (b) DC power consumption versus f_T

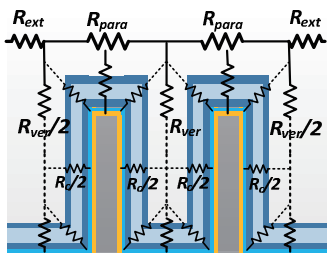

Fig. 4 The schematic of the parasitic resistance of 14nm FinFET

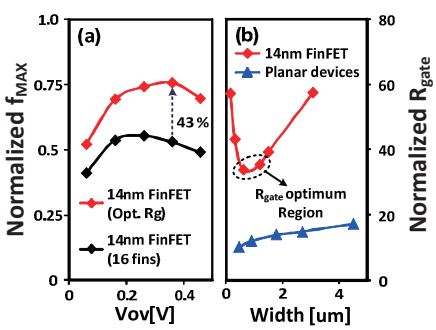

Fig. 5 (a) The f_{MAX} and (b) the gate resistance, as a function of fins for 14nm FinFETs and planar devices

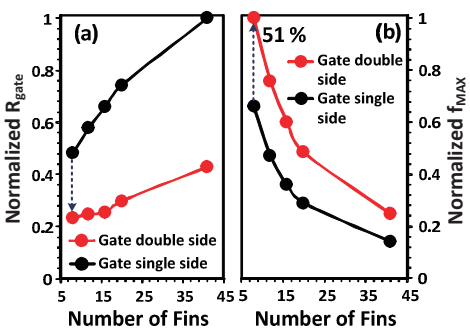

Fig. 6 (a) The gate resistance and (b) f_{MAX} versus number of fins for gate double side and gate single side

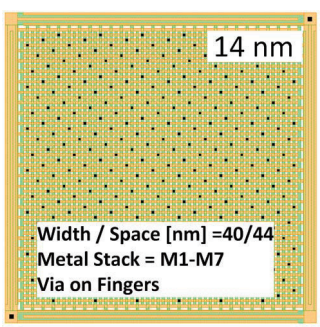

Fig. 7 The layout of VNCAP for 14nm Technology

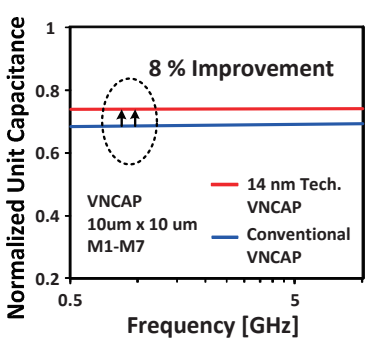

Fig. 8 Comparison of unit capacitance between 14nm technology and Conventional VNCAP

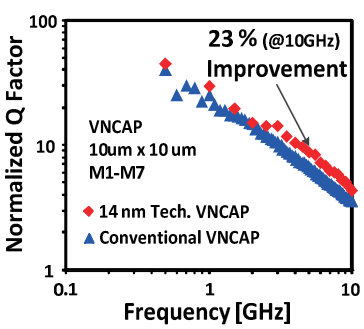

Fig. 9 Comparison of Q-factor between 14nm technology and Conventional VNCAP

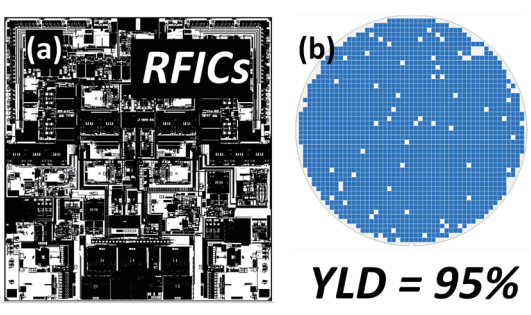

Fig.10 (a) The RF mobile chip and (b) yield of the product in 14nm FinFET Technology