Analysis and Comparison of Leakage Power Reduction Techniques in CMOS circuits

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***Abstract*—This paper compares various leakage reduction techniques including Multi-threshold CMOS, Super-Cutoff CMOS, Zigzag, Stack Effect, Input Vector Control, LECTOR, Sleepy Stack, Sleepy Keeper, VCLEARIT, GALEOR, Dual Sleep, Sleepy-Pass Gate and Transistor Gating. The paper elaborately explores the working, comparison and analysis of all these techniques in different CMOS technologies. Leakage Power is analyzed during the standby mode of operation. It has been observed that for a particular circuit leakage depends on CMOS technology as well as leakage reduction technique. In this paper, wide range of results for leakage power reduction techniques of CMOS technologies from 180nm to 45nm is covered which will be helpful for further research in this area.**

Key Words- *Sleep approach, Leakage reduction, MTCMOS, SSCMOS, GALEOR and Sleepy Pass Gate.*

I. INTRODUCTION

VLSI industry had already implemented various leakage power reduction techniques at different levels of design abstraction like introduction of sleep transistors, clock gating, self gating flip flops and latches, pipelining, operator reduction etc for high performance chips [1]. However, leakage current is still a big challenge before this industry. In deep-submicron CMOS technology, the impact of subthreshold leakage current is maximum [2].The following equation relates subthreshold current with other device parameters [3]:

$$I_{SUB} = I_0 e^{\frac{V_{gs} - V_{th0} - \eta V_{ds} - \gamma V_{sb}}{nV_\theta}} \left(1 - e^{\frac{-V_{ds}}{V_\theta}}\right) \quad (1)$$

Where,

$$I_0 = \mu C_{ox} \left(\frac{W}{L}\right) V_\theta^2 e^{1.8} \quad (2)$$

$$V_\theta = \frac{kT}{q} \quad (3)$$

V_θ is thermal voltage,
W and L are the width and length of the transistor,
μ denotes carrier mobility,
η is the Drain Induced Barrier Lowering Coefficient (DIBL),
n is the slope shape factor/subthreshold swing coefficient,
γ is the Body-bias effect coefficient

Techniques for leakage power reduction can be grouped into two categories: (i) state-destructive techniques where the current boolean output value of the circuit might be lost and (ii) state-saving techniques where circuit state is retained [4].

Multi-threshold CMOS (MTCMOS) technique, introduced in 1995, is one of the state destructive technique in which sleep transistors are introduced with high threshold voltage to control leakage power [5] . Super-cutoff CMOS (SSCMOS) instead, lowers the standby current and increases speed by introducing sleep transistors with lower threshold voltage and overdriving the gate of cut-off MOSFET [6]. Zigzag technique introduced in 2003 reduces the wake up overhead of the sleep transistors [7]. Another state destructive technique named Transistor Gating was introduced in 2013 [8].

In 2001, Narendra et. Al. stacked MOSFETs and found that stacking of two *off* devices has lower leakage current than one *off* device [9]. Input Vector Control (IVC) [10] determines the input vector for the standby mode of operation to reduce the leakage current. LECTOR [11] for leakage reduction introduce the stacking effect in the path of supply voltage to ground. In 2005, Park introduces Sleepy Stack technique by combining the transistor stacking and sleep transistor techniques to further lower down the leakage power [12]. Sleepy Keeper approach uses sleep transistors with additional MOSFETS to save logic state [13]. In VCLEARIT a combination of high threshold voltage and standard threshold voltage sleep transistors are used as a circuitry in the CMOS design to reduce the leakage current [14]. GALEOR again retains the circuit state in the standby mode. This technique introduces the high threshold voltage sleep transistors in the design to reduce the leakage current [15]. Dual Sleep method [16], introduce in 2010, uses sleep transistors and PMOS and NMOS transistor as a common circuitry to reduce the leakage power as well as area as compared to other leakage techniques. Sleepy-pass gate is another leakage reducing technique [17] using two pass gate transistors. In 2013, Hybrid techniques are also introduced combining MTCMOS and stacking effect as well SSMOS and stacking effect [18].

Contribution: Our paper contributes the compiled data of almost all standby leakage reduction techniques with analysis and comparison amongst themselves.

Organization of Paper: In section II we have described the behavior of CMOS circuits for all these techniques elaborately. In section III simulation results, carried on Cadence Virtuoso tool, of various techniques are analyzed on various parameters like *Average Power*, *Static Power* and *Propagation Delay.* Simulation results of leakage reduction techniques carried by different authors are also mentioned. Graphs comparing among different leakage reduction techniques with respect to two parameters – leakage and delay are shown. Concluding remarks are given in section IV.

II. LEAKAGE REDUCTION TECHNIQUES

A. State-Destructive Techniques

In these techniques, power gating is used to control the leakage power in which power supply is removed during standby mode and it is resumed during the active mode of operation.

1) Multi-threshold CMOS: The multithreshold-voltage CMOS circuit was proposed by inserting high threshold devices in series into low-Vth circuitry [5].

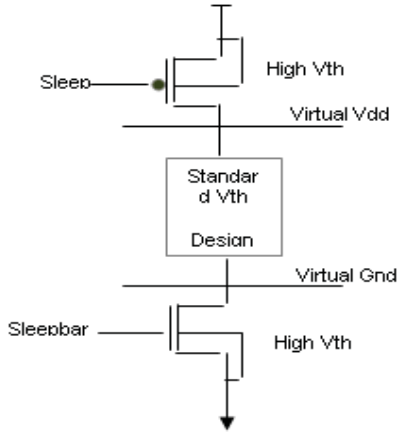

Fig. 1. MTCMOS

Figure 1. shows the MTCMOS technique in which lower threshold voltage devices increases the performance of the circuit while the high threshold voltage sleep transistors decreases the standby current of the circuit. The power terminals of the standard design is not connected directly to the supply but to virtual Vdd and virtual Gnd. During the active mode sleep signal is *off (*sleepbar is *on)* and the circuit operates normally. During the standby mode, sleep signal is *on (*sleepbar is *off)*thus both the sleep control transistors are *off* the design is cut-off from the power supply. Since sleep transistors are high threshold voltage transistors, the leakage current is reduced.

There is a performance degradation associated with the sleep transistor insertion. This is due to the IR drop across the MTCMOS cells in the active mode of operation. Larger the

sleep transistors, lower is the performance degradation and larger is the area. However the power consumption will increase with the size of the sleep transistors. Therefor there is a trade-off between the amount of the performance degradation and the size of the sleep transistors in the MTCMOS circuit [19]. Currently a lot of analysis is being done on optimum transistor sizing of sleep transistors. This technique is also called as SLEEP approach.

2) Super-Cutoff CMOS: SCCMOS scheme [6] is proposed to achieve high-speed and low stand-by current. By overdriving or under driving the gate of a cut-off MOSFET, the SCCMOS suppresses leakage current in a stand-by mode while high-speed operation in an active mode is possible with low-threshold voltage. Figure 2 shows the SSCMOS technique which is similar to MTCMOS instead of the low threshold voltage sleep transistors as compared to high threshold voltage sleep transistors in MTCMOS. The sleep (sleepbar) signal is overdriven or under driven to as to super cut-off the sleep transistors during standby mode thus reducing the leakage current. This has the advantage of have single threshold voltage devices in the design as compared to MTCMOS technique having two threshold voltages in the design. Circuit delay still increases due to the increased circuitry in the active mode.

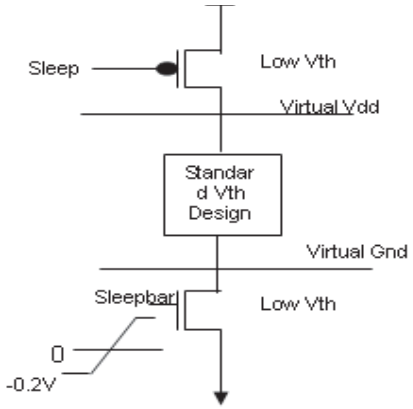

Fig. 2. SSCMOS

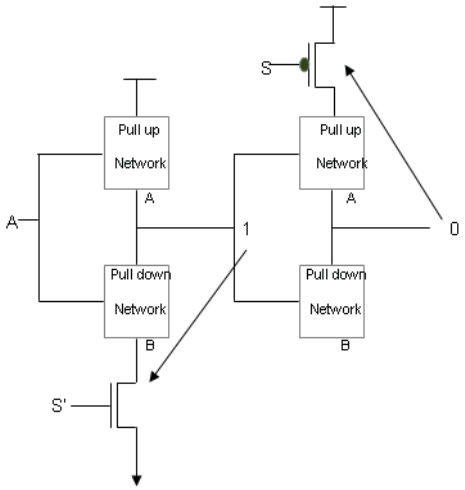

Fig. 3. Zigzag Technique

3) Zigzag: The zigzag technique [7] reduces the wake-up overhead of sleep transistors. This technique chooses a particular circuit state and then for that particular state, turning off the pull-down network for each gate whose output is high while turning-off the pull-up network for those gate whose output is low. Although the zigzag technique retains the particular state chosen prior to chip fabrication, any other arbitrary state chosen during regular operation is lost in power-down mode. Also, zigzag technique may need extra circuitry to generate a specific input vector.

Figure 3 shows the zigzag technique. Input A is applied during standby mode due to which the output values are shown in figure. A pull-down sleep transistor is applied for output value '1' and a pull-up sleep transistor is applied for output value '0' [12].

4) Dual Threshold CMOS: Dual Threshold CMOS (DTCMOS) or Dual V_t CMOS effectively reduces the subthreshold leakage power by assigning higher threshold voltage to the transistors in non-critical paths , while the performance is maintained due to the use of low threshold transistors in the critical path(s) [3].

5) Transistor Gating: This technique [8] introduce PMOS sleep transistor between pull up network and pull down network while an NMOS sleep transistor between pull down network and ground. In Figure 4 during active mode, signal s is low (s' is high) turning on both the sleep transistors and normal operation of the circuit. During standby mode, signal s is high (s' is low) turning off both the sleep transistors creating a high impedance path from supply voltage to ground thus reducing the leakage power. When a full subtracter circuit is simulated in 45 nm CMOS technology, this technique reduces the leakage power by 24.38% [8].

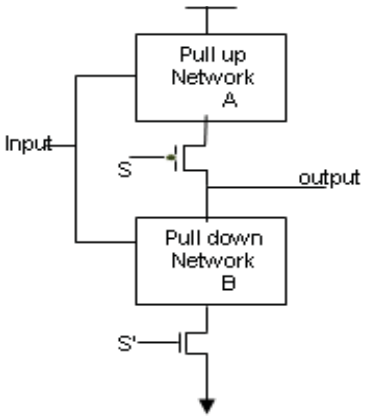

Fig. 4. Transistor Gating Technique

In MTCMOS, SSCMOS and Zigzag there is speed degradation due to the introduction of sleep transistors in the switching mode of operation. Also, a hardware circuitry is required to find out the standby and active/switching mode of operation in the circuit. This extra hardware also consumes area, power and cost of the circuit. In all the techniques including Dual threshold voltages, the fabrication process is complex [11].

B. State-Preserving Techniques

1) Transistor Stacking: Stack effect is the phenomenon, where leakage current decreases due to two or more series transistors that are off [9]. In some circuits Transistor Stacking already exist such as NAND gate. As the depth of the stack is increased, higher leakage power saving is observed. In some circuits, natural stacking does not exist and to utilize the stack effect *force stacking* is done by replacing a single transistor of width W by two transistors in series each of width W/2. Figure 5. shows the NMOS transistor stacking in CMOS inverter.

Stack effect factor (X) is the ratio of leakage current in one *off* device to the leakage current in a stack of two or more *off* devices.

Authors in [12] had derived the stack effect factor as:

$$X = \frac{I_{sub0}}{I_{sub1}\left(=I_{sub2}\right)} = e^{\frac{V_x}{nV_\theta}(1+\gamma+\eta)} \quad (4)$$

where, $V_{\theta,}$ η, n, and γ have the same meaning as mentioned earlier. Isub0 and Isub1 are the sub-threshold leakage currents in M0 and M1 respectively.

As an example, let 'In' is 0, then M1 and M2 both are in *off* state. Due to the internal resistance of M2, the intermediate node *Vx* is higher than *Gnd.* Due to the positive potential of Vx following points are observed:

I. *Vgs*, gate-to-source voltage of M1 is negative. From the equation of sub-threshold leakage current it is clear that the negative gate-to-source voltage decreases the sub-threshold current.

II. *Vsb,* source-to-body voltage of M1 is positive. As Vsb is increased, the threshold voltage is increased, which in turn decreases the sub-threshold current.

III. *Vds*, drain-to source voltage of M1 is reduced, which degrades Drain Induced Barrier Lowering effect (since reduced DIBL increases the threshold voltage which again decreases the subthreshold current due to the reason mentioned in point 2).

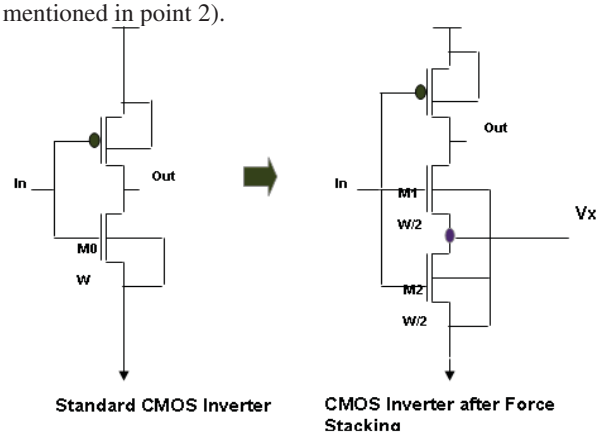

Fig. 5. Transistor Stacking

Because of all the above points, the leakage reduction factor is changed reducing the leakage current.

2) Input Vector Control: Leakage current depends on the Input combination of the circuit. It has been found in the transistor stacking effect that the leakage current decreases due to two or more off transistors that are stacked. Input Vector Control (IVC)is a technique in which input vector is determined to reduce the leakage current when the circuit is in standby mode. The main aim is to find the input pattern which maximizes the number of off transistors in all the stacks in the circuit. This pattern is then used to drive the circuit in standby mode [10]. For example [3] a 3-input NAND gate has the minimum leakage power when the input combination is (0,0,0). Thus the circuit will be provided with this input vector in standby mode. Few algorithms to generating the input vector combination for minimum leakage can be found in [10] and [21].

3) LECTOR: This technique [11] is based on the observation that "a state with more than one transistor off in a path from supply voltage to ground is far less leaky than a state with only one transistor off in any supply to ground path". So, in order to ensure that there are more than one off transistors in the path of supply voltage and ground, Leakage Control Transistors (LCTs) are included in the path of supply voltage and ground as shown in Figure 6.

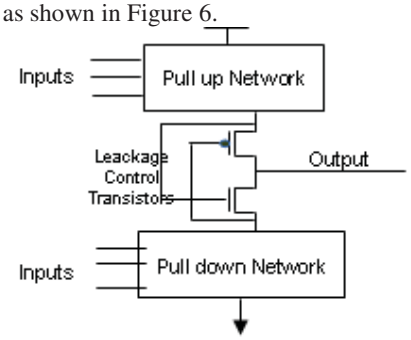

Fig. 6. LECTOR

The gate of PMOS LCT is connected to the drain of pull down network while the gate of NMOS LCT is connected to the drain of the pull up network. With this wiring, with any input combination during standby mode one of the two LCTs is always near its cut-off region. This increases the resistance of the path from supply voltage to ground thus reducing the leakage power.

LECTOR technique of reducing the leakage power adds an extra circuitry as compared to the conventional design which reduces the performance of the circuit. Thus the sizing of the LCTs have to be done optimally so as to meet the performance.

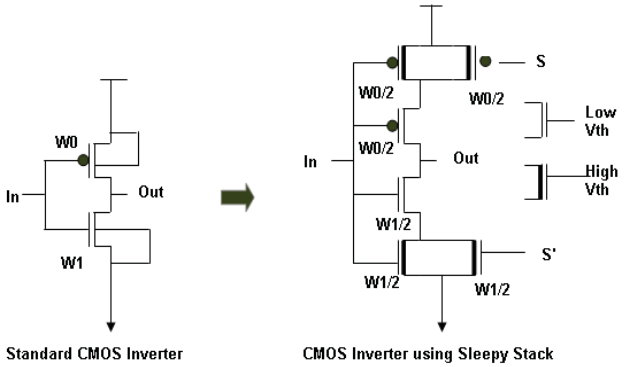

Fig. 7. Sleepy Stack

4) Sleepy Stack: This technique was introduced by Park in 2005 [12]. The sleepy stack technique has a combined structure of forced stack technique and sleep transistor technique. However, unlike sleep transistor technique, the sleepy stack technique retains exact logic state and unlike the forced stack technique, the sleepy stack technique can utilize high-Vth transistors without delay penalties.

In order to use sleepy stack technique, for example in standard CMOS inverter (Figure 7.), first force stacking technique is applied by replacing the transistor with two or more series transistors. Then, sleep transistor is added in parallel to one of the stacked transistors.

Figure 8. shows the working of sleepy stack circuit during active mode and during standby mode of operation. During the active mode, sleep transistors are *on* (sleep signal S='0'), thereby reducing the resistance of the path due to the presence of two parallel transistors. Thus the propagation delay is reduced during the active mode. During the stand-by mode (sleep signal S='1'), sleep transistors are *off* and the leakage is suppressed due to the transistor stacking effect as explained previously.

The main disadvantage of this approach is that each transistor in the original is replaced by three transistors in the sleepy stack equivalent [13].

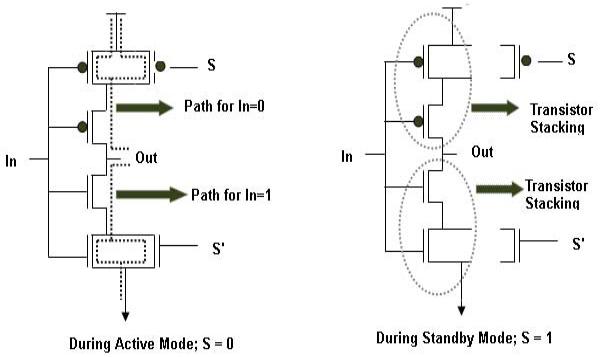

Fig. 8. Working of Sleepy stack

5) Sleepy Keeper: This approach [13] uses the benefits of sleepy stack approach without large area overhead. In this technique an NMOS transistor is placed parallel to the pull-up sleep transistor, while a PMOS transistor is placed parallel to the pull-down sleep transistor.

Sleepy Keeper achieves less delay and area than sleepy stack technique. However, the dynamic power consumption is increased as compared to sleepy stack technique. Figure 9. explains the working of Sleepy Keeper circuit. First part of the figure shows the sleepy keeper circuit in part (a) in active mode. It can be seen that in sleepy keeper circuit two sleep transistors are added and two transistors, known as *keeper* transistors, each parallel to the sleep transistor is added. During active mode (Figure 9(a)), sleep transistors are *on* (S='1') reducing the delay while during standby mode or sleep mode (Figure 9(b) and (c)), sleep transistors are *off* (S='0') and keeper transistors are used to save the state of the circuit. Here, high threshold voltages may be applied in the sleep as well as keeper transistors to further reduce the leakage.

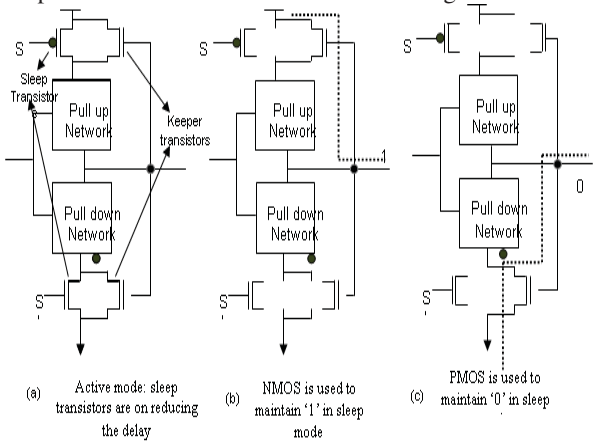

Fig. 9. Working of Sleepy Keeper

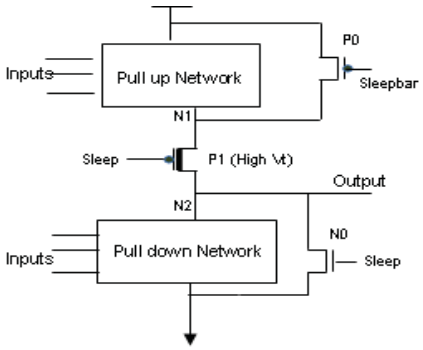

Fig. 10. VCLEARIT

6) VCLEARIT: This technique [14] (VLSI CMOS Leakage Reduction Technique) as shown in Figure 10 introduced the combination of one high Vt sleep transistor (P1) and two standard Vt sleep transistors (P0 and N0). In the circuit, sleep signal is '0' during active mode and '1' during standby mode. During active mode, P1 is on P0 and N0 are off. Thus the circuit operates as a conventional design. During standby mode, P1 is off and P0 and N0 are on, node N1 is connected to supply voltage and node N2 is connected to ground. Thus, the pull up network is connected across the same supply voltage and pull down network is connected across the same ground voltage thus reducing the leakage power. P1 is the leaky transistor in the design which needs to be sized appropriately match the performance with that of conventional CMOS design.

7) GALEOR: This technique [15] introduced the Gated Leakage Transistors in the CMOS design. Figure 11. describes the connection of high threshold voltage Gated Leakage Transistors. The PMOS and NMOS transistors in pull up network and pull down network have standard threshold voltages. Due to the node voltages of N1 and N2, each or both of the leakage transistors during standby mode forms transistor stacking with the a part of the design thereby reducing the leakage current. Due to the Gated Leakage transistors, there is a threshold voltage loss which reduces the voltage swing of the circuit. The propagation delay of the circuit is also increased.

Authors in [20] has combined the transistor stacking and GALEOR techniques to form a new leakage reduction technique called *Galeorstack.*

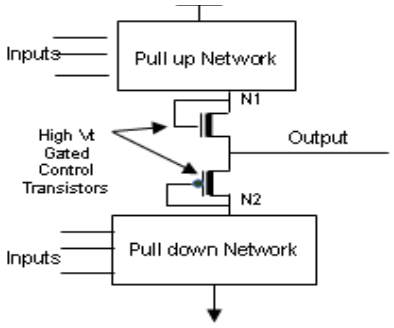

Fig. 11. *GALEOR Technique*

8) Dual Sleep: In dual sleep method [16] two sleep transistors in each NMOS or PMOS block are used. . Dual sleep approach uses the advantage of using the two extra pull-up and two extra pull- down transistors in sleep mode either in OFF state or in ON state. Since Dual Sleep portion is common in the circuitry therefore less number of transistors are required.

Figure 12(a). shows the dual sleep circuit. In part (b) during active mode, S=1, pull down NMOS transistor is ON and the pull-up PMOS transistor is ON. So the arrangement works as a normal device. In Figure 12(c), during standby mode state S forced to 0 and hence the pull down NMOS transistor is OFF and PMOS transistor is ON and the pull-up PMOS transistor is OFF while NMOS transistor is ON. So in standby mode or sleep mode, PMOS is in series with an NMOS both in pull-up and pull-down circuits which is liable to reduce power.

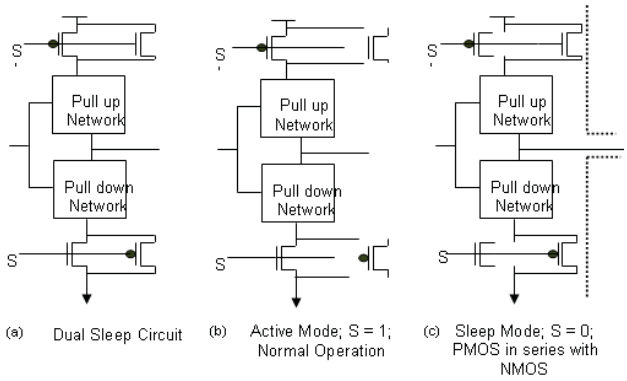

Fig. 12. Working of Dual Sleep Approach

9) Sleepy-Pass Gate Technique: This technique [17] increases the resistance of the path from supply voltage to ground in the standby mode thereby reducing the leakage power. Figure 13. shows the Sleepy-Pass Technique in which two high threshold pass-transistors (PMOS and NMOS) are connected. Sleep signal is '1' for active mode and both the sleep-pass transistors are on allowing normal operation of the circuit. During standby mode sleep signal is '0' and both the sleep-pass transistors are off . Because of the increased resistance, due to sleepy-pass transistors, leakage current is reduced. Its disadvantage is that during the standby mode, output high state will be saved, but output low state can be lost due to its disconnection from ground.

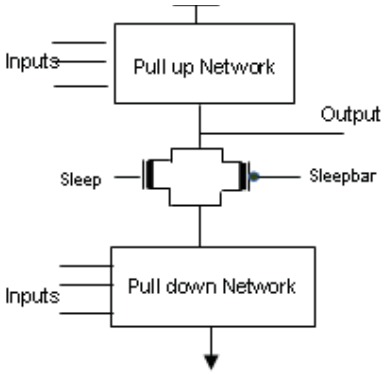

Fig. 13. Sleepy-Pass Gate Technique

10) Hybrid Techniques: Authors in [18] have combined the MTCMOS and transistor stacking techniques as well as SSCMOS and transistor stacking techniques to form four new techniques namely hybrid MTCMOS complete stack technique, hybrid MTCMOS partial stack technique, hybrid super cutoff complete stack technique and hybrid super cutoff partial stack technique, for the reduction of subthreshold leakage power dissipation in standby modes.

III. SIMULATION RESULTS AND ANALYSIS

CMOS inverter is chosen as the base inverter with the width of PMOS is twice the width of NMOS transistor. This is done in order to have the switching threshold Vm to be located around the middle of the available voltage swing (or at Vdd/2). All other circuits are sized according to the base inverter. The simulation results are carried on Cadence Virtuoso tool on 180nm technology. Static Power is calculated during standby mode of operation i.e. assuming that the circuit is idle and than calculating the static power for input = '1' and input = '0'. Static power is calculated for time period of 200ns. Dynamic power is calculated while giving an input pulse to the circuit for 200ns. Results with respect to static, dynamic power and propagation delay are shown in Table I, II, III and IV. Table I shows the Static power of CMOS inverter at 180nm. It can be seen that there is significant reduction in leakage power in different leakage reduction techniques when the input is '0' during standby mode. This is due to the reduction in sub-threshold leakage current (drain current when the gate-to-source voltage is below the threshold voltage). Here, SSCMOS with dual threshold voltage (high threshold voltage sleep transistors and standard threshold voltage design) reduces the maximum leakage power.

Table II shows the propagation delay of the CMOS inverter at 180nm. The propagation delay of the leakage reduction techniques increases with respect to base circuit due to the circuitry introduced in the design to reduce the leakage power.

Table III show the compiled data of static power, dynamic power and propagation delay of the CMOS inverter at 180nm. The comparison of different leakage reduction techniques with respect to base circuit is shown in Table IV.

In Table V and VI results of 1 bit adder at 180nm for various leakage reduction technologies are given [13]. Results shows the maximum reduction in MTCMOS leakage reduction technique with a delay penalty due to two additional series transistors. PDP (*Power-Delay Product)* values (not shown) shows that SSCMOS technique is more efficient than MTCMOS technique. This is due to the slight overdriven (underdriven for NMOS) values of sleep transistors during standby mode to reduce leakage current. On the other hand, Table VII and VIII describe the results of 1 bit adder at 70 nm [13]. Results of 1-bit adder at 180nm and 70nm prove that the leakage power increases as the technology is lowered.

In Table IX we have compiled the results of 2 input NAND gate for LECTOR, VCLEARIT, Sleepy-pass Gate and GALEOR techniques. Here, Sleepy-Pass gate technique reduces the maximum leakage power with respect to the base circuit at 100nm.Table X describes results of 2 input AND gate at 65nm technology for new Hybrid technologies along with traditional technologies for leakage power reduction.

TABLE I. Static Power of CMOS Inverter at 180nm

Technique	*Static Power (pW)*	
	Input = 0	*Input = 1*
Base Case	26.72	4.59
MTCMOS	1.98	5.82
Transistor Stacking (NMOS and PMOS both)	5.24	0.26
Sleepy Stack	7.88	6.02
Sleepy Keeper	2.08	5.81

Technique	*Static Power (pW)*	
	Input = 0	*Input = 1*
Dual Sleep	5.73	0.336
Sleepy Stack (Dual Vth)	5.32	6.11
Dual Sleep (Dual Vth)	5.32	6.09
SSCMOS (Dual Vth)	0.023	0.49

TABLE II. Propagation Delay of CMOS Inverter at 180nm

Technique	*Delay (ps)*	
	tphl	*tplh*
Base Case	17.98	22.06
MTCMOS	27.32	30.61
Transistor Stacking (NMOS and PMOS both)	31.00	37.29
Sleepy Stack	24.00	28.84
Sleepy Keeper	35.90	41.77
Dual Sleep	24.94	29.96
Sleepy Stack (Dual Vth)	24.26	27.97
Dual Sleep (Dual Vth)	22.77	26.38
SSCMOS (Dual Vth)	27.27	30.17

TABLE III. Static Power, Dynamic Power and Delay of CMOS Inverter at 180nm

Technique	*Static Power (pW)*	*Dynamic Power (μW)*	*Delay (pS)*
Base Case	15.93	1.83	15.02
MTCMOS	3.90	2.33	28.97
Transistor Stacking (NMOS and PMOS both)	2.75	2.90	34.15
Sleepy Stack	6.95	2.39	26.42
Sleepy Keeper	3.94	3.43	38.84
Dual Sleep	3.03	2.31	32.45
Sleepy Stack (Dual Vth)	5.71	2.33	26.12
Dual Sleep (Dual Vth)	5.71	2.22	24.58
SSCMOS (Dual Vth)	0.25	2.326	28.72

TABLE IV. Comparison of Leakage reduction techniques with respect to Base Case – CMOS Inverter 180nm

Technique	*Static Power*	*Propagation Delay*
MTCMOS	-75.50%	+92.84%
Transistor Stacking (NMOS and PMOS both)	-82.73%	+127.33%
Sleepy Stack	-56.34%	+75.90%
Sleepy Keeper	-75.23%	+158.56%
Dual Sleep	-80.95%	+116.05%
Sleepy Stack (Dual Vth)	-64.10%	+73.87%
Dual Sleep (Dual Vth)	-64.16%	+63.62%
SSCMOS (Dual Vth)	-98.39%	+91.21%

TABLE V. Static Power, Dynamic Power and Delay of 1 bit adder at 180nm [3]

Technique	*Static Power (pW)*	*Dynamic Power (μW)*	*Delay (ps)*
Base Case	301.2	7.23	77.8
MTCMOS	4.55	7.16	88.9
SSCMOS	25.72	6.99	83.75
Transistor Stacking	206.98	7.35	79.72
Sleepy Stack	211.2	7.56	79.47
Input Vector Control	87.00	7.35	79.72

TABLE VI. Comparison of Leakage reduction techniques with respect to Base Case – 1-bit adder 180nm [3]

Technique	*Static Power*	*Propagation Delay*
MTCMOS	-98.49%	+14.27%
SSCMOS	-91.46%	+7.65%
Transistor Stacking	-31.28%	+2.47%
Sleepy Stack	-29.88%	+2.15%
Input Vector Control	- 71.12%	+2.47%

TABLE VII. Static Power, Dynamic Power and Delay of 1 bit adder at 70nm [13]

Technique	*Static Power (W)*	*Dynamic Power (W)*	*Delay (s)*
Base Case	8.90E-08	8.63E-06	3.76E-10
Sleep (MTCMOS)	1.36E-08	8.77E-06	5.38E-10
Zigzag	9.09E-09	8.37E-06	5.25E-10
Transistor Stacking	6.83E-09	7.41E-06	1.16E-09
Sleepy Stack	1.08E-08	7.39E-06	8.64E-10
Sleepy Keeper	1.30E-08	9.71E-06	5.90E-10
Sleep (Dual Vth)	3.65E-11	9.03E-06	7.52E-10
Zigzag (Dual Vth)	2.19E-11	8.46E-06	7.43E-10
Sleepy Stack (Dual Vth)	3.50E-11	7.06E-06	1.24E-09
Sleepy Keeper (Dual Vth)	3.89E-11	1.00E-05	8.30E-10

TABLE VIII. Comparison of Leakage Reduction techniques with respect to Base Case – 1-bit adder 70nm [13]

Technique	*Static Power*	*Delay*
Sleep (MTCMOS)	-84.72%	+43.09%
Zigzag	-89.79%	+39.63%
Transistor Stacking	-92.33%	+208.51%
Sleepy Stack	-87.87%	+129.79%
Sleepy Keeper	-85.39%	+56.91%
Sleep (Dual Vth)	-99.96%	+100.00%
Zigzag (Dual Vth)	-99.98%	+97.61%

Technique	*Static Power*	*Delay*
Sleep (MTCMOS)	-84.72%	+43.09%
Sleepy Stack (Dual Vth)	-99.96%	+229.79%
Sleepy Keeper (Dual Vth)	-99.96%	+120.74%

TABLE IX. Comparison of Leakage Reduction Techniques with respect to Base Case – 2 input NAND Gate
1,2 – [14] , 3 – [17], 4 - [15]

Technique	*Static Power*	*Delay*
LECTOR[1]	-28.89%	+38.88%
VCLEARIT[2]	-97.96%	+23.65%
Sleepy-Pass Gate[3]	-99.4%	+15.38%
GALEOR[4]	-52.00%	+50.00%

TABLE X. Simulation Results of Leakage Reduction Techniques for 2 input AND gate 65nm [18]

Technique	*Static Power (nW)*	*Dynamic Power (µW)*	*Delay pS*
MTCMOS	7.00	0.87	1.42
SSCMOS	5.00	0.78	21.2
Transistor Stacking	18.00	0.98	22.1
Sleepy Stack	19.00	1.12	18.7
Hybrid MTCMOS complete Stack	3.00	1.68	32.1
Hybrid MTCMOS partial Stack	3.40	1.45	19.1
Hybrid Super cut-off complete stack	2.00	1.52	4.12
Hybrid Super cut-off partial stack	2.45	1.36	3.18

Graphical representation with respect to Table IV, VI, VIII and IX are shown in Figures 14, 15, 16 and 17 respectively.

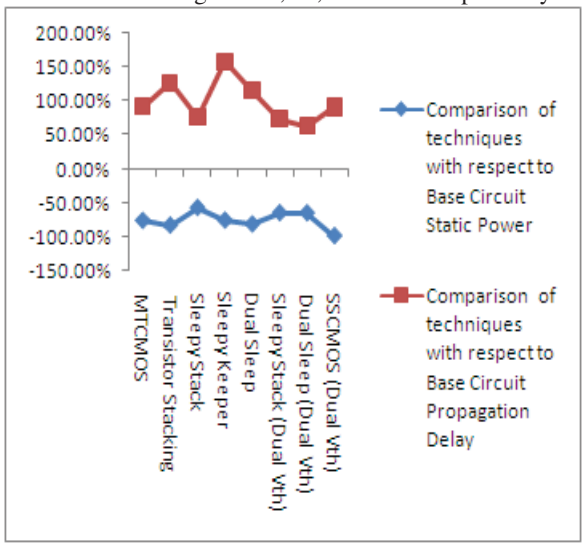

Fig. 14. Simulation Results of CMOS Inverter at 180nm

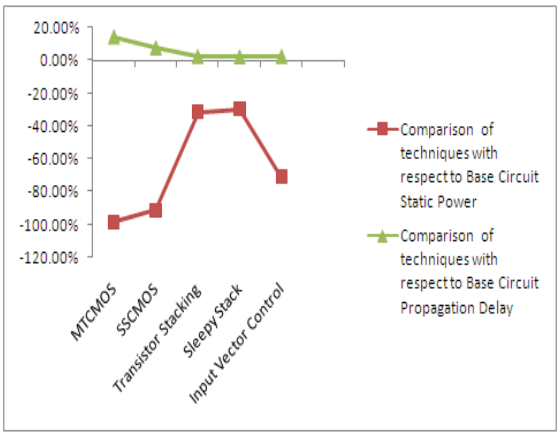

Fig. 15. Simulation Results of 1-bit adder at 180nm

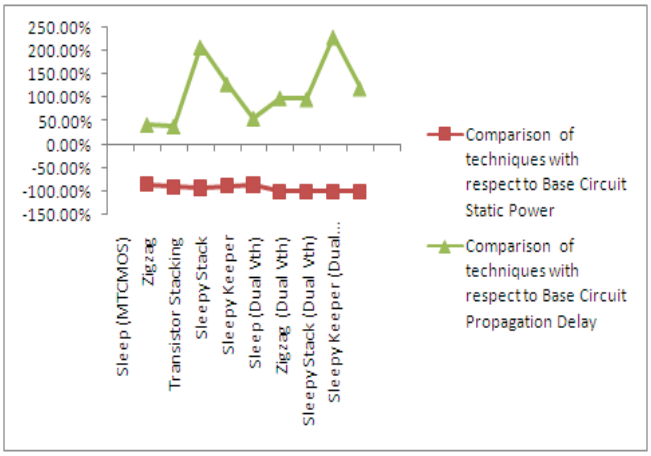

Fig. 16. Simulation Results of 1-bit adder at 70nm

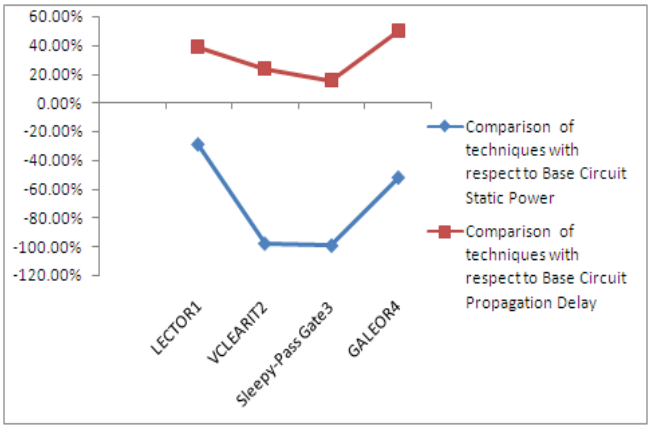

Fig. 17. Simulation Results of 2 Input NAND gate

IV. CONCLUSION

It is evident from the table and graph that there is appreciable reduction in leakage power in all the techniques as compared to base circuit. We can also see that as the technology is lowered, static power consumption is increased.

There is a power and performance trade-off evident from simulation result tables. We have found that in 180nm technology SSCMOS (dual) reduces the leakage power by 98.39% w.r.t. base inverter. For 1-bit adder circuit at 180nm technology MTCMOS technique reduces maximum power. At 100nm technology, for 2 input NAND gate Sleepy-Pass gate reduces 99.98% static power w.r.t. to base case. For 1-bit adder circuit at 70nm CMOS technology, Zigzag (dual Vth) reduces 99.98% of static power. At 65nm it is observed that Hybrid Super Cut-Off complete stack optimizes maximum static power in 2 input AND gate circuit. Research is still on in order to increase the performance of the circuit with the reduced static power consumption.

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