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New robust QCA D flip flop and memory structures

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ABSTRACT

Quantum dot Cellular Automata (QCA) is one of the candidate technologies to be replaced with CMOS. Using this technology, extra low power, extremely dense and very high speed structure is achieved. Since flip flops and memory cells are fundamental building blocks of digital circuits, constructing an efficient, dense, and simple QCA memory structure is of great importance. In this paper, using a robust 2:1 multiplexer, efficient level triggered and edge triggered QCA D flip flops and a memory cell with set/reset ability will be introduced. Simulation results demonstrate that the proposed desgins have efficient structures in terms of area, delay and complexity. Also, it is worth mentioning that these designs in contrast to the previous structures do not need any crossover wire. QCA designer, a common QCA layout design and a verification tool is employed to verify and simulate the proposed circuits.

1. Introduction

The technology of semiconductor fabrication has been changed rapidly in the last decades but some applications require less power and more speed yet. These problems force scientists to thrive on finding a remedy and may be an alternative technology. Quantum-dot Cellular Automata (QCA) is one of the candidate technologies. It is a novel nanotechnology which promises extra low power, extremely dense and very high speed structure for designing any arbitrary function at nano-scale [1].

The two types of QCA cells (90° and 45°) are shown in Fig. 1. As shown in this figure, a QCA cell contains four quantum dots positioned at the corners of the square. It has two electrons that can move within the cell. The electrons occupy two corners of the QCA cell diagonally. Regarding the two stable arrangements of the electrons, a binary representation can be achieved. This is shown by polarization (p) of -1 and $+1$ to distinguish between the two stable states [1]. A QCA wire can be easily constructed using a chain of QCA cells.

Three-input majority gates and inverters are the basic building blocks of QCA circuits. The structure of these elements is shown in Fig. 2. As shown in Fig. 2(a), a three-input majority gate takes effect from three sides and emits the majority decision from the fourth side. The structure of an inversion which can be constructed using 11 QCA cells is shown in Fig. 2(b).

In QCA circuits, a group of QCA cells which have a same QCA pipeline clock are shown by a QCA clocking zone [2]. The wave forms of the four clocking zones which are used to design QCA circuits are presented in Fig. 3 [2]. As shown in this figure, each of the clocking zones has four phases (switch, hold, release and relax phase) and there is a 90° phase delay between the clocking zones. If a QCA clocking zone is composed of only one QCA cell, it would be vulnerable to noise; therefore each of the clocking zones should be composed of at least two QCA cells [2].

Some of the previous studies have focused on designing robust QCA circuits. In [3,4] sneak noise paths in QCA circuits have been investigated. Based on [3,4], a robust QCA coplanar crossover scheme should be constructed using two different QCA clocking zones with 90° phase delay. A robust three-input majority gate is constructed using three different clocking zones [3,4]. In a robust three-input majority gate, the wires of the input signals are positioned in the first clocking zone, the middle QCA cells which produce the output are positioned in the second clocking zone with the output wire positioned in the third clocking zone. It is worth mentioning that there is a 90° phase delay between the clocking zones [3,4].

To date, different studies have been performed on QCA and its circuits design and structures [1–22]. Memory cells are one of the attractive areas in designing QCA circuits. In [12–20] various QCA flip flops and memory cells have been introduced. The main aim of this paper is to present efficient designs for level and edge triggered QCA D flip flops. Also, a QCA memory cell with set/reset

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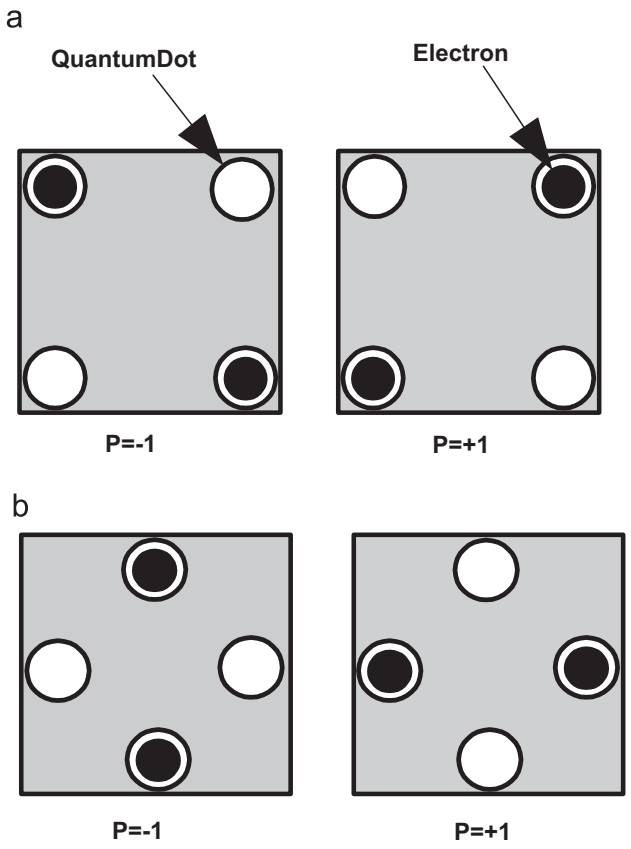

Fig. 1. Basic QCA cells and binary encoding (a) 90° QCA cells and (b) 45° QCA cells.

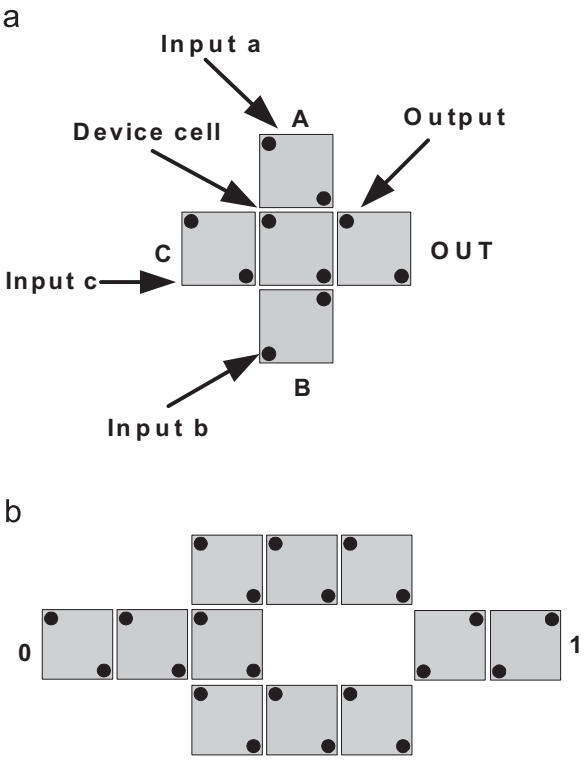

Fig. 2. (a) Three-input majority gate and (b) QCA inverter.

ability will be introduced. The proposed designs have a simple and robust structure and do not need any crossover wire. In these designs, the QCA clocking rules for constructing a robust QCA

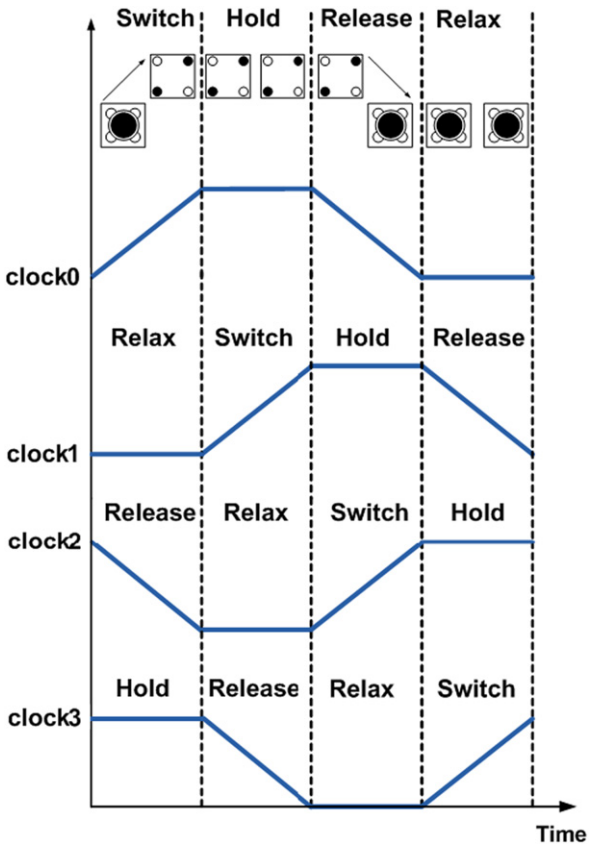

Fig. 3. QCA clocks wave forms.

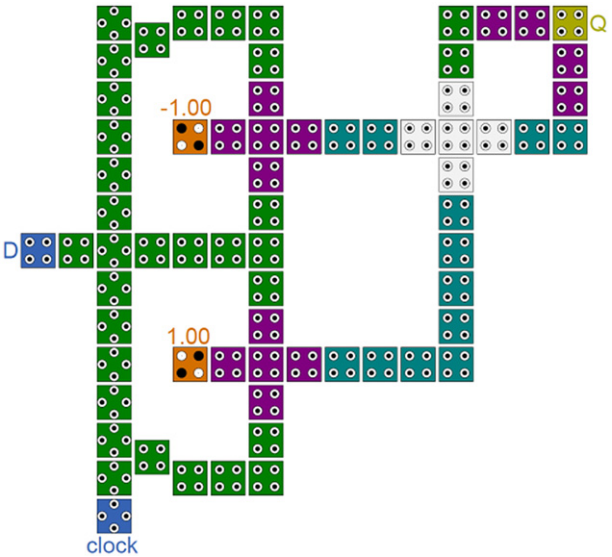

Fig. 4. QCA layout of the presented D flip flop in [13].

circuit have been considered [3,4]. The remainder of this paper is organized as follows: the previous QCA D flip flops and loop based memory cells are presented in Section 2. The new structures are proposed in Section 3. Section 4 compares the new designs with the previous best designs and finally Section 5 provides conclusions.

2. Previous QCA D flip flop and memory cell structures

To date various QCA memory studies have been performed [12–20]. The proposed designs can be categorized in two main groups: loop based [12–17,20] and line based [18,19] structures. In [13] efficient designs for QCA flip flops (D, JK, SR and T flip flops) have been introduced. The presented D flip flop in [13] uses coplanar wire crossing scheme and has a loop based structure (i.e. the previous value of the D flip flop is easily saved using a QCA wire loop). The layout of this structure is shown in Fig. 4. In this layout when the *clock*='0', the value of the D flip flop is not changed whereas when the *clock*='1' the new input value (*D*) is transmitted to the output.

In [14], a dual-edge triggered QCA D flip flop has been introduced (Fig. 5). In this design, *cp* represents the clock pulse input and *D* is the data input of the circuit. Similar to the previous structure [13], this design uses coplanar crossover scheme. In this structure, the previous state of the clock signal and the inversion of the current state of the *cp* are used to determine the output value of the QCA D flip flop.

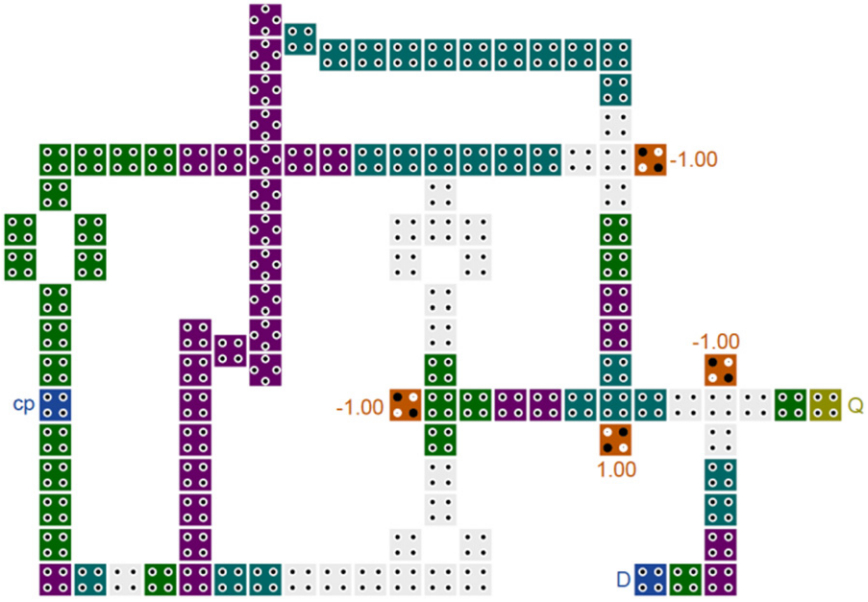

Fig. 5. QCA layout of the presented D flip flop in [14].

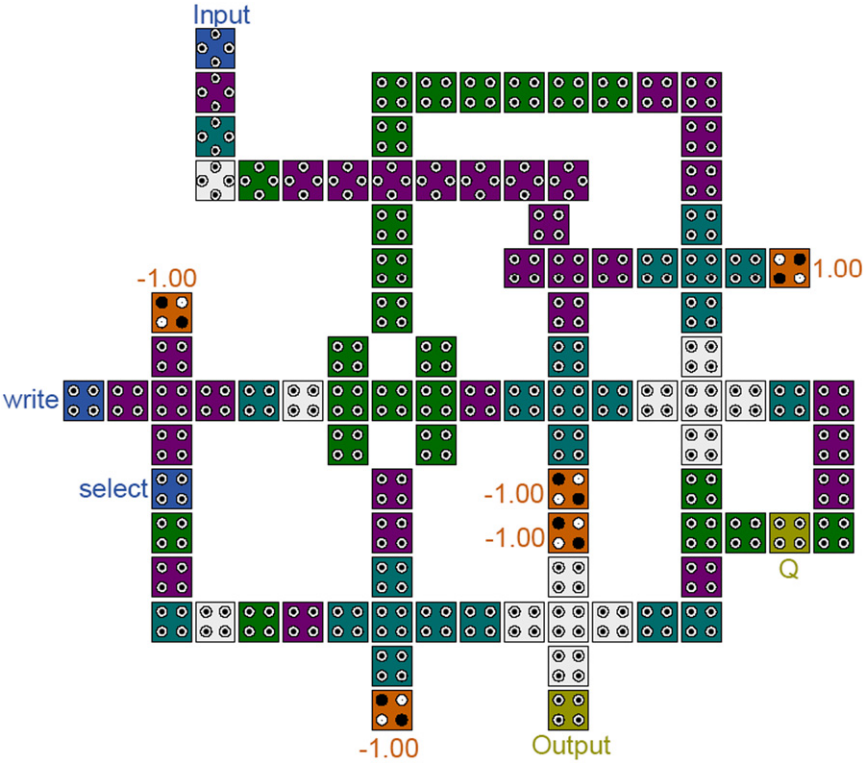

Fig. 6. The first memory layout presented in [15].

Efficient loop based memory cells have been introduced in [15,16]. In these designs, similar to the previous structures, set/reset ability has not been considered. The presented designs in [15] are shown in Figs. 6 and 7. In these layouts, *select* signal is used to activate the QCA memory cell. When the *write*='0', the value is not changed whereas when the *write*='1' the new input value (*input*) is transmitted to the output. As shown in Figs. 6 and 7, these designs do not have a robust structure [3,4]. Also, some of the clocking zones are composed of only one QCA cell and they are vulnerable to the noise.

In addition to the presented designs (Figs. 6 and 7), two other QCA memory cells have been introduced in [15]. These designs have a regular structure and in comparison to the presented designs in Figs. 6 and 7 consume more area and complexity. One of these regular structures is shown in Fig. 8. As shown in this figure, the clocking zones are aligning vertically and horizontally consequently. However, these alignments are not suitable for robust structures. The structure of a robust three-input majority gate [3,4] is shown in Fig. 9. In this figure, required directions of the clocking zones are shown by arrows. Regarding the presented clocking zones, it is clear that in a robust structure, up to down and down to up clocking zone alignments are required simultaneously which is different with the presented design in Fig. 8.

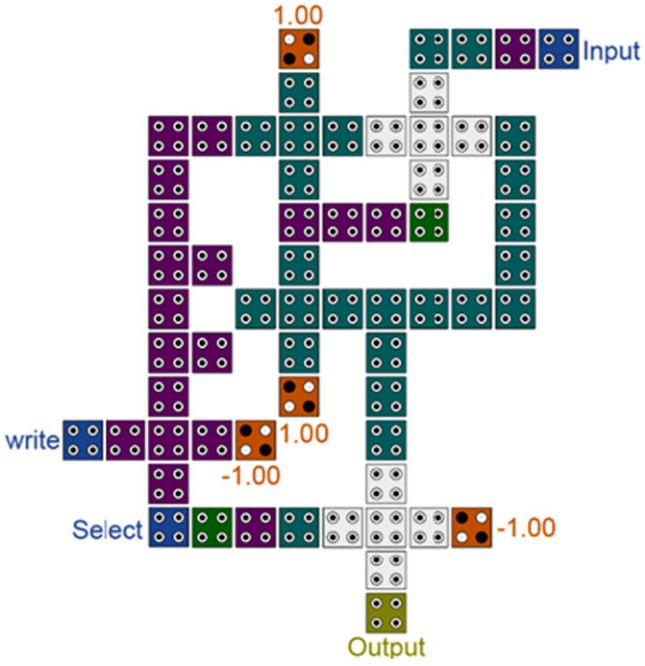

Fig. 7. The second memory layout presented in [15].

3. New QCA D flip flop and memory cell structures

In this section, new robust level and edge triggered QCA D flip flops and a memory cell with set/reset ability are introduced. The basic component of these designs is a robust 2:1 multiplexer. The description of the proposed designs is as follows.

3.1. New robust QCA D flip flops

The schematic of an efficient 2:1 multiplexer with its QCA layout is shown in Fig. 10(a) and (b) (the operation of this design is demonstrated in Table 1). As shown in Fig. 10(b), in this structure the presented design rules for constructing robust three-input majority gates have been considered [3,4]. In this design, each of the three input majority gates is constructed using three different clocking zones. The wires of the input signals are positioned in the first clocking zone, the middle QCA cells which produce the output are positioned in the second clocking zone with the output wire positioned in the third clocking zone. It is worth mentioning that there is a 90° phase delay between the clocking zones [3,4]. Using the proposed 2:1 multiplexer, loop based QCA D flip flops can be easily constructed (as shown in Figs. 11, 13–15). A new level triggered QCA D flip flop with its schematic is shown in Fig. 11(a) and (b). In this structure, if the clock signal is set to '0' then the output will not change. However, when the *clock* is set to '1' the *input* signal will be transmitted to

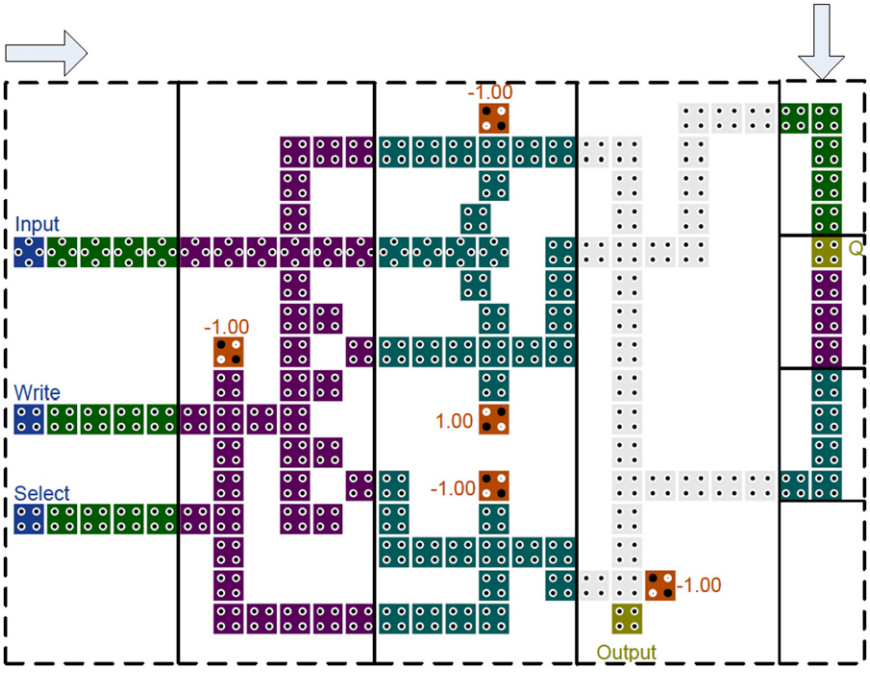

Fig. 8. QCA layout of the first presented RAM cell in [15] constructed using regular clocking zones (direction of the clocking zones are shown by arrows).

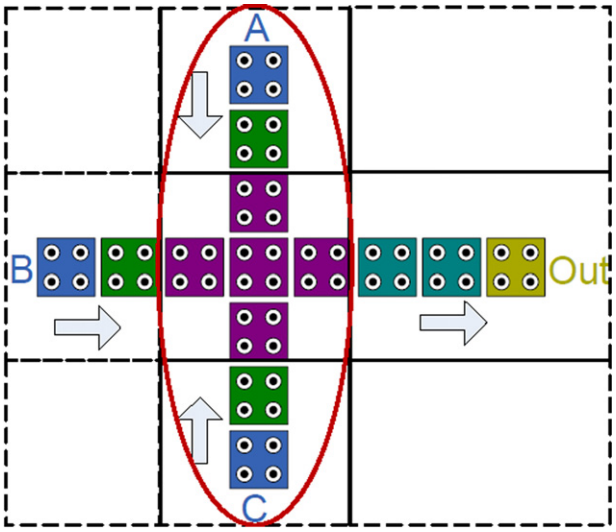

Fig. 9. Robust three-input majority gate with its clocking zones directions.

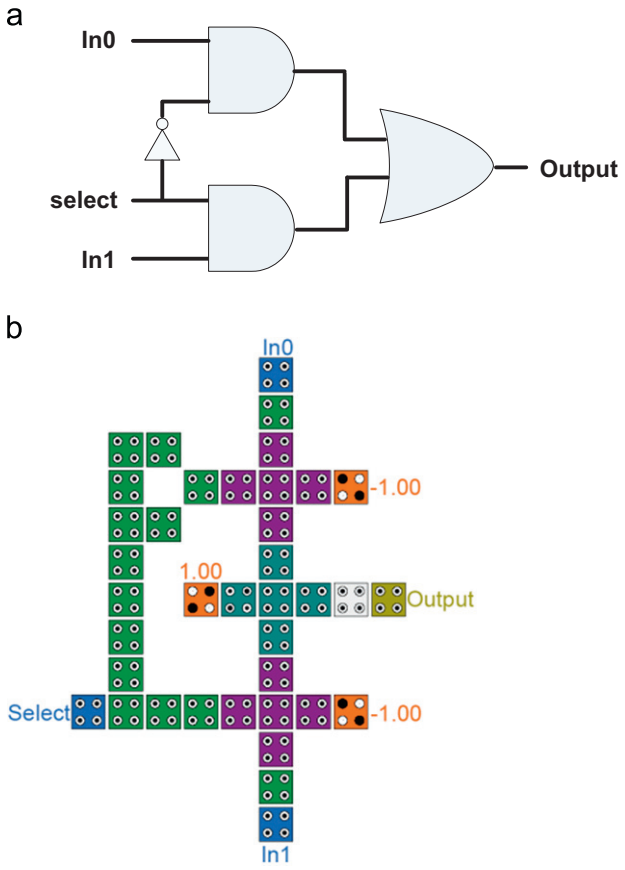

Fig. 10. (a) Schematic of a 2:1 multiplexer and (b) layout of a simple QCA 2:1 multiplexer.

the output. Regarding the proposed operation, this component is sensitive to the level of the clock signal (as shown in Table 2).

An edge triggered QCA JK flip flop has been introduced in [20]. This component uses specific QCA structures to determine the falling edge of the clock signal. These structures [20] are shown in Fig. 12(a) and (b). As shown in this figure, the presented structures have a simple operation. For example, in Fig. 12(a) an AND operation is used between the previous value of the clock signal and the inversion value of the current signal. Therefore, at the falling edge of the clock signal, these values are equal to '1'. In this case, the output of the majority gate (*output*) is set to '1' which determines the falling edge of the clock signal. Based on this structure, an edge triggered QCA D flip flop can be easily constructed. The layout of a new falling edge triggered QCA D flip flop is shown in Fig. 13. In this structure, the part which is shown by dashed square is used to detect the falling edge of the clock signal. In this part, $clock(t-1)$ is the previous value of the clock signal (the value of the clock signal in time $(t-1)$), $\overline{clock}(t)$is the inversion of the current value of the clock signal and *out*1 is the output of the three-input majority gate. As shown in this figure, in comparison to the presented design in Fig. 12(a), the number of clocking zones has been reduced and *out*1 will be valid after 1.75 clock cycles. Also, as shown in this figure, each of the clocking zones is constructed at least using two QCA cells. Based on this

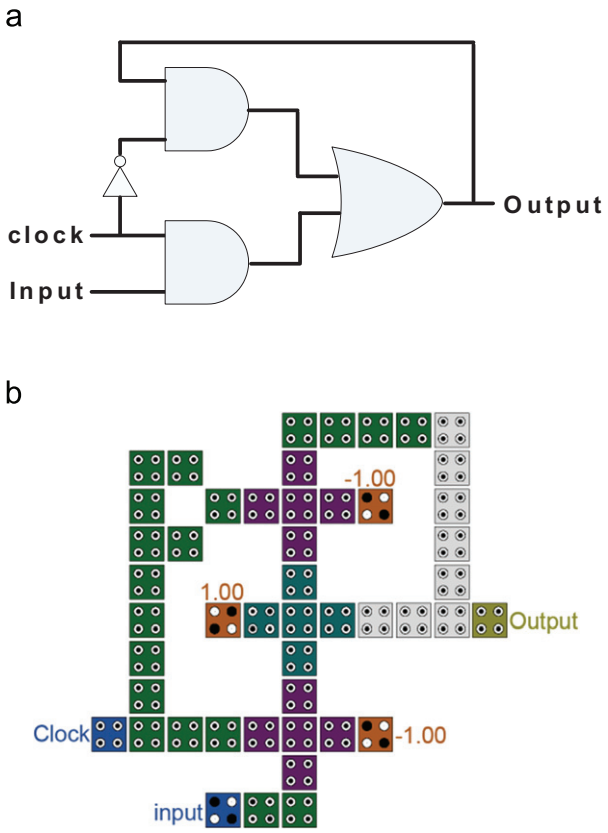

Fig. 11. (a) The schematic of a D flip flop and (b) layout of a level triggered QCA D flip flop constructed using the 2:1 multiplexer in Fig. 10(b).

Table 1
The operation of the proposed 2:1 multiplexer (Fig. 10(b)).

Select	*Output*
0	*In*0
1	*In*1

Table 2
The operation of the proposed level triggered QCA D flip flop (Fig. 11).

Clock	*Output*(t)
0	*Output*$(t-1)$
1	*Input*

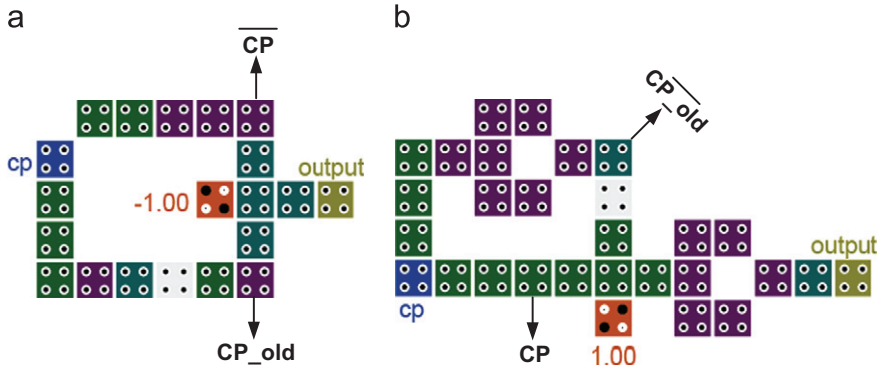

Fig. 12. Two QCA layouts to determine the falling edge of the clock signal presented in [20].

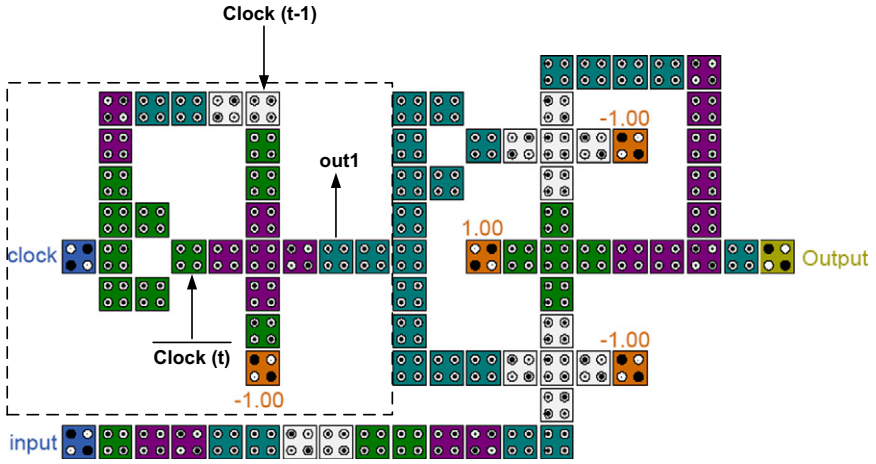

Fig. 13. The QCA layout of a new falling edge triggered QCA D flip flop constructed using the proposed 2:1 multiplexer in Fig. 10(b).

Table 3
The operation of the proposed falling edge triggered QCA D flip flop in Fig. 13.

$Clock(t-1)$	$Clock(t)$	$\overline{Clock(t)}$	$Out1 = maj\left(\overline{clock(t)}, clock(t-1), -1\right)$	*Output*
0	0	1	0	Not changed
0	1	0	0	Not changed
1	0	1	1	*Input*
1	1	0	0	Not changed

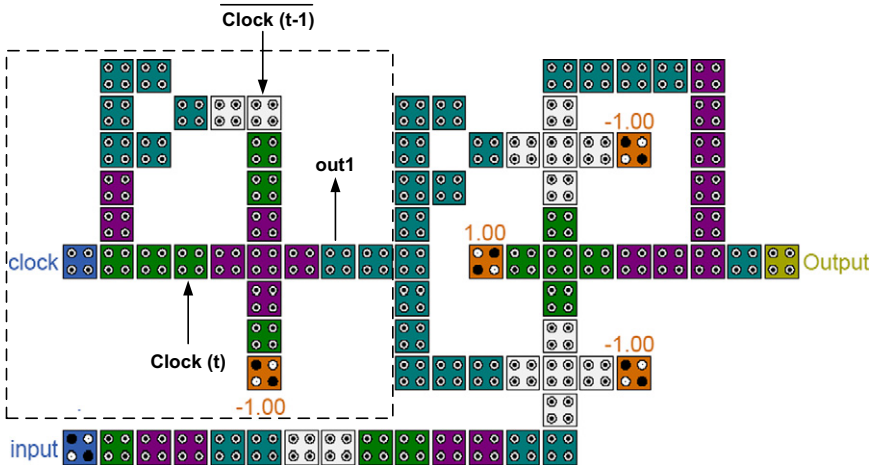

Fig. 14. The QCA layout of a new rising edge triggered QCA D flip flop constructed using the 2:1 multiplexer in Fig. 10(b).

Table 4
The operation of the proposed rising edge triggered QCA D flip flop in Fig. 14.

$Clock(t-1)$	$Clock(t)$	$\overline{Clock(t-1)}$	$Out1 = maj\left(\overline{clock(t-1)}, clock(t), -1\right)$	*Output*
0	0	1	0	Not changed
0	1	1	1	*Input*
1	0	0	0	Not changed
1	1	0	0	Not changed

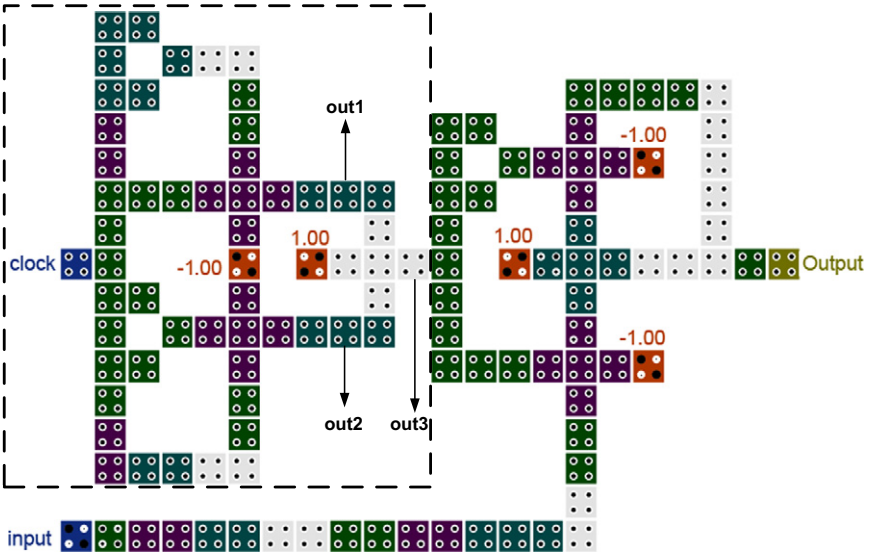

Fig. 15. QCA layout of a new dual edge triggered QCA D flip flop.

Table 5
The operation of the proposed dual edge triggered QCA D flip flop in Fig. 15.

$Clock(t-1)$	$Clock(t)$	$Out1$	$Out2$	$Out3 = maj(out1, out2, 1)$	*Output*
0	0	0	0	0	Not changed
0	1	1	0	1	*Input*
1	0	0	1	1	*Input*
1	1	0	0	0	Not changed

structure, at the falling edge of the clock signal, $\overline{clock(t)}$and *clock* $(t-1)$ are equal to '1' and the new *input* is transmitted to the *output* (in this case, the *out1* is equal to '1'). The complete operation of this component is shown in Table 3. Based on this table, it is clear that only at the falling edge of the clock signal, the *out*1 is set to '1' and the new input is transmitted to the output. Regarding the proposed structure, a rising edge triggered QCA D flip flop can be easily constructed. The layout of this component is shown in Fig. 14 and Table 4 demonstrates the operation of this design. As shown in this figure, the inversion of the previous value of the clock signal (inversion of the clock signal in time $(t-1)$), the current value of the clock signal (the value of the clock signal in time (t)) and the fixed value '-1' are the three inputs of the first majority gate (which is used to generate *out*1). Based on this structure, at the rising edge of the clock signal, $\overline{clock(t-1)}$and *clock(t)* are equal to '1' and the new *input* is transmitted to the *output* (in this case, the *out*1 is equal to '1'). It is worth mentioning that regarding the proposed layouts in Figs. 13 and 14, a dual edge triggered QCA D flip flop can easily be constructed.

The QCA layout of a new dual edge triggered QCA D flip flop is shown in Fig. 15 and Table 5 demonstrates the operation of this

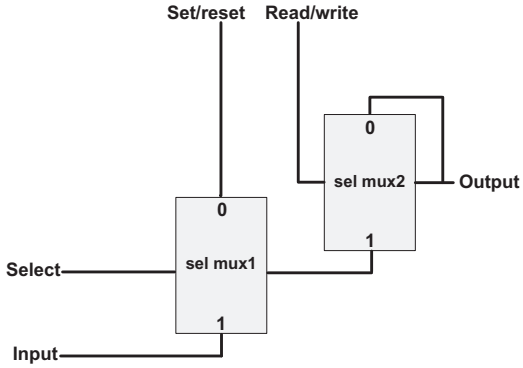

Fig. 16. Schematic of the new QCA memory cell with set/reset ability.

design. As shown in Fig. 15, this structure is made using the proposed falling and rising edge triggered components (which are shown by dashed squares in Figs. 13 and 14) and has a simple operation. In this structure, the outputs of the rising and falling edge components are shown by *out*1 and *out*2 respectively and *out*3 is obtained using an OR gate between these results. Therefore at the falling and rising edge of the clock signal, *out*3 is set to '1' and the new input is transmitted to the *Output* (as shown in Table 5).

3.2. New robust QCA memory cell with set/reset ability

The schematic of a QCA memory cell with set/reset ability is shown in Fig. 16. This structure is constructed using the proposed 2:1 multiplexer in Fig. 10. Based on Fig. 16, the *set/reset* and the

input signal are the two inputs of mux1 and the *select* signal is used as the select line of this element. Also, the output of the mux1 and the *output* signal of the circuit are the two inputs of mux2 and the *read/write* signal is used to select the required value in mux2. The layout of this structure is shown in Fig. 17 and Table 6 demonstrates the operation of this design. In this table, immaterial values are shown by × and *Out* $(t-1)$ indicating the previous value of the circuit. As shown in this table, when the *read/write*='0', the value of the D flip flop is not changed whereas when the *read/write*='1' the new input value (*input*) or *set/reset* signal can be transmitted to the output. In this case, when the *select*='0', the *set/reset* signal is transmitted to the output. It is clear that by using *select*='1' the new input is transmitted to the output. It is worth mentioning that in QCA circuits, synchronization of the input signals is of great importance. As shown in Fig. 17, in the proposed design, this criterion has been considered and in order to synchronize the input signals, additional clocking zones have been added to the *read/write* wire. Therefore, the

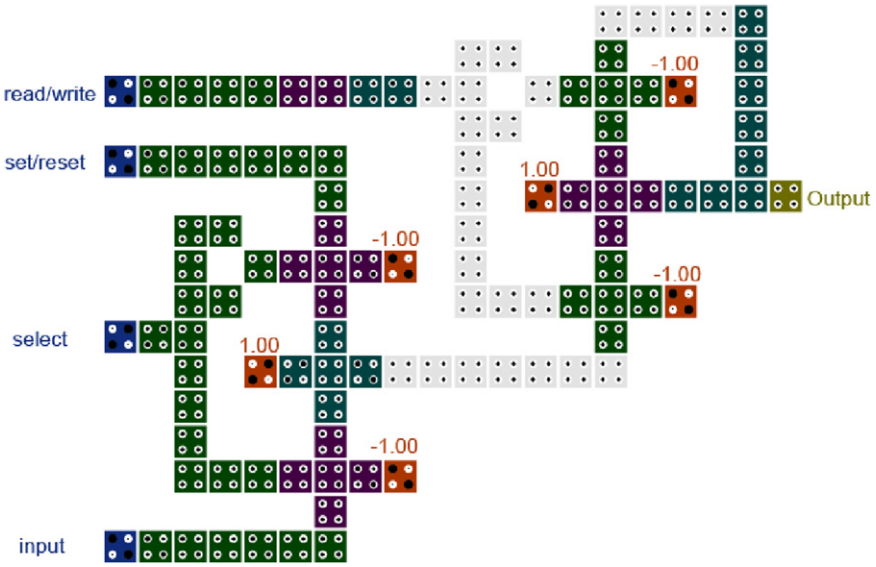

Fig. 17. Layout of the new QCA memory cell with set/reset ability.

Table 6
The operation of the proposed QCA memory cell with set/reset ability (Fig. 17).

Read/write	Select	Set/reset	*Out*(t)
0	×	×	*Out*($t-1$)
1	0	0	0
1	0	1	1
1	1	×	*Input*

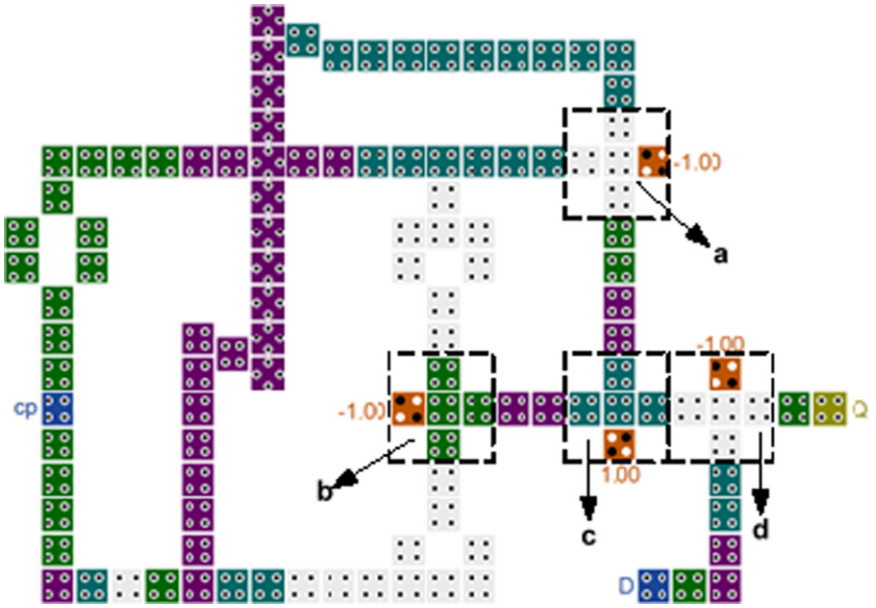

Fig. 18. QCA layout of the presented D flip flop in [14].

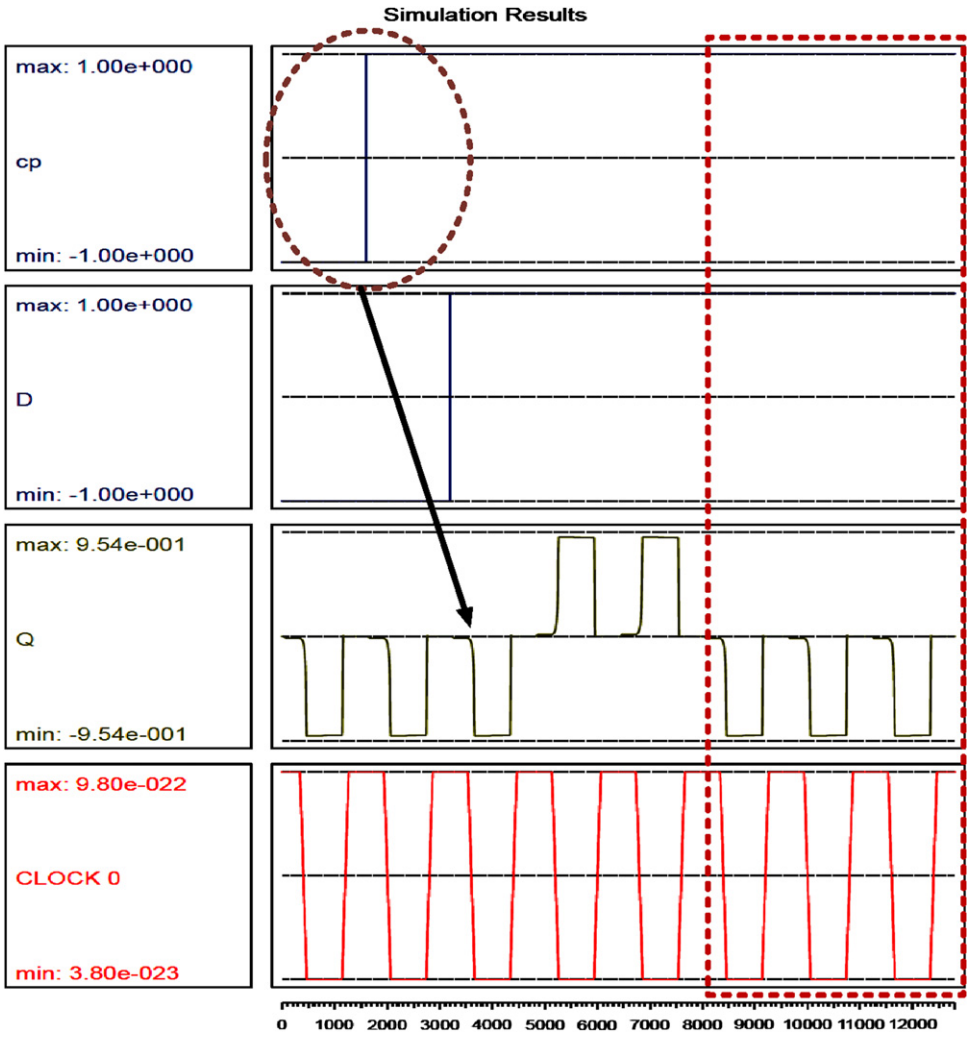

Fig. 19. Simulation result of the presented design in [14].

output of mux1 and *read/write* signal arrive to the mux2 with a same latency.

4. Results and discussion

As mentioned earlier, in [14] a dual-edge triggered QCA D flip flop was introduced. The QCA layout of this design is shown in Fig. 18. In this figure, *cp* represents the clock pulse and *D* is the data input of the circuit. This design uses four three-input majority gates to generate the output (*Q*), which are shown by dashed squares *a*–*d* (Fig. 18). Using the three-input majority gates *a*–*c*, EX-NOR operation between the inversion of *cp* and *cp_old* (the previous value of the clock signal *cp*) is implemented [14]. The outputs of these majority gates are as follows:

Output a: $cp\_old.\overline{cp}$, *Output b*: $(\overline{cp\_old}.\overline{\overline{cp}})$, *Output c*: $(cp\_old.\overline{cp}+\overline{cp\_old}.\overline{\overline{cp}}=(cp\_old)EX{-}NOR(\overline{cp}))$

The final result (*Q*) is obtained in the last three-input majority gate (which is shown by *d*) through an AND operation between the result of the EX-NOR operation and the input *D*

$$Q=\left(cp\_old.\overline{cp}+\overline{cp\_old}.\overline{\overline{cp}}\right)AND(D)$$

Regarding the proposed operation, this component [14] has a dual edge structure and the input value is transmitted to the output in each of the rising and falling edges of the clock signal (in the rising and falling edges of the *cp*, the EX-NOR result is equal to '1' and the input value *D* is transmitted to the output). However, this design has remarkable disadvantages. The most important drawback is the fact that this component does not act as a D flip flop. It is clear that in a D flip flop, the output will not change unless the required clock condition is satisfied (regarding the type of the D flip flop). For example in the presented QCA D flip flop in [13] (presented in Fig. 4), the previous value of the circuit easily has been saved using a QCA wire loop. In this structure (Fig. 4), regarding the value of the clock signal the previous value is kept or the new input is transmitted to the output. However, in the presented design in [14], as shown in Fig. 18, the previous value of the output (*Q*) is not saved. In other words, in this structure in each of the rising and falling edges of the *cp* the input *D* is transmitted to the output. However, in this structure when the clock signal is kept high or low, the value of the circuit is not saved. The simulation result of this structure is shown in Fig. 19. This simulation has been done using the default parameters of both coherence and bi-stable simulation engines [21] achieving the same results. Based on the presented simulation result, after the forth falling edge of the clock 0, the output *Q* is valid and '1' is transmitted to the output (*Q* is equal to '1'). However, when the clock signal is kept high (which is shown by dashed square in Fig. 19), the output is not saved and is changed to '0'.

It is worth mentioning that in the presented design in [14], the input *D* and the output of the three-input majority gate *c* have

Fig. 20. Simulation results of the proposed QCA D flip flops in Figs. 11, 13, 14 and 15.

different delays. The new values of the three-input majority gate *c* are valid after 2.75 clock cycles while the new input *D* arrives to the three-input majority gate *d* after 0.75 clock cycles. Therefore, in order to achieve the expected results, the input *D* must be stable at least for 2.75 clock cycles. For example, as shown in Fig. 19, at first there is a rising edge in the clock signal *cp* (which is shown by dashed circle in Fig. 19). In this case, the input *D* is equal to zero and it is expected that after the forth falling edge of the clock 0, the output *Q* is set to '0'. But, as shown in Fig. 19, after this delay, the output (*Q*) is equal to '1'. This is due the fact that the input *D* at first is equal to zero. But, it rapidly has been changed to '1'. Therefore after 2.75 clock cycles, the result of the EX-NOR and the input *D* are equal to '1' and this value ('1') is transmitted to the output. It is worth mentioning that the new

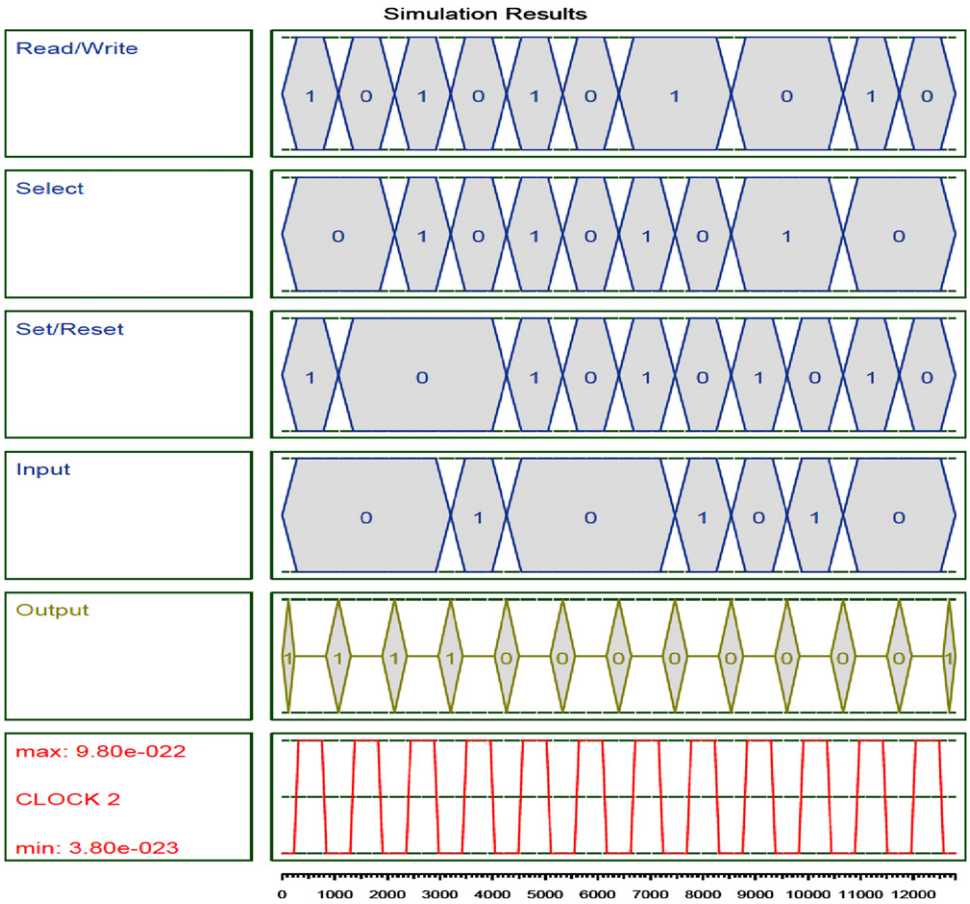

Fig. 21. Simulation results of the proposed QCA memory cell with set/reset ability (Fig. 17).

Table 7
Comparison of the proposed QCA circuits.

QCA D flip flop/memory structures		Crossover type	Set/reset ability	Area (μm^2)	Complexity (cell count)	Delay (clock cycle)
QCA D flip flops	Presented dual edge triggered design in [14]	Coplanar	No	0.16	116	3
	Presented level triggered design in [13]	Coplanar	No	0.08	66	1.5
	The level triggered QCA D flip flop in Fig. 11	–	No	0.05	48	1
	The falling edge triggered QCA D flip flop in Fig. 13	–	No	0.09	84	2.75
	The rising edge triggered QCA D flip flop in Fig. 14	–	No	0.09	84	2.75
	The dual edge triggered QCA D flip flop in Fig. 15	–	No	0.14	120	3.25
QCA memory cells	Memory design 1 in [15] (Fig. 6)	Coplanar	No	0.11	100	2
	Memory design 2 in [15] (Fig. 7)	–	No	0.07	63	2
	Proposed memory cell in Fig. 17	–	Yes	0.13	109	1.75

edge triggered QCA D flip flops in contrast to the presented design in [14] have a correct operation and can be useful components for designing larger QCA circuits.

As mentioned earlier, in this study simulations have been performed using QCA designer [22] version 2.0.3. All of the simulations have been done using the default parameters of both coherence and bi-stable simulation engines [21] achieving the same results. Fig. 20(a)–(d) indicates the simulation results of the proposed QCA D flip flops in Figs. 11, 13, 14 and 15 respectively. Also, the simulation result of the proposed QCA memory cell (Fig. 17) has been shown in Fig. 21. It is worth mentioning that in this design (Fig. 17) the results are valid after the second falling edge of the clock 2.

Based on the simulation results, it is clear that the proposed designs work accurately. For example, in the proposed structure in Fig. 11(b), the results are valid after the first falling edge of the clock 3. It is worth mentioning that in order to clear the simulation results of this circuit for the readers, one clocking zone 0 (a clocking zone which is composed of QCA cells positioned in clock 0) has been added to the wire which transmits the output. Therefore, in Fig. 20(a), the outputs are valid after the second falling edge of the clock 0. Based on this figure, it is clear that the proposed design has a correct operation. For example, at first, the *clock* and *input* signals are equal to '1'. Therefore, (based on Table 2) after the second falling edge of the clock 0 the input must be transmitted to the output. As shown in Fig. 20(a), the expected result has been achieved which shows the correct operation of the proposed design. The operation of other designs can be easily investigated. For example, the simulation results of the proposed falling edge triggered QCA D flip flop (Fig. 13) is shown in Fig. 20(b). Based on this design, the results are valid after the third falling edge of the clock 2. As shown in Fig. 20(b), the first and second values of the clock signal are equal to '1' and '0' respectively. Therefore, based on Table 3, after the third falling

edge of the clock 2, the input (which is equal to '1') must be transmitted to the output. Fig. 20(b) shows that the proposed circuit has a correct operation and expected result is achieved. Based on Fig. 20(b), after the falling edge of the clock signal, this signal is equal to '0' for two clock cycles. After this state, there is a rising edge and then the clock signal is stable (is equal to '1') for one clock cycle. In all of these states (based on Table 3), the output must be stable and equal to the first value of the circuit (*i.e.* it must be equal to '1' for four clock cycles). As shown in Fig. 20(b), these expected results have been achieved which show the correct operation of the proposed design.

Using QCA Designer, area, delay and complexity (cell count) of QCA circuits can be easily obtained. The comparison results of the proposed designs are shown in Table 7. As mentioned earlier, the new dual edge QCA D flip flop in comparison to the previous structure [14] has a more accurate operation. Also, the new circuits have a robust structure and the new memory cell has a set/reset ability which is different with the previous structures. These designs do not need any crossover wire and can be constructed using 90° QCA cells. Table 7 also demonstrates that the new level triggered QCA D flip flop (Fig. 11) surpasses the previous design (presented in [13]) in terms of area, delay and complexity (cell count). Also, based on this table, it is clear that the proposed QCA memory cell (Fig. 17) consumes more QCA cells in order to obtain set/reset ability. Regarding these comparison results, the new structures can be suitable components for designing larger QCA circuits.

5. Conclusions

In this study, simple and robust QCA D flip flops and a memory cell with set/reset ability were introduced. The proposed designs have efficient structures in terms of area, delay and complexity (cell count). Simulations of the proposed designs were carried out using both bi-stable and coherence engines of QCA designer. The results show the accuracy of the proposed designs and these structures can be useful components for designing larger QCA circuits.

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