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RESEARCH ARTICLE

Efficient Quantum Dot Cellular Automata Memory Architectures Based on the New Wiring Approach

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Quantum dot cellular automata (QCA) implies a pioneer technology at Nano scale computer designs. Employing this technology is one of the solutions to decrease the size of circuits and reducing power dissipation. In this paper, an area optimized level sensitive *D* Flip Flop as well as an overall high performance edge triggered *D* Flip Flop and *T* Flip Flop and finally an ultra-high speed, area efficient with minimum number of cells RAM cell are presented. Random access memory (RAM) is a principle component of the QCA digital circuits, which is made based on one of the four kind of flip flops. It is to be notified that a novel approach in QCA wiring is also presented. The QCA structures, which utilize this wiring approach, are more efficient in the number of cells, the area occupation, the propagation delay and also there are no coplanar cross over wiring which makes the designs feasible. The proper logical functionality of the proposed designs is proven using the QCADesigner.

Keywords: Quantum Dot Cellular Automata, *D* Flip Flop, *T* Flip Flop, RAM Cell, Set/Reset Ability.

1. INTRODUCTION

Nowadays with explosive trend of integration in the digital circuits, transistors scaling have diminished aggressively and power dissipation have been reduced. Accordingly, the needs for new devices replacing the conventional CMOS circuits have been increased.[1] Therefore possible nanoscale alternate technologies such as Carbon Nanotube Field Effect Transistor (CNFET), Single Electron Transistor and its related challenges and also Optoelectronic devices and interconnections are investigated.[3–6] Quantum dot cellular Automata (QCA) is one of these alternative technologies at Nano scale with extremely slight feature size and ultra-low power consumption.[2]

The basic building blocks of QCA devices are shown in Figure 1. Each squared cell consist four quantum dots and two excess electrons occupying the opposite sites due to coulomb repulsion. These electrons can tunnel between neighbor dots, but they cannot tunnel out of the cell due to high inter cellular potential (barrier). A QCA cell has two stable states as shown in Figure 1, noted as the cell polarizations ($P = +1$ and $P = -1$) and are encoded to binary values of "1" and "0", respectively.[2,7] There are two main types of cells in QCA, a 90° standard cell and 45° Rotated cell. The wires are constructed from one of these two types, as illustrated in Figure 2. In 90° wire scheme, when an input signal is applied to the input cell, all cells will be forced to have the identical polarization as the first one and signal will be propagated from left to right (Fig. 2(a)). However, in 45° wire scheme, cells polarization will be reversed at each cell (Fig. 2(b)).

The coplanar cross-over wiring is reached by overpassing these two types of wires. An inverter and a majority gate are shown in Figures 3(a), (b). The elementary logic building in QCA is majority gate, which is composed of three input cells, a device cell and an output cell. Assuming the inputs are A, B, C, the logic function of the majority gate is

$$M(A, B, C) = AB + AC + BC \quad (1)$$

By setting one of the input's polarization to "0" or "1", 2-input AND gate or 2-input OR gate is implemented, respectively.[2]

Computation in QCA is accomplished by controlling the tunneling with a four-phase clock (switch, hold, release, relax), so a clocked QCA utilizes four clocks 1, 2, 3, 4, as demonstrated in Figure 4. Each clock has a 90° phase delay from the preceding clock.[7] It is noteworthy that the number of cells in the same clocking zone must be at least

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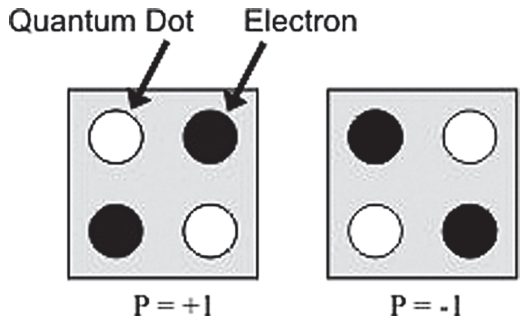

Fig. 1. Basic QCA cells and two possible polarizations.

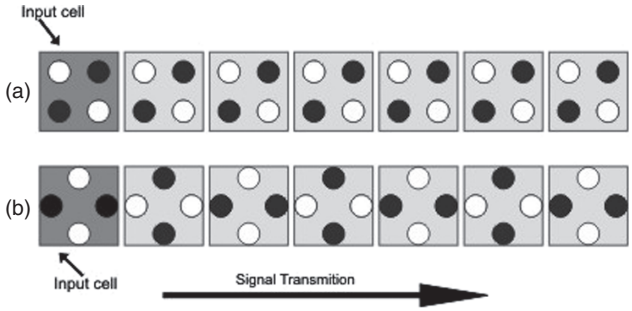

Fig. 2. (a) The standard QCA wire, (b) The inverter chain.

two cells to prevent the noise effects on the circuit. Moreover, the longest QCA wire length within each clocking zone should be controlled to avoid the increased delay, slow timing and other negative effects of this matter on the QCA circuits.[8,9]

Many efforts have been made to design various logic QCA circuits. For instance, an efficient design for one bit full adder,[10,11] the testable *n*-input logic gates in QCA,[29] QCA implementation of a configurable logic block,[12] study on five input majority gate,[13] a fault tolerance analysis in QCA,[17] a new approach in QCA cell arrangements,[27]and some flip flops and memory structures in Refs. [14–16, 18–25] can be mentioned.

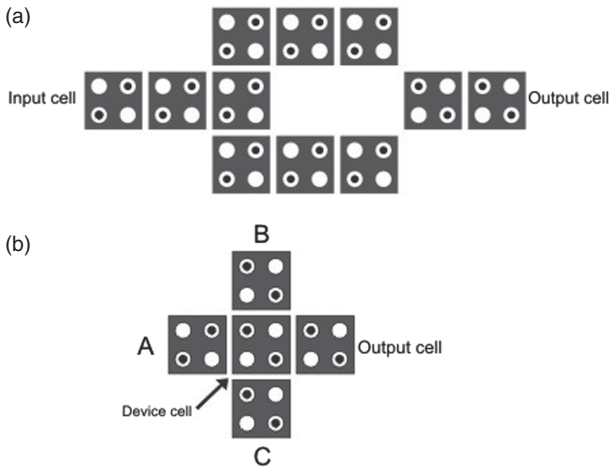

Fig. 3. (a) QCA Inverter, (b) 3-input majority gate.

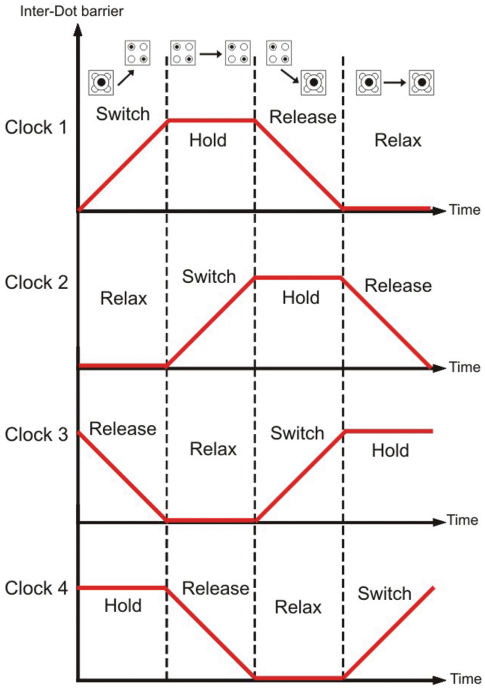

Fig. 4. QCA clocking zones.

In this paper, we propose a new wiring approach to simplify designing of QCA logics. By utilizing this kind of wiring instead of traditional QCA wiring, circuits can be more efficient in terms of cells number, clocking zones number and wasted area. To demonstrate the advantage of this approach a novel robust *D* and *T* flip flop and also new RAM cell with set and reset ability are implemented. Comparison results by state-of-the art show efficiency of this approach. The rest of the paper is organized as follow: Section 2 provides previous works review for *D* flip flop, *T* flip flop and RAM cell designs in QCA. The presented wiring method and the implementation of level sensitive *T* and *D* flip flops and also the edge triggered *D* flip flop will be introduced in Section 3. Sections 4, 5 discusses the novel robust architecture for RAM cell with set/reset

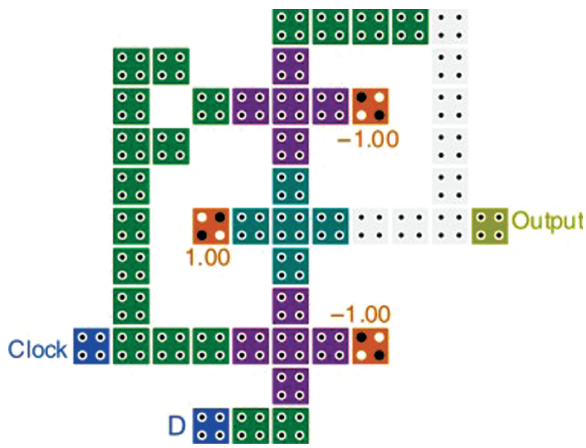

Fig. 5. The level triggered *D* flip flop.[22]

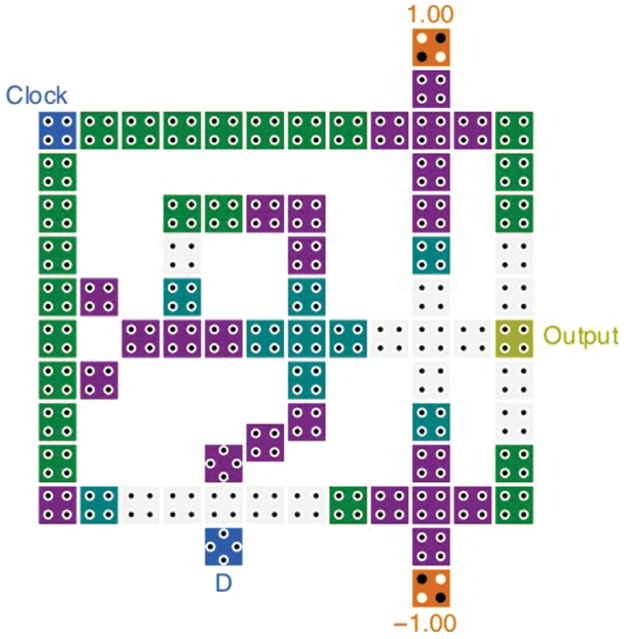

Fig. 6. The rising edge triggered *D* flip flop.[14]

ability and the simulation results for all proposed designs, respectively. Last section belongs to conclusion.

2. STATE-OF-THE-ART

Totally there are two kind of memory cell implementation in QCA, line-based in Refs. [19, 25] and loop-based in Refs. [14–16, 18, 20–24]. In this part previous works are studied, first the *D* flip flop, then the *T* flip flop and last the RAM cell.

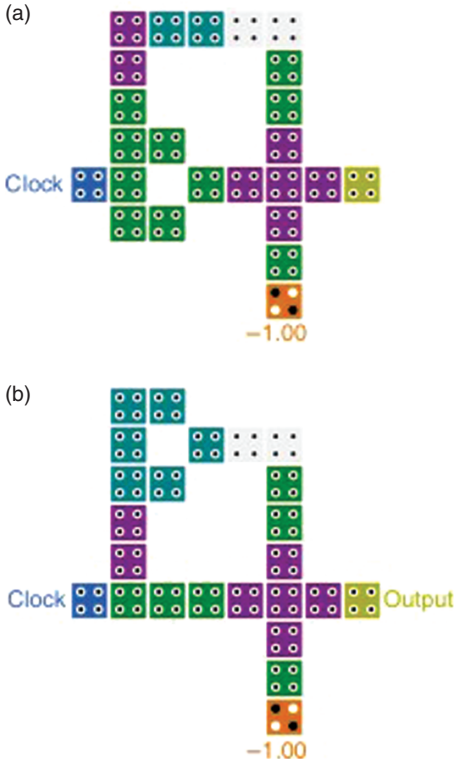

Fig. 7. (a)The falling edge converter,[22] (b) The rising edge converter.[22]

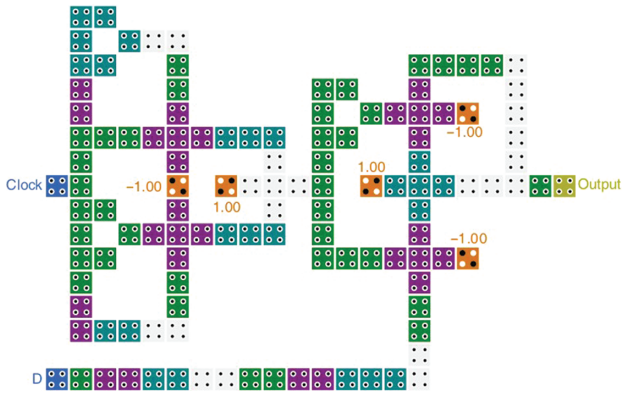

Fig. 8. The dual edge triggered *D* flip flop.[22]

2.1. *D* Flip Flop

The basic loop-based architectures for the four kind of flip flops have been described.[23] The main similarity of them is that all of the presented designs have been constructed using the coplanar cross over wires. Another loop-based QCA *D* flip flop based on the MUX2:1 has been introduced in Ref. [22], as shown in Figure 5. This design has a regular structure with employing the robust three-input majority gates.

An innovative structure for the rising edge *D* flip flop has been introduced.[14] When the clock signal is altered

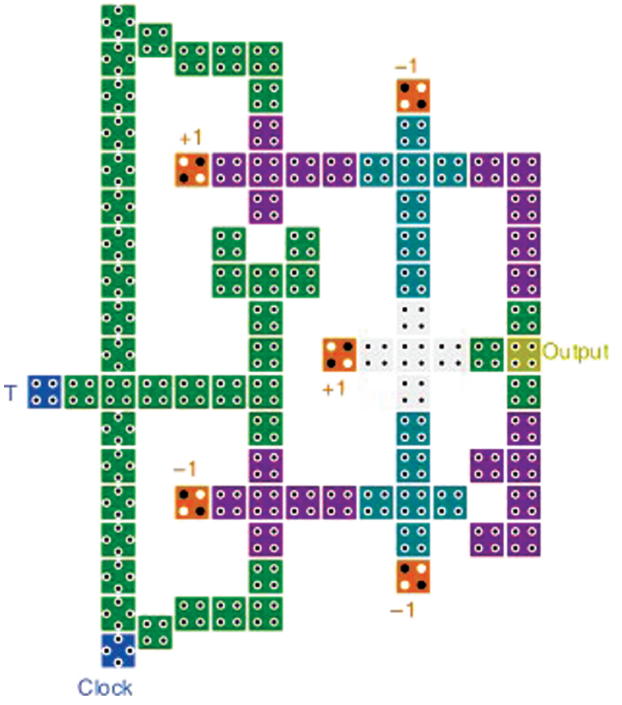

Fig. 9. The level sensitive *T* flip flop.[23]

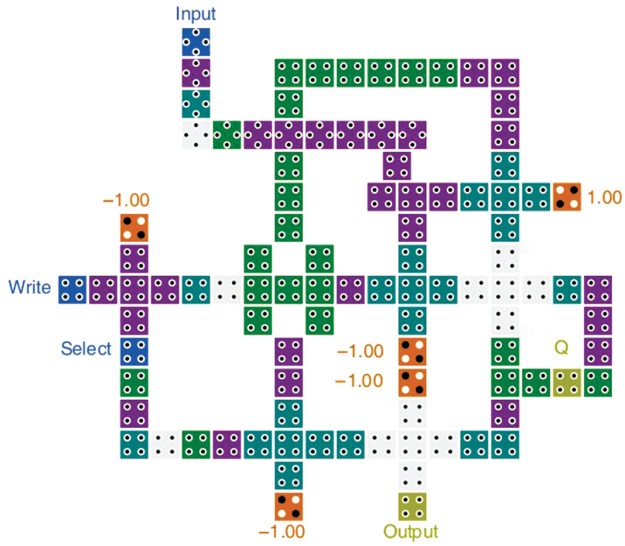

Fig. 10. The SR-Latch based RAM structure.[21]

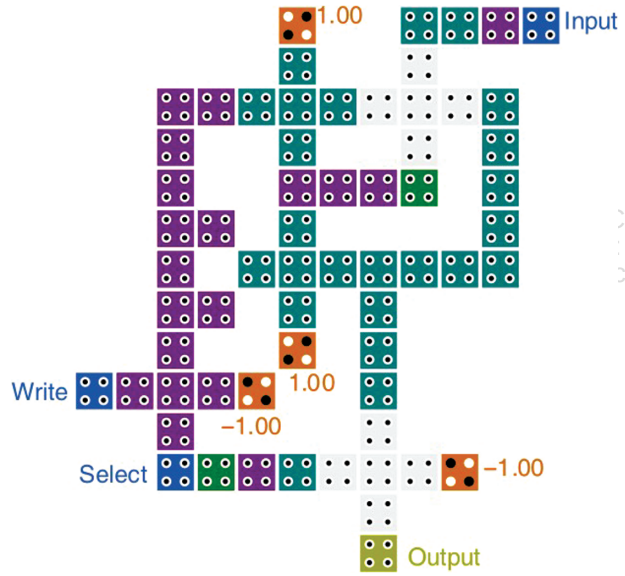

Fig. 11. The *D*-Latch based RAM structure.[21]

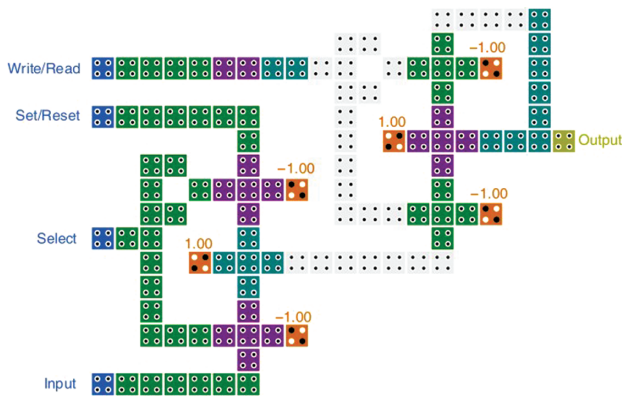

Fig. 12. The *D*-Latch based RAM structure.[22]

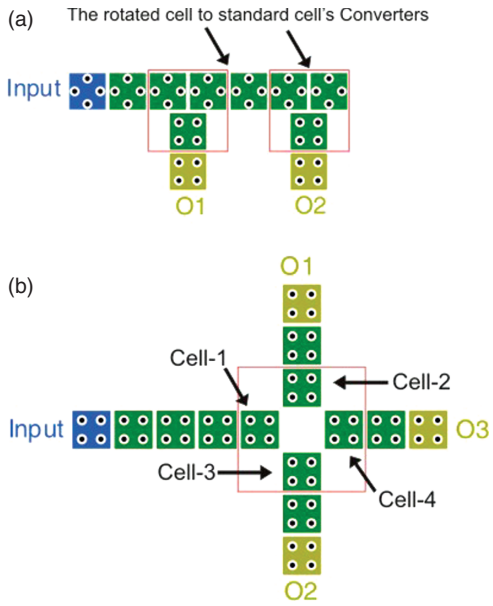

Fig. 13. (a) The conventional wiring scheme by using the converters. (b) The proposed wiring scheme.

from "0" to "1," the input signal is transmitted to the output in one clock cycle. The number of used cells in this design is 75 (Fig. 6). Moreover, a rising edge triggered *D* flip flop and also a falling edge triggered *D* flip flop have been suggested using the converters which shown in Figures 7(a), (b).[22] By connecting these converters to the presented *D* flip flop, edge sensing mechanism is accomplished. Both designs have been made using standard cells

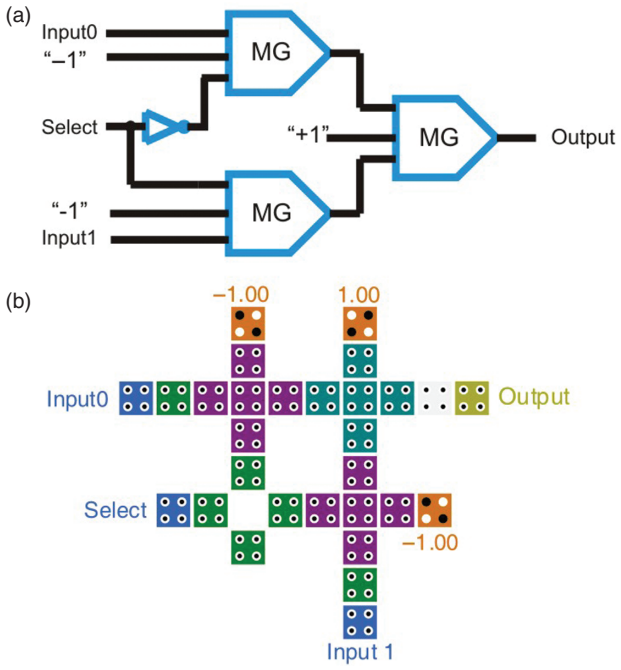

Fig. 14. (a) The schematic of MUX 2:1. (b) The proposed structure for MUX 2:1 based on the new wiring scheme.

Table I. The operation of MUX 2:1.

Select	Output
0	Input 0
1	Input 1

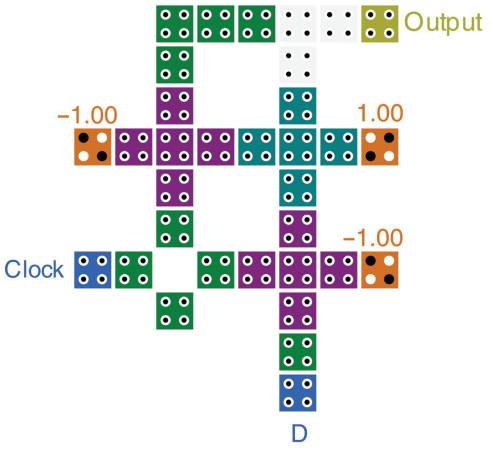

Fig. 15. The proposed level sensitive *D* flip flop.

Table II. The operation of proposed level sensitive *D* flip flop.

Clock	Output
0	Last output
1	*D*

with robust structure, also these designs have consumed 84 cells covering 0.09 μm^2 area with 2.75 latency for transmission of the input signal to the output.

A robust layout of a dual edge triggered QCA *D* flip flop is also presented in Ref. [22] which is constructed using the combination of two kinds of edge convertors and *D* flip flop components, as illustrated in Figure 8. In both edge of the clock (rising, falling), input signal is propagated to the output after 3.25 clock cycle.

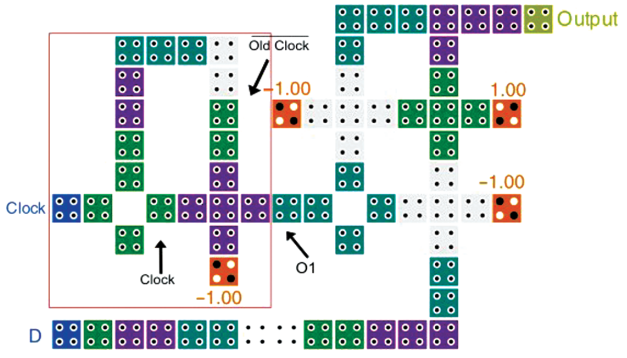

Fig. 16. The proposed rising edge triggered *D* flip flop based on the new wiring scheme.

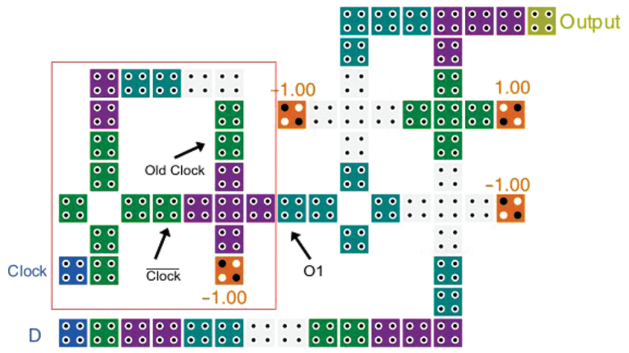

Fig. 17. The proposed falling edge triggered *D* flip flop based on the new wiring scheme.

Table III. The Operation of proposed rising edge triggered *D* flip flop.

Old clock	Clock	O1	*Output*
0	0	0	Last output
0	1	1	*D*
1	0	0	Last output
1	1	0	Last output

Table IV. The Operation of proposed falling edge triggered *D* flip flop.

Old clock	Clock	O1	Output
0	0	0	Last output
0	1	0	Last output
1	0	1	*D*
1	1	0	Last Output

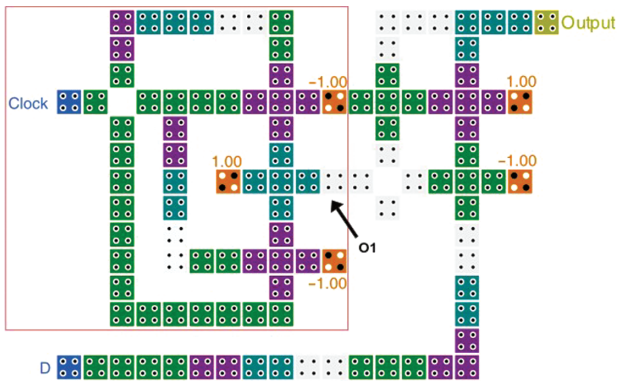

Fig. 18. The proposed dual edge triggered *D* flip flop based on the new wiring scheme.

Table V. The Operation of proposed dual edge triggered *D* flip flop.

Old clock	Clock	O1	*Output*
0	0	0	Last output
0	1	1	*D*
1	0	1	*D*
1	1	0	Last output

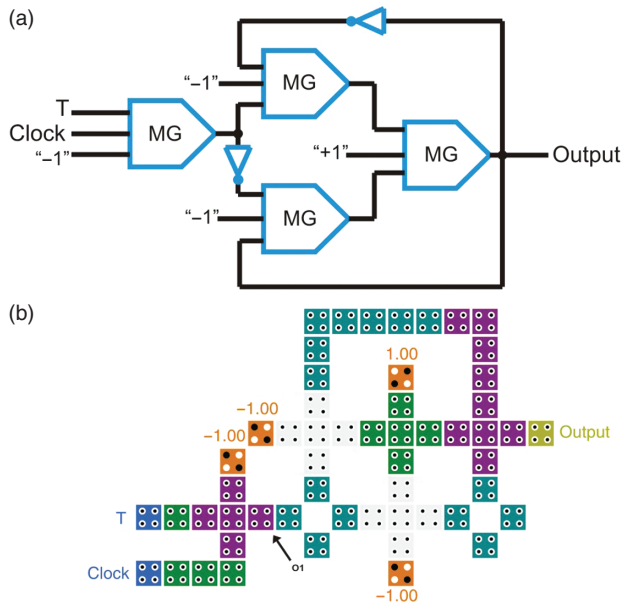

Fig. 19. (a) The schematic of proposed level sensitive *T* flip flop. (b) The proposed structure for *T* flip flop based on the new wiring scheme.

2.2. *T* Flip Flop

As mentioned above, a *T* flip flop structure has been represented,[23] which constructed using five 3-input majority gates with totally 92 cells and also misaligned cells, coplanar cross over method with eighteen cells longest wire length. This design does not use robust three input majority gate as it shown in Figure 9.

2.3. RAM Cell Review

There are many studies according to the improvement of the RAM cell. In Ref. [21] two QCA structures for loop-based random access memory (RAM) have been presented. The first design is based on SR-latch, as demonstrated in Figure 10. In this structure coplanar cross over wiring and consequently miss aligned cell have been employed. The second design (Fig. 11) has been based on *D*-latch. Both designs have not used robust 3-input majority gate structure in some places, also these structures have one cell in some of the clocking zones which leads to erroneous QCA circuit. In addition, set/reset ability of RAM is not considered in these architectures. A RAM cell architecture with set and reset ability has been introduced which is constructed using two MUX 2:1 (Fig. 12).[22] It enjoys robust architecture and fast computation. The propagation latency of this circuit is 1.75 clock cycle, but inappropriate

Table VI. The operation of proposed level sensitive *T* flip flop.

Clock	*T*	Q_{t+1}
1	0	Q_t
1	1	$\bar{Q}_t$
0	*x*	Q_t

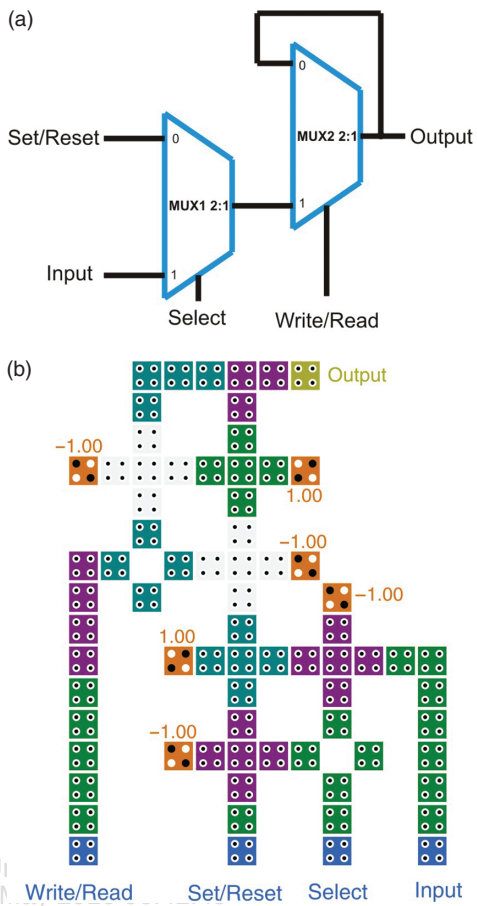

Fig. 20. (a) The presented schematic for RAM cell with set/Reset ability.[22] (b) The proposed RAM cell with set/Reset ability based on the new wiring scheme.

design of MUX 2:1 leads to high number of cells, more occupation area and input to output delay.

3. PROPOSED STRUCTURES FOR ROBUST *D* AND *T* FLIP FLOPS

In this section, a novel wiring scheme for the QCA circuits and a simple design for MUX 2:1 based on this approach have been presented, subsequently an efficient design for *D* and *T* flip flop have been proposed.

3.1. The Proposed Wiring Approach

In the most of QCA logic circuits, the inverter chains have been used contributing to their sufficiency to produce the

Table VII. The operation of proposed RAM cell with set/Reset ability in Figure 20(b).

Select	Write/read	Input	Set/reset	Output
0	1	*X*	0	0
0	1	*X*	1	1
1	1	0	*X*	0
1	1	1	*X*	1
X	0	*X*	*X*	Last output

similar input signal in odd cell numbers and the inverted input signal in even cell numbers and also supporting of coplanar cross over wiring. Using inverter chain ordinarily leads to more complicated circuits. As it is demonstrated in Figure 13(a), a converter is required to convert the 45° rotated cell to 90° standard cell.[2] Furthermore the circuit has consisted of some misaligned cell to connect the converted cell to rest of the standard cells. It was also exposed that standard QCA wires are more defect-tolerant than inverter chains. As mentioned before, in the QCA design a significant effort should be made to hold the length of the wire within same clocking zone to a minimum, so in these circuits length of the longest wire will be increased.

Our proposed approach is illustrated inside the red square in Figure 13(b), Constructing from four QCA cells which arranged diagonally. When the input signal is arrived at cell-1, the inverted signal transmitted to cell-2 and cell-3 at the same time and cell-4 accepted the polarization of cell-1 simultaneously. As it is clear, the corresponding polarization of the cell-1 and cell-4 and the inverted polarization of cell-2 and cell-3 can be applied to more simple and robust designs with no misaligned cell instead of conventional 45° wiring scheme.

To date, there are various designs for the MUX 2:1 have been introduced.[22, 26] As it shown in Figure 14, the schematic of MUX 2:1 and the proposed layout are indicated. The presented design has been composed of three majority gates with robust structure in least possible area. Each one of the majority gates have received the inputs in the same clocking zone, the middle cells are also in similar second clocking zone and the output has considered in third clocking zone. This architecture uses only 29 cells and 0.04 μm^2 wasted area. Moreover this design has a simple structure with a diagonal clocking zone that can be applied to more parallelism in larger buildings.[8] Operation of the proposed MUX 2:1 is shown in Table I, By setting select signal to "0" and "1," Input 0 and Input 1 have been transmitted to output, respectively.

3.2. The Proposed *D* and *T* Flip Flop

A novel optimized level sensitive *D* flip flop is constructed based on the proposed MUX 2:1 (Fig. 14(b)) by joining the output signal to the first input (Fig. 15). In negative level of the clock, *D* flip flop value is not changed and data saved through a four-clocked loop. In positive level, input data in *D* cell can be transmitted to the output. The operation of proposed *D* flip flop is illustrated in Table II.

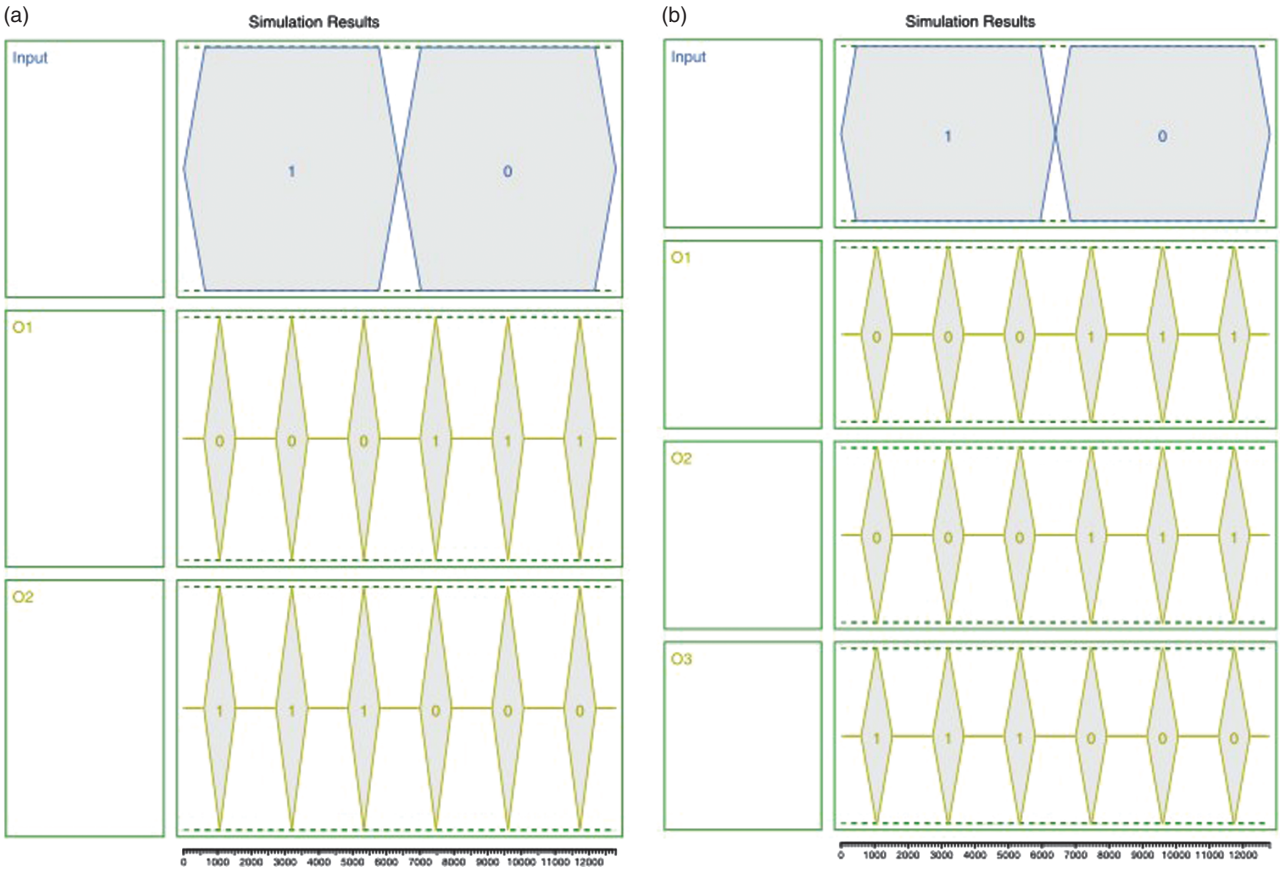

Fig. 21. (a) The simulation result of the conventional wiring scheme in Figure 13(a). (b) The simulation result of proposed wiring scheme in Figure 13(b).

Several types of convertors have been introduced in Refs. [16, 22] to implementation of an edge triggered QCA *D* flip flop. If the clock signal with one clock cycle delay (which called old clock) and the inversion of the clock signal have been arrived to the converter's majority gate at the same clocking zone, falling edge convertor will be constructed. If the majority gate has been received the inversion of clock signal with one clock cycle delay and

Fig. 22. Simulation results of the offered structures (a) presented in Figure 15 (b) presented in Figure 19(b) (c) presented in Figure 16 (d) presented in Figure 17.

the clock signal simultaneously, rising edge convertor will be constructed. The proposed rising and falling converters (shown by red square) which are connected to the presented *D* flip flop (Fig. 15) are demonstrated in Figures 16, 17, respectively. In Figure 16, the output of rising edge converter's majority gate that is indicated using the O1 pointer has been set to "1", only in transition of the clock signal from "0" to "1." In Figure 17, when the old clock signal is equaled to "1" and the clock signal is equaled to "0", the output of falling edge converter's majority gate has been set to "1," so the input data in *D* cell can be propagate to the output. For respect to synchronization of input streams in both designs, additional cells have been placed in input wires.

As mentioned before, the main idea of using this kind of wiring is simplicity and regularity of design. Both designs uses 2.5 clock cycle to data propagation from input to the output with least wasted area. The complete operation of rising edge triggered *D* flip flop and falling edge triggered *D* flip flop are shown in Tables III, IV, respectively.

Furthermore, a new robust architecture for dual edge converter has been proposed which is shown by red square in Figure 18. The dual edge triggered *D* flip flop is constructed by linking this converter and the presented *D* flip flop in Figure 15. This design enjoys least area occupation and optimized clock cycle number. It employs only 2.75 clock cycle to validate the output rather than previous designs. In rising and falling edge of the clock, the output of dual edge converter, which is shown by O1 pointer, is set to "1", consequently the input signal in *D* will be transmitted to the output in both edges of clock. The complete operation of proposed structure is demonstrated in Table V.

As noted earlier, a novel level sensitive *T* flip flop based on the presented MUX 2:1 is also introduced (Fig. 19(b)). The proposed structure utilizes 1.5 clock cycle to transmit the input signal to the output and also so dense in cell numbers and consumed area in comparison to state-of-the-art. A schematic of QCA operational circuit is illustrated in Figure 19(a). This design includes four robust majority gates, when the clock signal have been set to "1", the output of first majority gate, which is shown by O1 pointer, will be depended to *T*, absolutely. As it is shown in Table VI, if the $T =$ "0", last value of *T* flip flop will be saved whereas if the $T =$ "1", last value of *T* flip flop will be reversed.

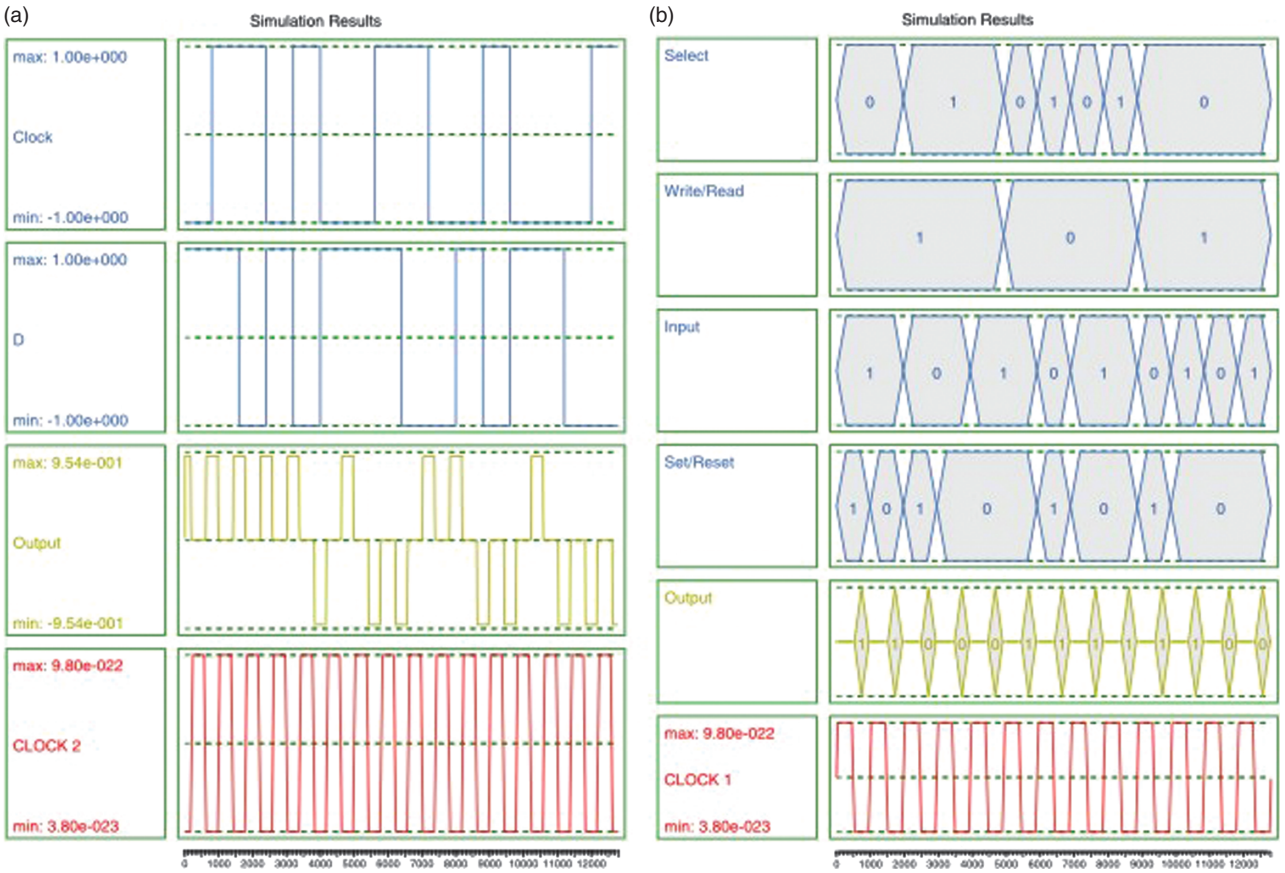

Fig. 23. (a) The simulation results of the proposed dual edge triggered *D* flip flop in Figure 18. (b) The simulation result of proposed RAM structure with set/reset ability in Figure 20(b).

4. THE PROPOSED RAM CELL STRUCTURE

The schematic of RAM cell structure with set and rest ability which has been presented in Ref. [22] is shown in Figure 20(a). This design has been constructed using two MUX 2:1 which linking together. The layout of proposed RAM cell architecture based on the offered *D* flip flop and multiplexer 2:1 in Figures 15 and 14(b) are shown in Figure 20(b). In this design, the MUX1 includes two input signals (set/reset, input) and one select signal; the MUX2 has accepted the output of the MUX1 as the second input and its output signal as the first input. The Select signal is used to enable RAM cell, when the select signal is activated, write operation will be performed by setting the Write/Read signal to "1" whereas Read operation will be accomplished by fixing it to "0". When the RAM cell has not enabled via select signal, set or reset operation will alter the memory cell's content to "1" or "0", respectively (Table VII).

Table VIII. Comparison results of the presented flip flop structures.

QCA flip flop designs	Hardware requirement (cell number)	Area occupation (μm^2)	Latency (clock cycle)	Cross over type
The Level triggered *D* flip flop in Ref. [23]	68	0.08	1.5	Coplanar
The level triggered *D* flip flop in Ref. [22]	48	0.05	1	–
The level triggered *T* flip flop in Ref. [23]	92	0.10	1.25	Coplanar
The raising edge triggered *D* flip flop in Ref. [22]	84	0.09	2.75	–
The falling edge triggered *D* flip flop in Ref. [22]	84	0.09	2.75	–
The raising edge triggered *D* flip flop in Ref. [14]	75	0.07	1	Coplanar
The dual edge triggered *D* flip flop in Ref. [22]	120	0.14	3.25	–
The proposed level triggered *D* flip flop in Figure 15	33	0.03	1	–
The proposed level triggered *T* flip flop in Figure 19(b)	55	0.06	1.5	–
The proposed raising edge triggered *D* flip flop in Figure 16	68	0.07	2.5	–
The proposed falling edge triggered *D* flip flop in Figure 17	69	0.07	2.5	–
The proposed dual edge triggered *D* flip flop in Figure 18	108	0.11	2.75	–

As mentioned above, there is a significant Matter in memory design that all input signals must be synchronized. To implementation of this object, excess cells have been placed in Read/Write wire, as demonstrated in Figure 20(b). This architecture is so efficient in term of complexity and speed. It uses only 1.5 clocking cycle to compute the output's value, rather than earlier designs.

5. SIMULATION AND RESULTS

In this section, simulation results of the proposed structures are provided using the coherence vector and bistable approximation engines of the QCA Designer version 2. 0. 3.[33] Both engines have used default values of parameters and produced similar outcomes. Verification analysis of the traditional and the proposed wiring method are illustrated in Figures 21(a), (b), respectively. As it is clear, in Figure 21(b), the input signal is transmitted to the O3 with no latency and also its inversion received at O1 and O2 simultaneously.

In Figures 22(a)–(d), the simulation results of proposed level sensitive *D* flip flop, level sensitive *T* flip flop, raising edge triggered *D* flip flop and falling edge triggered *D* flip flop are indicated, respectively. The simulation results of dual edge triggered *D* flip flop and RAM cell with set/reset ability are also illustrated in Figures 23(a), (b). For instance, as it shown in Figure 23(a), in the both edge of the clock (transmission from "1" to "0" and from "1" to "0") the output signal has been changed due to *D* signal after 2.75 clock cycle. It is obvious that in the rising or falling edge triggered *D* flip flop, the output value will be changed after 2.5 clocking cycle at one of these states (Figs. 22(c), (d)).

Applying of new wiring scheme in the presented QCA circuits leads to successful outcomes. The comparison results between the proposed memory architectures and various designs are shown in Tables VIII, IX. It can clearly be perceived that all of the proposed designs have a robust, simple and regular structure with reduction in area occupation, cells number and clocking zones number. Moreover

Table IX. Comparison results of the presented RAM structures.

QCA memory designs	Set/ reset ability	Hardware requirement (cell number)	Area occupation (μm^2)	Latency (Clock cycle)	Cross over type
The SR-Latch based RAM structure in Ref. [21]	No	100	0.11	3	Coplanar
The *D*-Latch based RAM structure in Ref. [21]	No	63	0.07	2	–
The *D*-Latch based RAM structure in Ref. [22]	Yes	109	0. 13	1.75	–
The proposed *D*-Latch based RAM structure in Figure 20(b)	Yes	74	0.08	1.5	–

these designs are more accurate than preceding structures. The proposed level sensitive *T* flip flop (Fig. 19(b)) has an extreme diminution in consumed cell numbers and area in contrast to presented *T* flip flop in Ref. [23] The proposed dual edge triggered *D* flip flop (Fig. 18) occupies 0.11 μm^2 and the circuit latency is two clocking zones less than previous structure in Ref. [22] (Table VIII). As it shown in Table IX, there is an improvement of efficiency in RAM structure with set/reset ability due to great reduction of Thirty five cells in the circuit complexity and 0.05 μm^2 in wasted area. The propagation delay of proposed design is also one clocking zone less than previous RAM cell in Ref. [22] The presented study investigates on the memory structures design using QCA device. Construction process of Quantum dot cellular automata's cell needs to particular types of matters, further types are exposed in Refs. [30–32]. Nowadays QCA can be based on the interpretation of modern quantum theory which is still an open question, as is illustrated in Ref. [28].

6. CONCLUSION

In this paper, a novel approach for QCA wiring is presented which leading to improvement of robustness, simplicity, regularity and speed of computation in QCA logic designs. In order to illustrate usefulness of this new method, various memory structures have been implemented. A level sensitive *D* flip flop, *T* flip flop, a rising and falling edge triggered *D* flip flop and also a dual edge triggered *D* flip flop are presented. Furthermore a *D*-latch based RAM structure with set and reset ability has been proposed. Comparison outcomes with previous designs which are attained using QCADesigner tool show an abundant decrement in cell counts, occupation area, clocking zones number in presented structures. Valuable achievements of these architectures can be used in larger QCA buildings.

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