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Research paper

Content addressable memory cell in quantum-dot cellular automata

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ABSTRACT

Quantum-dot cellular automata (QCA) is an alternative to the CMOS circuits based on the characteristics of confinement and mutual repulsion between electrons. QCA can be used in designing ultra-dense, low-power, high speed and high-performance structures at nanoscales. Since memory is a very important part of each computer system, designing a high speed QCA memory is a significant issue. Content addressable memory (CAM) is a special type of memory structures which is used in a certain very fast searching applications. In this paper, a new five input minority gate-based CAM cell is introduced. QCADesigner has been used for simulation of the proposed structure and verifying its operation.

1. Introduction

Until recently, the exponential scaling in feature size has been successfully achieved by CMOS technology. However, in recent years, there is remarkable evidence such as leakage current and high power consumption [1] that emerging technologies such as quantum-dot cellular automata will be required to minimize these limitations [2–7]. QCA is a promising replacement for the current most used silicon-based paradigm since QCA might be executed in high frequency with low power consumption and least feature size [8,9]. QCA is based on the confinement and mutual repulsion of electrons. The fundamental element in QCA is a squared cell with four dots and two excess electrons. Due to the Columbic interaction, these electrons occupy the dots diagonally.

QCA has many desirable features for processing [10]; for example, clocking and timing can be adjusted as a function of the cells in a Cartesian layout. Low power consumption, high density, and regularity are readily applicable to QCA; therefore, memory is well suited for implementation using this technology. Unlike semiconductor-technology-based (e.g., CMOS) memories, in QCA-based architectures, memory must be maintained in motion, that is, the memory state has to be continuously moved through a set of QCA cells. This continuous movement necessitates a remodeling of memory design for QCA implementation. There are two common types proposed for a one-bit memory cell in QCA so far: The loop-based memory cell [11] and the line-based memory cell [12]. The line-based memory cell stores data bits propagating back and forward on a line of QCA cells [12,13]. Line-based memory cells require additional clock zones which make their implementation complex. However, the loop-based memory stores data bits circulating on a feedback-loop of QCA cells. As the implementation of a loop-based memory cell makes use of no additional clock zones, they are preferred more.

Efficient QCA memory design is a problem that has been brought the attention of the research community. Many works such as [11,15,26–31] focus on this problem. But these works have been done on RAM model, where the each memory location is accessed by a specific address. Our work describes CAM, which is different from RAM model since each memory location in CAM is accessed by the content. CAM is a special type of memory which is used in a certain very high speed searching applications. The required time to find an item stored in the memory can be reduced considerably if the stored data can be identified by content instead of addresses [14].

The main contribution of this study is to present a new five-input minority gate-based CAM cell. For this purpose, first, we introduce the new five-input majority gate and subsequently five-input minority gate. Second, we design and implement five-input minority gate-based CAM cell. Finally, we evaluate operation of proposed CAM cell using QCADesigner [15].

The rest of this paper is organized as follows: Section 2 provides a background on QCA and CAM. QCA circuits are reviewed in Section 3. The new memory cell schematic and its QCA design will be explained in Section 4. Simulation results (based on QCADesigner) and discuss

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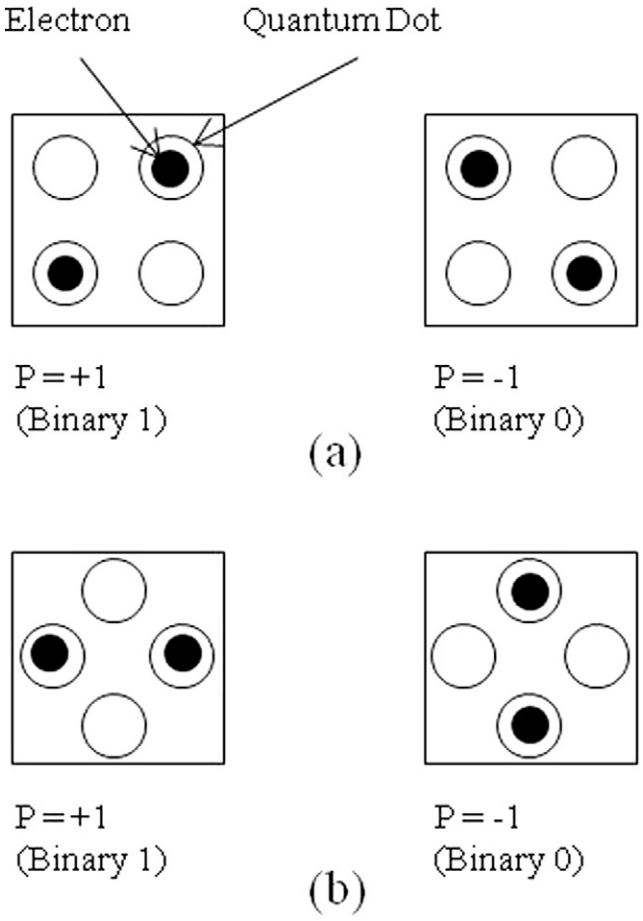


Fig. 1. Polarization states of QCA cells; (a) 90-degree cells, (b) 45-degree cells.

assessment are presented in Section 5 and then conclusion is appeared at the end.

2. Background

In this section, an overview about basic features of QCA and CAM is presented.

2.1. QCA

QCA is one of the promising new device architecture that gives a solution at nanometer scale [9]. This technology is based on a cellular approach that offers a new method of computation and information transformation [8,16]. QCA stores logic states not as current employed in CMOS but, rather, based on the position of individual electrons in the cell [8]. A quantum cell consists of four dots, positioned at the corners of a square cell. Computation is realized by the Columbic interaction of extra electrons in quantum dots. Each quantum dot is a nanometer-scaled square at each corner of the cell. The two extra electrons that are present in each cell can quantum tunnel between dots. The extra electrons occupy diagonally opposite dots due to electron repulsion. Binary information in the cells is encoded by formations of these two electrons (also named cell polarizations P). They make two different polarizations; $P = -1$ and $P = +1$ corresponding to binary states 0 and 1, respectively. Fig. 1 shows the two types of QCA cells (90-degree and 45-degree) with their binary behavior.

In order to build more complex QCA structures, needs to synchronize the information to moderate the data flow direction (thus computation) [17]. This feature that can guarantee the proper operation of QCA circuits is achieved by QCA clock. The clock can be applied to groups of cells (clock zones). In each zone, a set of QCA cells based on their placement are doing a certain operation and its output is used as input to the next clock zone.

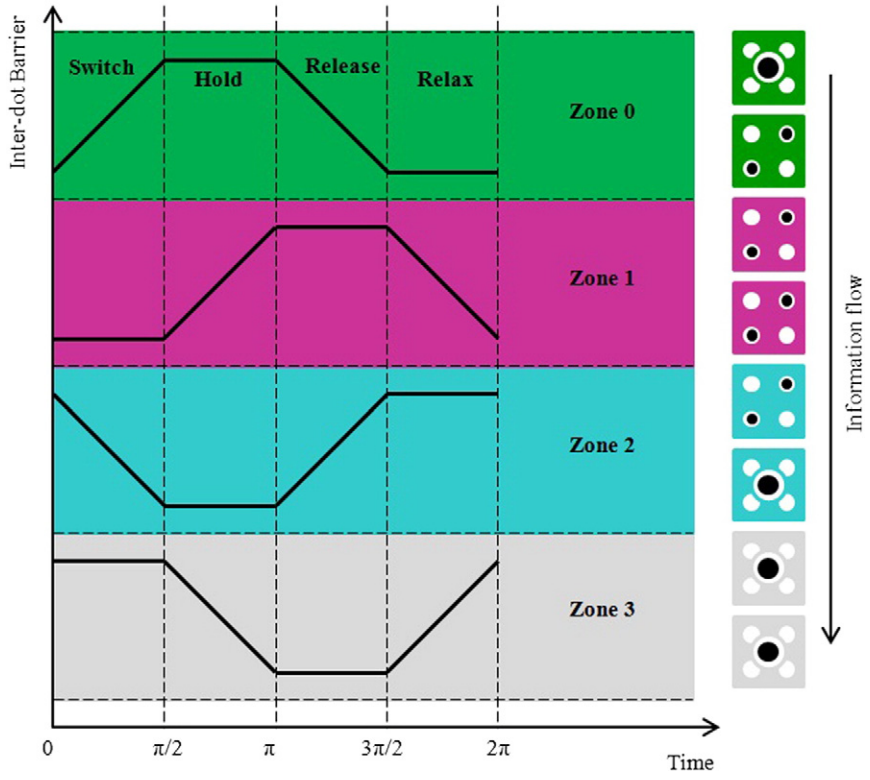


Fig. 2. QCA clocking scheme and its effect on a QCA wire.

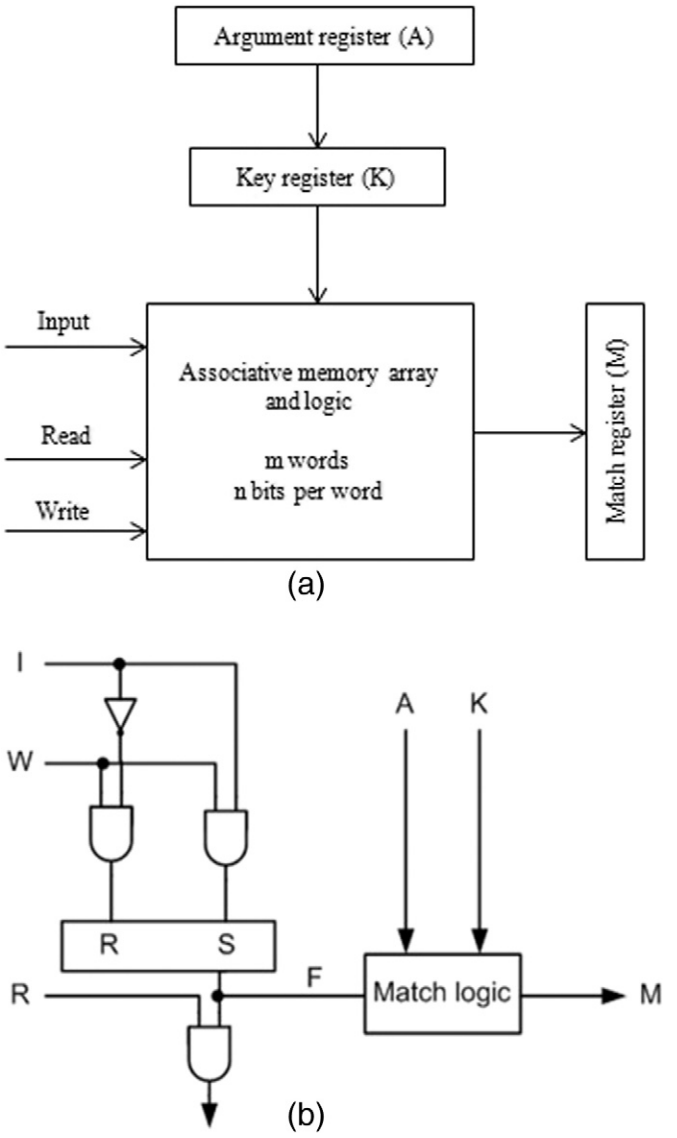


Fig. 3. Block diagram of a) organization of CAM and b) internal organization of a typical CAM cell.

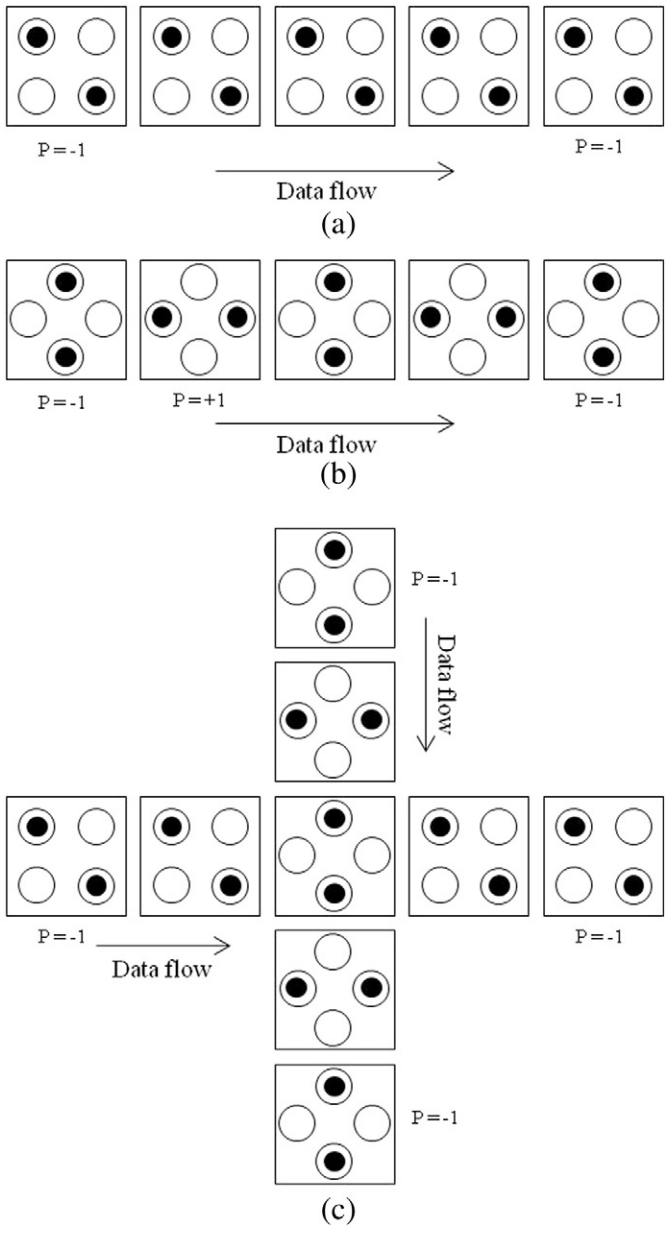


Fig. 4. Data propagation with a) 90-degree QCA wire, b) 45-degree QCA wire, c) coplanar wire crossing.

The QCA adiabatic clocking scheme [9,17], is illustrated in Fig. 2, has been widely adopted by researchers. In this scheme, the clock signal has four different phases, Switch, Hold, Release and Relax with 90-degree phase shift from each other. The cell becomes polarized by enabling the Columbic interaction with neighboring cells in the Switch phase. By taking a certain polarization, the cell stores current situation during the Hold phase. Cell polarization is reduced and eventually lost through the Release and Relax phases [17–19].

The polarization of a QCA cell which is determined by the Columbic interaction between QCA cells, namely kink energy, can be computed using the electrostatic interaction between all electrons in two neighboring cells, i and j, as:

$$E^{i,j} = \frac{1}{4\prod\varepsilon_0\varepsilon_r}\sum_{n=1}^{4}\frac{q_n^i q_m^j}{|r_n^i - r_m^j|} \tag{1}$$

where ε_0 is the permittivity of free space, ε_r is the dielectric constant, q_n^i is the charge in dot n of cell i, r_n^i is the position of dot n in cell i and $|r_n^i - r_m^j|$ is the distance between cells.

The kink energy between two cells is defined as the difference in energy between those which have opposite polarizations and those same two cells which have the same polarization:

$$E_{kink}^{n,m} = E_{P_n \neq P_m}^{n,m} - E_{P_n = P_m}^{n,m} \tag{2}$$

According to the recent equation, the polarization of each of the cells can be computed by Eq. (3) [32,33].

$$E^{i,j} = \frac{\frac{E_{kink}^{i,j}}{2\gamma}\sum_j P_j}{\sqrt{1+\left(\frac{E_{kink}^{i,j}}{2\gamma}\sum_j P_j\right)^2}} \tag{3}$$

where P_i is the polarization state of the cell, and P_j is the polarization state of the neighboring cells. γ is the tunneling energy of electrons

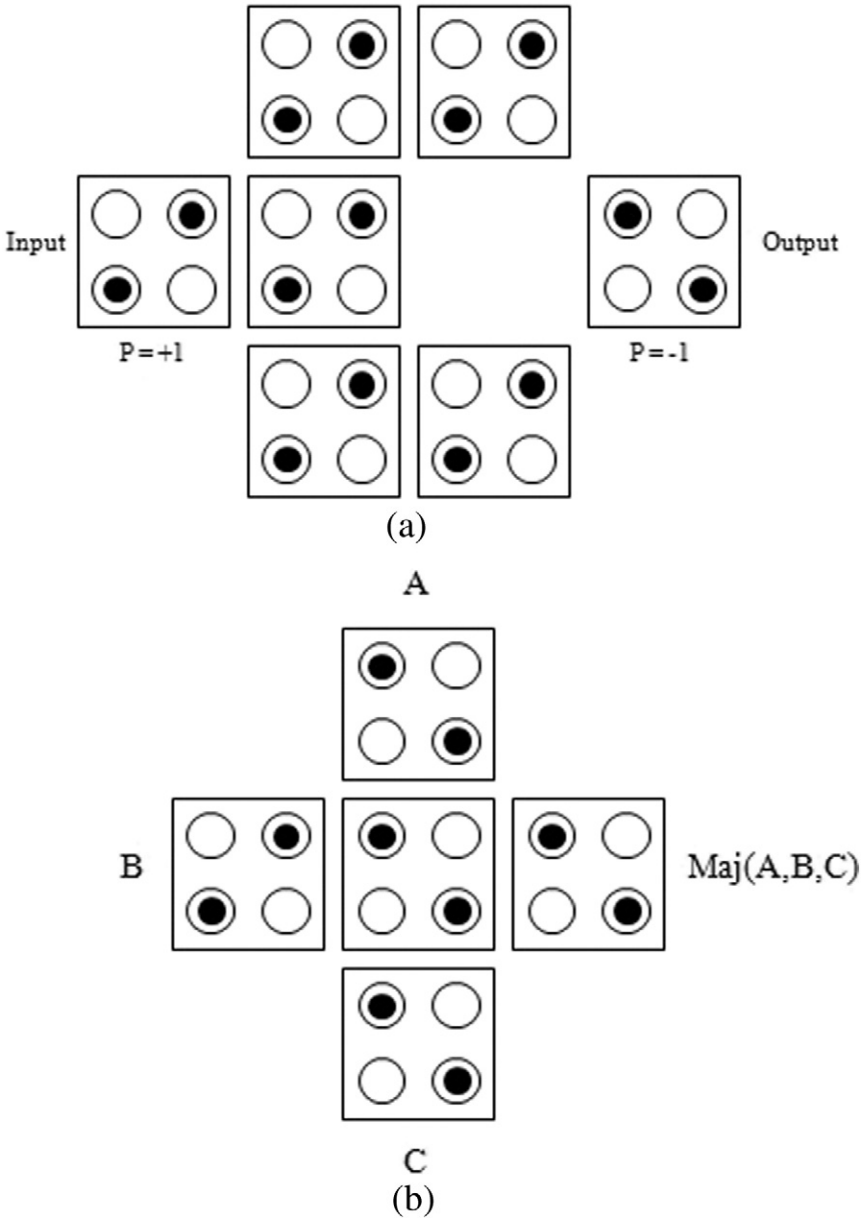


Fig. 5. Two fundamental QCA gates; a) inverter gate, b) three-input majority gate.

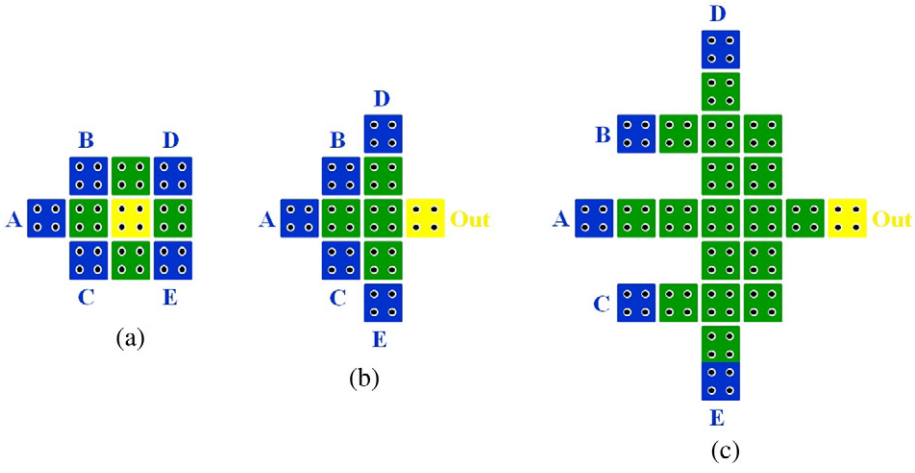


Fig. 6. QCA five-input majority gate; a) the presented structure in [23], b) the presented structure in [24], c) the presented structure in [25].

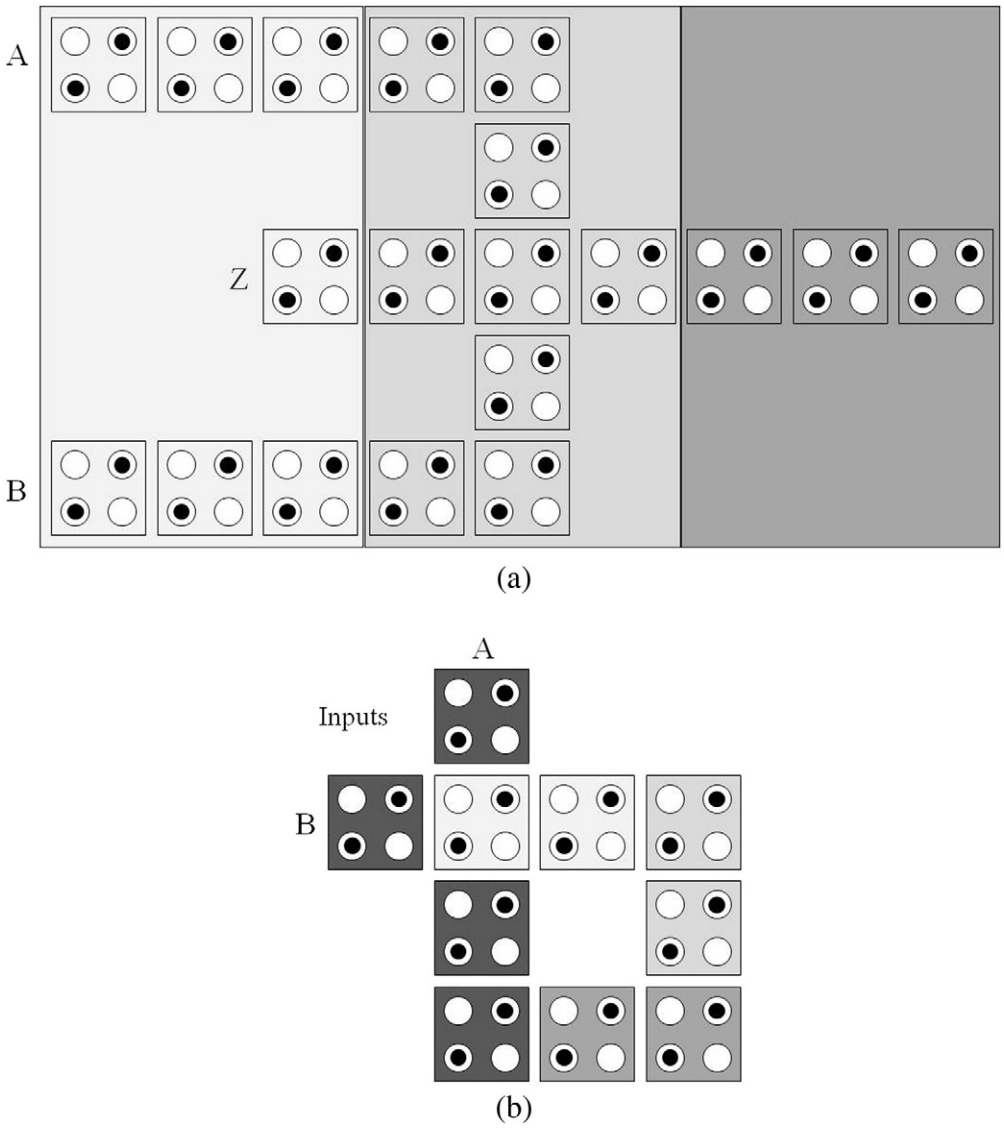


Fig. 7. Two common types of memory cell architectures in QCA; a) line-based memory cell, b) loop-based memory cell.

within the cell. The tunneling barriers' heights are controlled by QCA clock [32–34].

2.2. CAM

CAM accesses data using the content of the data itself. It is also known as associative memory, associative storage, or associative array. Compared to finding an item by its address, the required time to find an item can be reduced considerably if we know the content of that item [14,35]. Because of its associative memory organization, this memory is uniquely suited for parallel searches by data association. Each location in CAM, as illustrated in Fig. 3(a) and (b), has storage capacity as well as logic circuits for matching its content with an external argument. The overall operation of a CAM is to take a search word as a key and return the matching memory location as a result [20].

3. QCA circuits

In this section, the elementary components of QCA circuits are explained. Then, the fundamental QCA gates are presented. In addition, the common types of memory cell designs in QCA are reviewed.

3.1. Elementary components

The wire, inverter and three-input majority gates are the elementary components of QCA circuits. As it is shown in Fig. 4(a), the 90-degree QCA wire is constructed by cascading QCA cells to propagate a binary value from one side to the other based on Coulomb interactions. Fig. 4(b) illustrates 45-degree QCA wire where the polarization of each cell will be opposite of its neighbor cell [21]. Coplanar wire crossing is achieved using these two types of wires in a orthogonal form as

Table 1
Truth table for proposed five-input minority gate based on sum of the input values.

Sum (A, B, C, D and E)	Min (A, B, C, D and E)
0	1
1	1
2	1
3	0
4	0
5	0

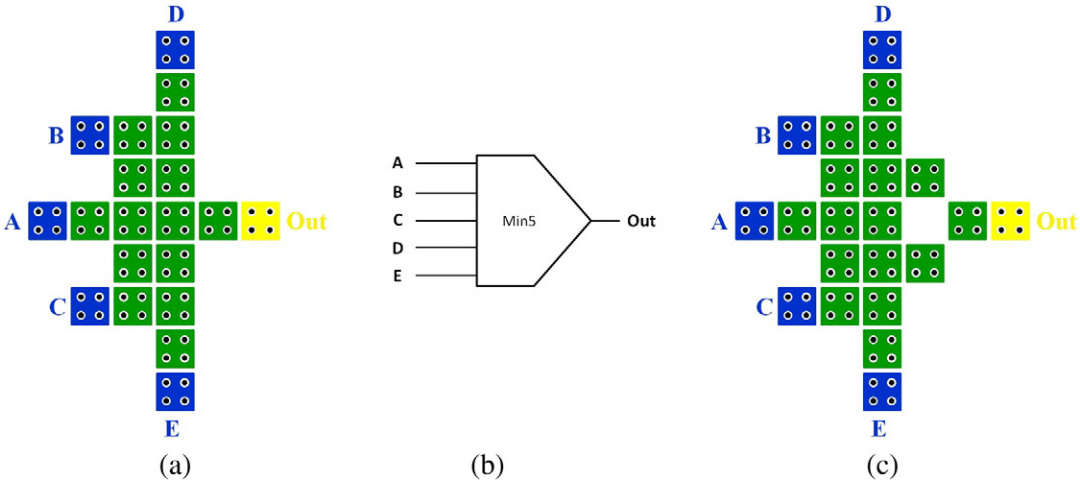


Fig. 8. Proposed designs; a) QCA layout of five-input majority gate, b) schematic of five-input minority gate, c) QCA layout of five-input minority gate.

shown in Fig. 4(c) [22]. In this technique, the binary values are propagated in two wires independently.

3.2. Fundamental gates

Two fundamental QCA gates, inverter and majority gates, are depicted in Fig. 5. QCA implementation of an inverter is illustrated in Fig. 5(a). The input signal divided into two QCA wires and consequently the complement of it is appeared at the merging point [8]. As it is shown in Fig. 5(b), QCA three-input majority gate implements the majority function of its three inputs A, B, and C as Maj(A,B,C) = AB + AC + BC. By setting the polarization of one input cell to constant value of −1 or +1, majority gate functionality behaves like a two-input AND or OR gate, respectively.

Three types of single-stage five-input majority gate have been introduced in [23,25] which are shown in Fig. 6. The logic function of five-input majority gate is

$$\begin{aligned} \mathrm{Maj}(A,B,C,D,E) = (&ABC + ABD + ABE + ACD + ACE \\ &+ ADE + BCD + BCE + BDE + CDE) \end{aligned} \tag{4}$$

In the first scheme, which is presented in [23] and is shown in Fig. 6(a), a five-input majority gate using only ten cells is implemented. The output of this scheme is surrounded by the input cells therefore can be accessed to it in another layer. In the later, which is presented in [24] and is shown in Fig. 6(b), input cells are adjacent to each other. In the recent scheme, which is presented in [25] and is shown in Fig. 6(c), majority gate takes all five input signals in one direction at the first clocking zone.

3.3. Memory cell structures

As mentioned earlier, due to main features of nanotechnology, QCA is an attractive technology for the development of high density and low power memories. Generally there are two common types of memory cell designs in QCA which are categorized as line-based memory cell [12] and the loop-based memory cell [11] according to the operational behavior of the QCA circuits. The line-based memory cell stores data bits propagating back and forward on a line of QCA cells [12,13], which is illustrated in Fig. 7(a). Line-based memory cells require additional clock zones which make their implementation complex. However, the loop-based memory cell stores data bits circulating on a feedback-loop of QCA cells, which is illustrated in Fig. 7(b). As the implementation of a loop-based memory cell makes use of no additional clock zones, they are preferred more.

An improved line-based memory cell has been proposed in [14]. This new structure of the memory cell requires only two new clocking zones. Moreover, read throughput is improved to one operation per clock cycle.

An addressable S-RAM cell, as well as, a memory system based on addressable shift registers using the SQUARES formalism has been presented in [11]. The use of SQUARES for big circuits is not recommended as it presents an extra cost both in terms of access time and spatial redundancy.

A layout of a conventional random access memory (RAM) structure using QCA has been presented in [10]. The presented structure is based on D-latch and a loop is used for storing the memory content. It also consumes two clocking cycles to transmit the input signal to the output.

A QCA random access memory without set and reset ability has been suggested in [29]. This structure has a loop-based mechanism and is constructed based on SR-latch. Coplanar wire crossing method has been employed in this structure. Another structure for RAM cell is presented in [29] with the same operation. This structure has been based on D-latch with an un-robust three-input majority gate structure.

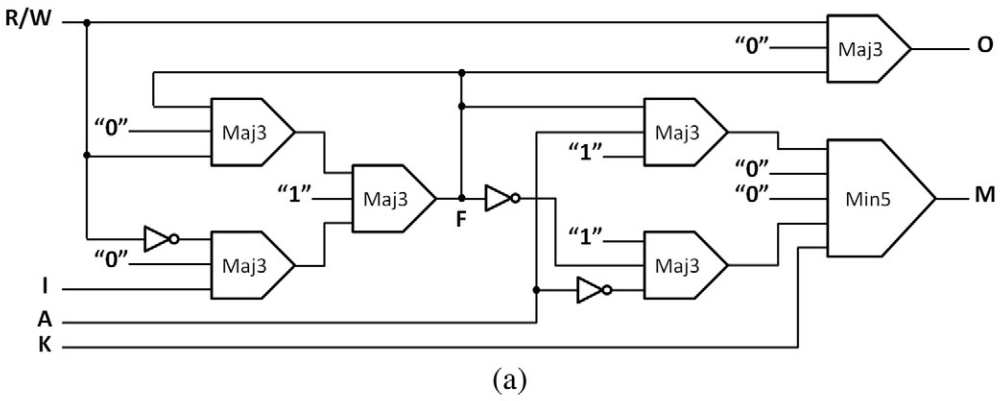
RAM cell structure with set and reset ability has been presented in [30]. This structure is composed of two 2:1 multiplexers. The new designs of Flip Flops and RAM with minimum number of cells by using a new wiring approach have been presented in [31].

In a recent work [15], a robust five-input majority gate is presented which is appropriate for implementation of simple and efficient QCA circuits in single layer. By employing this structure, a novel RAM cell structure with set and reset ability has been proposed.

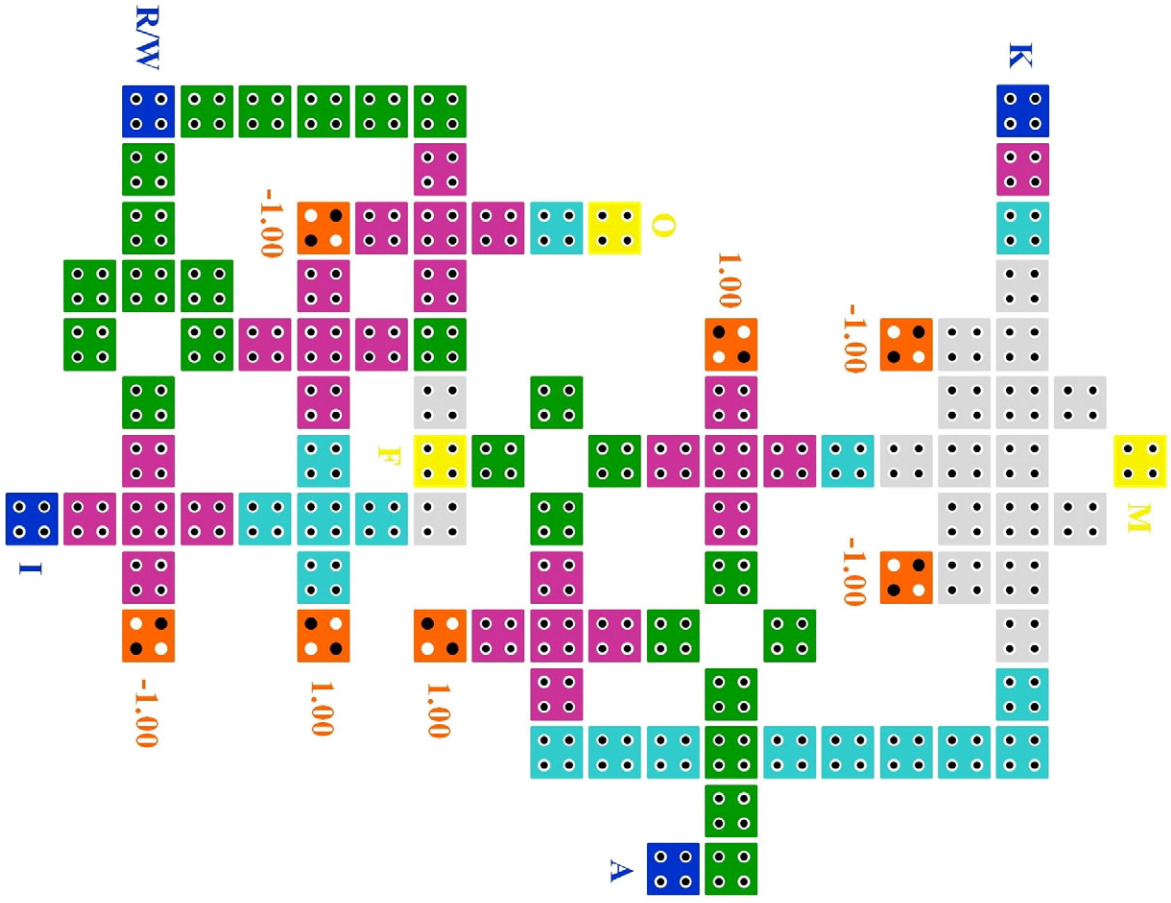
Unlike previous described works which utilize the RAM model, where the each memory location is accessed by a specific address, our work describes CAM, which is different from RAM model since each memory location in CAM is accessed by the content instead of addresses.

4. Proposed structure

This section describes the proposed structure of five-input minority gate-based CAM cell. For this purpose, first, we introduce the new five inputs QCA minority gate and then describe the structure of five-input minority gate-based CAM cell using QCA cells.



(a)



(b)

Fig. 9. Proposed CAM cell structure; a) schematic of the proposed CAM cell structure, b) QCA layout of proposed CAM cell structure using the five-input minority gate in Fig. 8(c).

Table 2
Truth table for memory operation.

Type of operation	*R/W*	*I*	Previous *F*	*F*	*O*
Write	0	1	X	1	0
Write	0	0	X	0	0
Read	1	X	1	1	1
Read	1	X	0	0	0

Table 3
Truth table for match operation.

K	A	F	M
0	X	X	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

4.1. Five-input minority gate

As mentioned earlier, majority gate and subsequently minority gate are fundamental structures in QCA designs which are used to construct the other various useful QCA gates. Hence, in this section a five-input minority gate is presented. The logic function of five-input minority gate is

$$\mathrm{Min}(A,B,C,D,E) = (\overline{ABC + ABD + ABE + ACD + ACE + ADE + BCD + BCE + BDE + CDE}) \quad (5)$$

By setting two of the five input cells' polarizations to -1 or $+1$, a three-input NAND gate and a three-input NOR gate can be formed, respectively. A truth table of a five-input minority gate based on sum of the inputs is shown in Table 1.

As can be inferred, five-input minority gate can be created by applying a little changes in the five-input majority gate. In the first scheme of five-input majority gate, which is presented in [23] and is shown in Fig. 6(a), the output cell is surrounded by the input cells therefore preventing access to it in one layer. In the later, which is presented in [24] and is shown in Fig. 6(b), input cells are adjacent to each other therefore causing unwanted effect on one another (for example inputs B and D or inputs C and E). In the recent scheme, which is presented in [25] and is shown in Fig. 6(c), majority gate takes all five input signals in one direction at the first clocking zone. When this scheme is applied to construct a minority gate, the results are not robust and so this scheme is not proper to construct a minority gate.

Our proposed structures for five-input majority gate and five-input minority gate are demonstrated in Fig. 8.

There are 20 and 22 cells in the proposed five-input majority gate and five-input minority gate, respectively. Five of cells labeled A, B, C, D, and E are input cells, one of them is the output cell and the remaining cells are device cells in both structures. Polarization of input cells is fixed and device cells and output cell is free to change.

Table 4
Simulation parameters.

Parameter	Value
Cell size	18 nm × 18 nm
Dot diameter	5 nm
Number of samples	12,800
Convergence tolerance	0.001000
Radius of effect	65.000000 nm
Relative permittivity	12.900000
Clock high	9.800000e−022
Clock low	3.800000e−023
Clock shift	0.000000
Clock amplitude factor	2.000000
Layer separation	11.500000
Maximum iterations per sample	100
Temperature	1.000000
Relaxation time	1.000000e−015
Time step	1.000000e−016
Total simulation time	7.000000e−011

4.2. Five-input minority gate-based CAM cell

The schematic and QCA implementation of proposed CAM cell are illustrated in Fig. 9(a) and (b), respectively. This design is composed of six three-input majority gates and one five-input minority gate which is presented in Fig. 8(c). This circuit has two components, one of which is memory unit and another is match unit. The memory unit receives the read/write signal (marked as *R/W*) and also data input (marked as *I*)·The match unit receives the content of memory cell (marked as *F*) and also the argument and key signals. The circuit gives as output (marked as *O*) the content of cell where the data have been read and also sets the match signal (marked as *M*) where the data have been found. Table 2 shows the truth table for the memory operation and Table 3 shows the truth table for the match operation.

In proposed design when the *R/W* signal has been set to "0", input data will be transmitted to the output *F* and consequently write operation will be done. Moreover, read operation has been done by setting the *R/W* signal to "1". The value of previous *F* is transmitted to the output *F* and also to the output *O* in read operation. When the *K* signal has been set to "0", regardless of the values of *A* and *F*, the match signal *M* will be set to "1". But when the *K* signal has been set to "1", the match signal *M* will be set to "1" if the values of *A* and *F* are equal and will be set to "0" if the values of *A* and *F* are not equal.

5. Simulation results

In this section, simulation results of the proposed structures are verified using QCADesigner version 2.0.3 [15]. Proposed structures were simulated using the Coherence Vector simulation engine and also Bistable Approximation simulation engine with default parameters shown in Table 4 and similar outcomes were achieved from both simulation engines. Gallium arsenide material parameters have been considered in our QCA model.

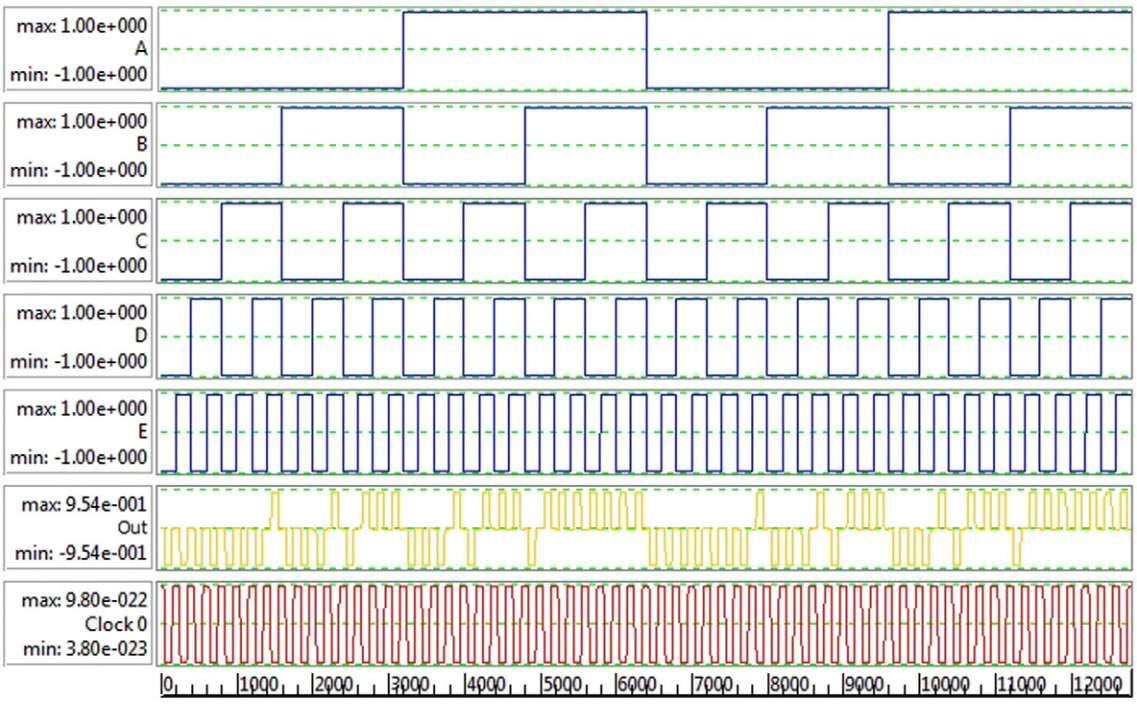
The simulation results of the presented five-input majority and minority gates are illustrated in Fig. 10. The majority and minority of input cells' polarizations (A, B, C, D and E) determine the value of output in majority gate and minority gate, respectively. Analysis of the achieved results confirms that the presented QCA structures work correctly.

The simulation result of the presented CAM structure is illustrated in Fig. 11. The waveform in Fig. 11 shows that the proposed CAM structure works correctly and expected operations are performed. Table 5 reports the implementation results for the proposed CAM cell structure and the previous RAM cell designs.

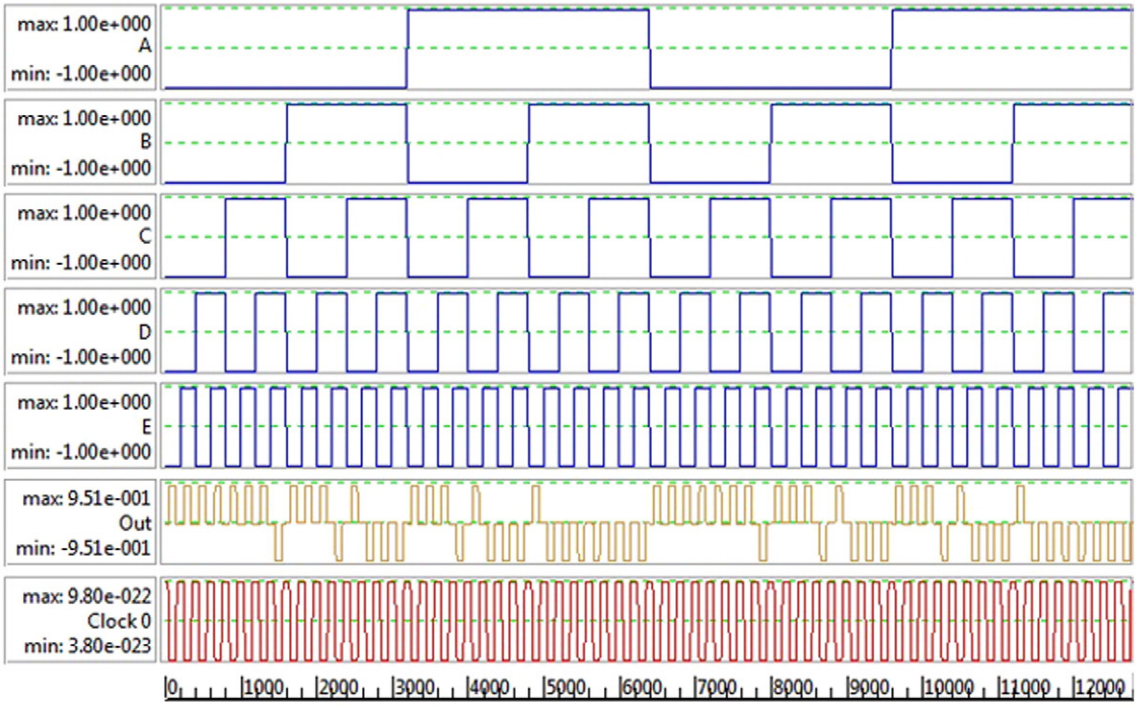
We have also investigated the effect of temperature fluctuations on output polarization of proposed CAM cell. Fig. 12 shows the result of this analysis. It can be seen that the polarization of the output *O* is slumped after 18 K and the polarization of the output *M* is reduced with gentle slope and eventually lost at 27 K.

6. Conclusion

In this paper, a novel robust five-input majority gate and subsequently the five-input minority gate for quantum-dot cellular automata have been proposed. These components can be used to design the various useful QCA circuits. By utilizing this gate, we proposed and implemented a five-input minority based content addressable memory (CAM). We implemented these two QCA structures using the QCADesigner. Simulation results demonstrated functionalities of these proposed structures and validated the architectures.



(a)



(b)

Fig. 10. Simulation results of a) presented five-input majority gate in Fig. 8(a) and b) presented five-input minority gate in Fig. 8(c).

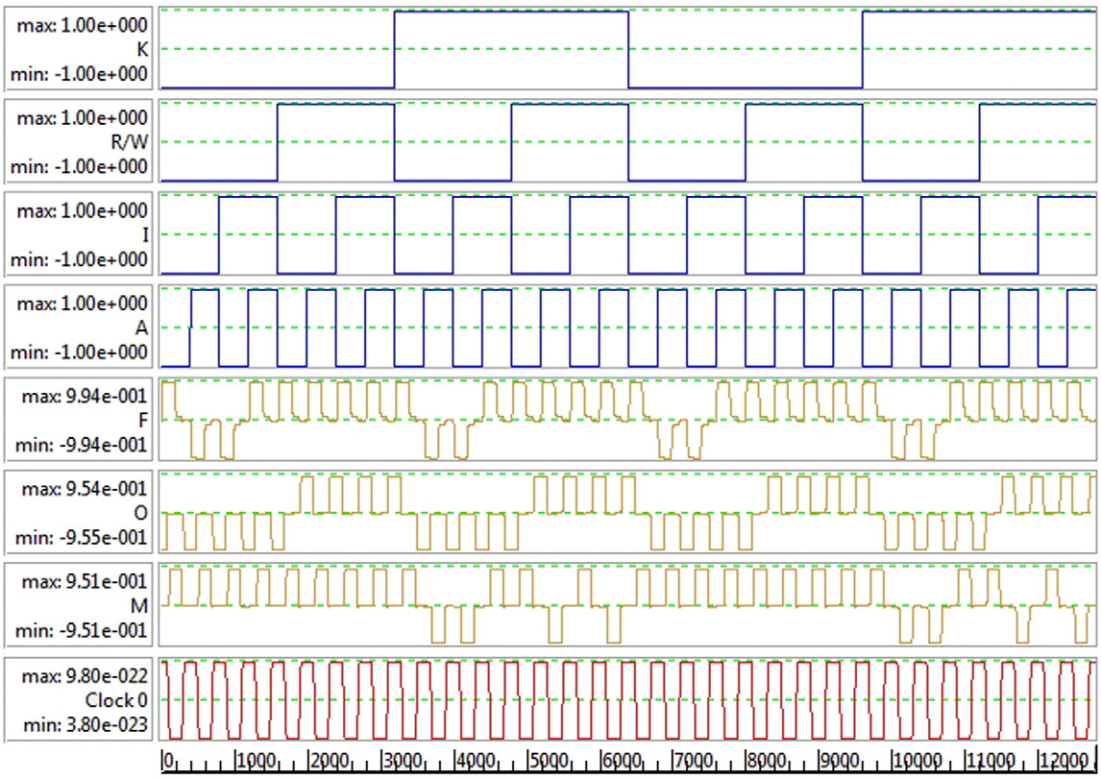


Fig. 11. Simulation result of presented CAM cell in Fig. 9(b).

Table 5
Implementation results for presented memory cell structures.

Memory structure	Number of cells	Number of gates	Clock cycles	Occupation area (μm^2)
Presented RAM cell in [10]	158	8	2	0.16
Presented RAM cell in [30]	109	8	1.75	0.13
Presented RAM cell in [25]	88	5	1.5	0.08
Proposed CAM cell in Fig. 9(b)	100	10	2	0.14

7. Future works

For future works, we intend to analysis power consumption of proposed CAM cell and also expand it to construct a CAM block.

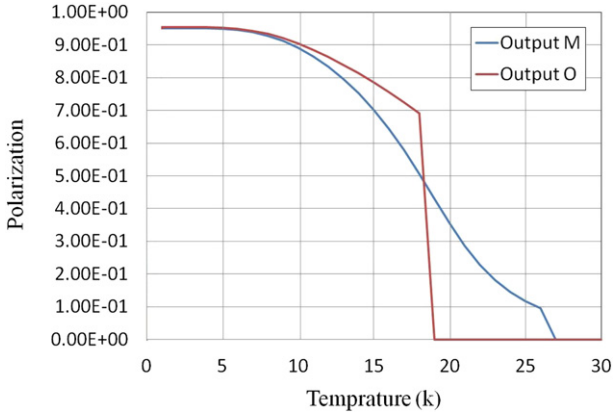


Fig. 12. The effect of temperature fluctuations on output polarization of proposed CAM cell in Fig. 9(b).

References

[1] R. Compano, L. Molenkamp, D.J. Paul, Technology roadmap for nanoelectronics, European Commission IST Programme, Future and Emerging Technologies, 2000.
[2] C.S. Lent, P.D. Tougaw, W. Porod, G.H. Bernestein, Quantum cellular automata, Nanotechnology 4 (n1) (1993) 49–57.
[3] M.T. Niemer, P.M. Kogge, Problems in designing with QCAs: layout = timing, Int. J. Circuit Theory Appl. 29 (2001) 49–62.
[4] G.H. Bernstein, A. Imre, V. Metlushko, A. Orlov, L. Zhou, L. Ji, G. Csaba, W. Porod, Magnetic QCA systems, Microelectron. J. 36 (2005) 619624.
[5] J. Huang, F. Lombardi, Design and Test of Digital Circuits by Quantum-dot Cellular Automata, Artech House, Inc, Norwood, MA, USA, 2007.
[6] W. Liu, L. Lu, M.O. Neill, E.E. Swartzlander Jr., Design rules for quantum-dot cellular automata, Proc. of the IEEE International Symposium on Circuits and Systems (ISCAS), Rio De Janeiro, Brazil May 2011, pp. 2361–2364.
[7] K. Kim, K. Wu, R. Karri, Towards designing robust QCA architectures in the presence of sneak noise paths, Proc. of the IEEE Design, Automation and Test in Europe Conference and Exhibition (DATE) March 2005, pp. 1214–1219 (Munich, Germany).
[8] P. Tougaw, C. Lent, Logical devices implemented using quantum cellular automata, J. Appl. Phys. 75 (3) (1994) 18181825.
[9] C. Lent, P. Tougaw, A device architecture for computing with quantum dots, Proc. IEEE 85 (4) (1997) 541557.
[10] K. Walus, A. Vetteth, G.A. Jullien, V.S. Dimitrov, RAM design using quantum-dot cellular automata, Technical Proc. Nanotechnology Conf. and Trade Show, vol. 2 2003, pp. 160–163.
[11] D. Berzon, T.J. Fountain, A memory design in QCAs using the squares formalism, Proc. Great Lakes Symp. VLSI Mar. 1999, p. 166169.
[12] V. Vankamamidi, M. Ottavi, F. Lombardi, A line-based parallel memory for QCA implementation, IEEE Trans. Nanotechnol. 4 (6) (Nov. 2005) 690698.
[13] B. Taskin, B. Hong, Improving line-based QCA memory cell design through dual phase clocking, IEEE Trans. VLSI 16 (12) (2008) 16481656.

[14] L. Chisvin, R.J. Duckworth, Content-addressable and associative memory: alternatives to the ubiquitous RAM, IEEE Comput. 22 (1989) 5164.
[15] K. Walus, T.J. Dysart, G.A. Jullien, R.A. Budiman, QCADesigner: a rapid design and simulation tool for quantum-dot cellular automata, IEEE Trans. Nanotechnol. 3 (1) (2004) 2631.
[16] A.O. Orlov, I. Amlani, G.H. Bernstein, C.S. Lent, G.L. Snider, Realization of a functional cell for quantum-dot cellular automata, Science 277 (1997) 928930.
[17] C.S. Lent, P.D. Tougaw, W. Porod, Bistable saturation in coupled quantum dots for quantum cellular automata, Appl. Phys. Lett. 62 (7) (1993) 714716.
[18] K. Kim, K. Wu, R. Karri, Quantum-dot cellular automata design guideline, IEICE Trans. Fundam. Electron. Commun. Comput. Sci. E89 (A(6)) (2006) 16071614.
[19] V. Vankamamidi, M. Ottavi, F. Lombardi, Two-dimensional schemes for clocking/timing of QCA circuits, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 27 (2008) 3444.
[20] K. Pagiamtzis, A. Sheikholeslami, Content-addressable memory (CAM) circuits and architectures: a tutorial and survey, IEEE J. Solid State Circuits 41 (3) (2006) 712–727.
[21] I. Amlani, A.O. Orlov, G. Toth, G.H. Bernstein, C.S. Lent, G.L. Snider, Digital logic gate using quantum-dot cellular automata, Science 284 (1999) 289291.
[22] K. Kim, K. Wu, R. Karri, The robust QCA adder designs using composable QCA building blocks, IEEE Trans. Comput. Aided Des. Integr. Circuits Syst. 26 (2007) 176183.
[23] K. Navi, S. Sayedsalehi, R. Farazkish, M. Rahimi Azghadi, Five-input majority gate, a new device for quantum-dot cellular automata, J. Comput. Theor. Nanosci. 7 (2010) 15461553.
[24] K. Navi, R. Farazkish, S. Sayedsalehi, M. Rahimi Azghadi, A new quantum-dot cellular automata full-adder, Microelectron. J. 41 (2010) 820826 (Elsevier).
[25] S. Angizi, S. Sarmadi, S. Sayedsalehi, K. Navi, Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata, Microelectron. J. 46 (2015) 4351 (Elsevier).
[26] S.E. Frost, A.F. Rodrigues, A.W. Janiszewski, R.T. Rausch, P.M. Kogge, Memory in motion: a study of storage structures in QCA, The First Workshop on Non-silicon Computing, vol. 2, 2002.
[27] M. Ottavi, V. Vankamamidi, F. Lombardi, S. Pontarelli, Novel memory designs for QCA implementation, The Fifth IEEE Conference on Nanotechnology, Vol. 2005, IEEE, Nagoya, Japan 2005, p. 545548.
[28] V. Vankamamidi, M. Ottavi, F. Lombardi, A serial memory by quantum-dot cellular automata (QCA), IEEE Trans. Comput. 57 (5) (2008) 606618.
[29] M.A. Dehkordi, A. Shahini Shamsabadi, B. Shahgholi Ghahfarokhi, A. Vafaei, RAM novel cell designs based on inherent capabilities of quantum-dot cellular automata, Microelectron. J. 42 (2011) 701708 (Elsevier).
[30] S. Hashemi, K. Navi, New robust QCA D ip op and memory structures, Microelectron. J. 43 (2012) 929940 (Elsevier).
[31] S. Angizi, K. Navi, S. Sayedsalehi, A.H. Navin, Efficient quantum dot cellular automata memory architectures based on the new wiring approach, J. Comput. Theor. Nanosci. 11 (11) (2014) 23182328.
[32] G. Toth, Correlation and Coherence in Quantum-dot Cellular Automata, University of Notre Dame, Notre Dame, 2000 (Ph.D. Thesis).
[33] G. Schulhof, K. Walus, G.A. Jullien, Simulation of random cell displacements in QCA, ACM J. Emerg. Technol. Comput. Syst. (JETC) 3 (216) (2007), http://dx.doi.org/10.1145/1229175.1229177.
[34] T. Teodosio, L. Sousa, QCA-LG: A Tool for the Automatic Layout Generation of QCA Combinational Circuits, Norchip, IEEE, Lisbon, 2007 15, http://dx.doi.org/10.1109/NORCHP.2007.4481078.
[35] S.R. Heikalabad, A.H. Navin, M. Hosseinzadeh, Midpoint Memory: A Special Memory Structure for Data-Oriented Models Implementation, Journal of Circuits, Systems and Computers 24 (5), 2015.