J Comput Electron
DOI 10.1007/s10825-014-0589-5

A symmetric quantum-dot cellular automata design for 5-input majority gate

Arman Roohi · Hossein Khademolhosseini · Samira Sayedsalehi · Keivan Navi

© Springer Science+Business Media New York 2014

Abstract By the inevitable scaling down of the feature size of the MOS transistors which are deeper in nanoranges, the CMOS technology has encountered many critical challenges and problems such as very high leakage currents, reduced gate control, high power density, increased circuit noise sensitivity and very high lithography costs. Quantum-dot cellular automata (QCA) owing to its high device density, extremely low power consumption and very high switching speed could be a feasible competitive alternative. In this paper, a novel 5-input majority gate, an important fundamental building block in QCA circuits, is designed in a symmetric form. In addition to the majority gate, a SR latch, a SR gate and an efficient one bit QCA full adder are implemented employing the new 5-input majority gate. In order to verify the functionality of the proposed designs, QCADesigner tool is used. The results demonstrate that the proposed SR latch and full adder perform equally well or in many cases better than previous circuits.

A. Roohi (✉) · S. Sayedsalehi · K. Navi
Nanotechnology and Quantum Computing Laboratory, Shahid Beheshti University, G. C., Tehran, Iran
e-mail: a.roohi@srbiau.ac.ir

H. Khademolhosseini
Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran

K. Navi
Department of Electrical and Computer Engineering, Shahid Beheshti University, G. C., Evin, Tehran, Iran

Published online: 18 June 2014

Keywords Quantum cellular automata (QCA) · Majority gate · SR latch · Full adder · Nanoelectronic circuit

1 Introduction

Due to defects of conventional CMOS technology and its physical limits, wide-range researches on nanoscale such as quantum cellular automata (QCA), tunneling phase logic (TPL), single electron tunneling (SET), and carbon nanotube (CNT) have been studied. QCA would be of more interest because of its capability to implement general computation as well as its attractive features including high speed operation, low power consumption and small dimension. A QCA cell consists of four dots and two identical electrons. Each dot can be occupied by one of the two hopping electrons in a way that the electrons stay diagonally opposite owing to Columbic interaction. In QCA technology binary information is encoded by formations of electrons rather than current employed in CMOS. Two fundamental building blocks for QCA are the inverter and the majority gate [1–3]. In implementation of many structures these gates are utilized as basic elements [4–11].

In this paper, we propose a new powerful 5-input majority gate and then in order to investigate the effectiveness of the proposed gate, a SR latch and a one bit QCA full adder using the new majority gate are implemented.

The rest of this paper is organized as follows. In Sect. 2, a review of the QCA and previous similar works is presented. The proposed approach and implementation of the symmetric 5-input majority gate as well as the SR latch and the QCA full adder are represented in Sect. 3. In Sect. 4, we demonstrate simulation results and comparisons and finally Sect. 5 concludes the paper.

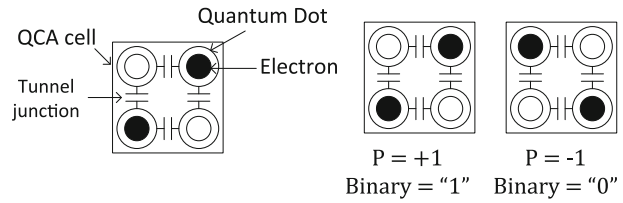

Fig. 1 QCA cell and two possible polarizations

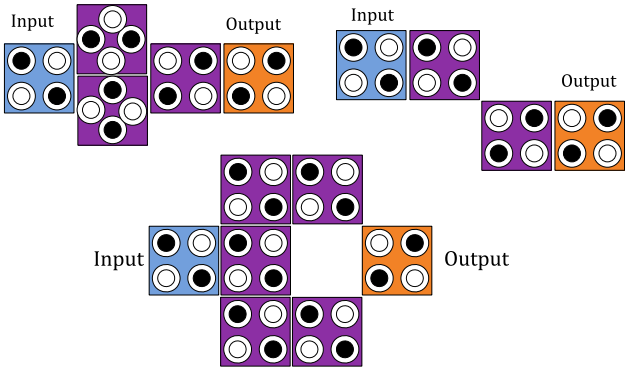

Fig. 2 Three types of inverter gate

2 Preliminaries

2.1 QCA gates review

The basic structure in QCA is a squared cell that has four dots positioned at its corners and two free electrons. Due to Coulombic interactions, two stable arrangements of electrons might occur, which are encoded to logic "0" and logic "1" [1,2,12], as shown in Fig. 1.

The basic gates in QCA design are majority gate and inverter gate by which various gates and circuits can be constructed. In Fig. 2 three formerly proposed types of inverter gate are shown. Although the last inverter consists of more cells in comparison with the other two ones, it is being employed more due to its proper functionality in different cases.

On account of the major role of majority gate in QCA, different majority gate designs have been suggested over the last years. Earlier designs used in important circuits such as full adders, were almost 3-input majority gates as shown in Fig. 3. These majority gates acts according to the following equation:

$$M(A, B, C) = AB + AB + BC \tag{1}$$

Recently some 5-input majority gates have been proposed. The 5-input majority gate functions as Eq. (2). In [13] which provides a three dimensional design for the 5-input majority gate, the five input cells affect on the middle cell and the output polarization is determined. Figure 4 shows this majority

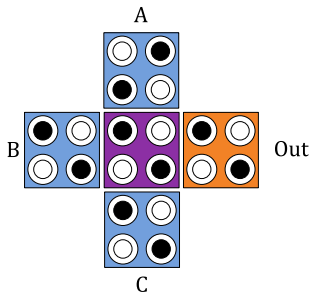

Fig. 3 A QCA 3-input majority gate

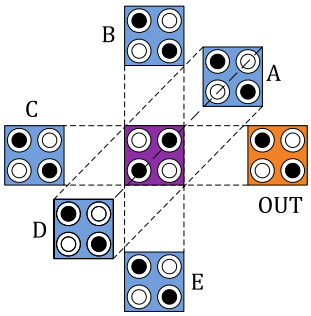

Fig. 4 Schematic symbol for a 5-input majority gate [13]

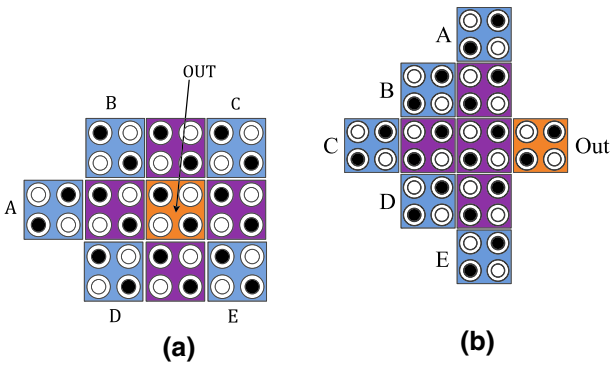

Fig. 5 Two layouts of effective 5-input majority gate [14,15]

gate. Although only seven cells are employed, it is hard to implement because the gate cells are located in three layers.

$$M(A, B, C, D, E) = \text{ABC} + \text{ABD} + \text{ABE} + \text{ACD} + \text{ACE} + \text{ADE} + \text{BCD} + \text{BCE} + \text{BDE} + \text{CDE} \tag{2}$$

In [14] as shown in Fig. 5a, the output cell is a middle cell and it is surrounded by the five input cells. In order to connect this gate to other gates a multilayer design is needed. In [15] the same number of cells as in the majority gate proposed in [14] is used; however, the output cell is not a middle cell. Figure 5b illustrates the majority gate proposed in [15].

Another design of 5-input majority gate suggested in [16] is depicted in Fig. 6.

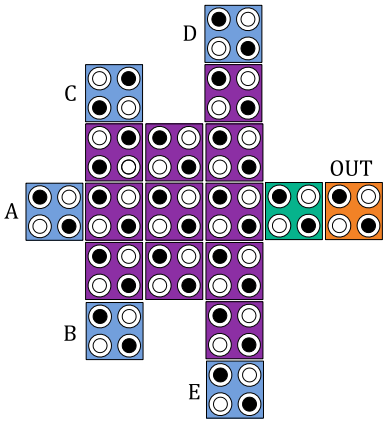

Fig. 6 A 5-input majority gate [16]

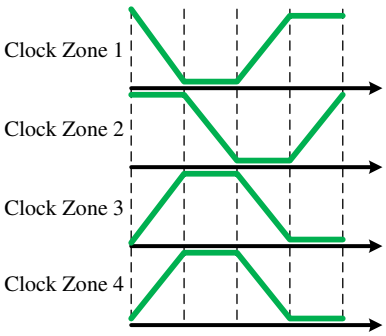

Fig. 7 Four-phased clocks of the QCA zones

2.2 QCA clocking

Clocking in QCA is different from clocking in CMOS. To synchronize and control each part of QCA circuitry properly, four clock signals are employed where each signal is shifted by 90° compared to the previous clock signal. Each clock signal has four phases, Switch, Hold, Release and Relaxed and each cell could be in one of the four phases in accordance to the clock signal applied. The four clock signals are shown in Fig. 7.

The clocking mechanism provides synchronization as well as signal energy restoration.

2.3 Kink energy

The polarization of a QCA cell is computed by all its neighbors placed in the energy-effective range. This state is determined by the Coulombic interaction between QCA cells, namely kink energy, which can be computed using the electrostatic interaction between all electrons in two cells, i and j, as

$$E^{i,j} = \frac{1}{4\prod \varepsilon_0 \varepsilon_r} \sum_{n=1}^{4} \sum_{m=1}^{4} \frac{q_n^i q_m^j}{\left| r_n^i - r_m^j \right|} \tag{3}$$

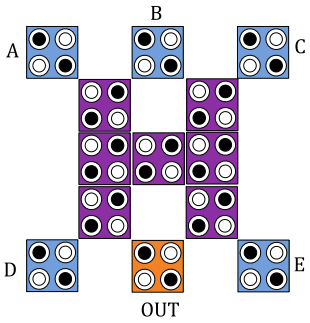

Fig. 8 Proposed symmetric 5-input majority gate

where ε_0 is the permittivity of free space, ε_r is the dielectric constant, q_{in} is the charge in dot n of cell i, r_{in} is the position of dot n in cell i and $|r_n - r_m|$ is the distance between cells. The kink energy between two cells is defined as the difference in energy between the state in which the cells have opposite polarizations and the one in which those same two cells have the same polarization:

$$E_{kink}^{n,m} = E_{p_n \neq p_m}^{n,m} - E_{p_n = p_m}^{n,m} \tag{4}$$

According to the recent equation the polarization state of each of the cells is computed using Eq. (5) [17,18],

$$P_i = \frac{\frac{E_{kink}^{i,j}}{2\gamma} \sum_j p_j}{\sqrt{1 + (\frac{E_{kink}^{i,j}}{2\gamma} \sum_j p_j)^2}} \tag{5}$$

where P_i is the polarization state of the cell, and P_j is the polarization state of the neighboring cells. γ is the tunneling energy of electrons within the cell. The tunneling barriers' heights are controlled by QCA clock [17–20].

3 Proposed approach

In this paper we consider simultaneously achievement of two criteria for our designs: improvement in reduction of cell number as well as symmetry which leads to fault tolerance feature.

3.1 Five input majority gate

Figure 8 illustrates the design of a novel symmetric 5-input majority gate. The gate is fault tolerant owing to its symmetric structure. The new 5-input majority gate is composed of 13 cells, five input cells, one output cell and seven device cells. Additionally all input cells have an inverting effect on polarizations of device cells. A 3-input OR gate and 3-input AND gate can be easily implemented by fixing two of the five input cells to +1 or −1, respectively. The new five-input

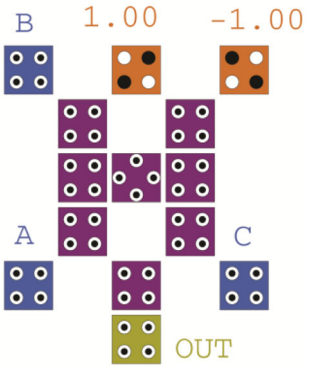

Fig. 9 Layout of Boolean function A+BC

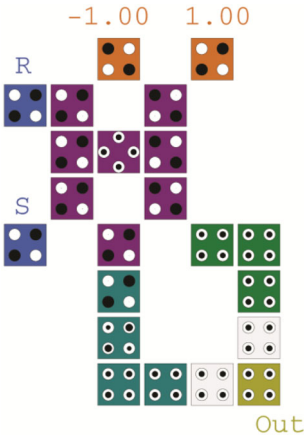

Fig. 10 Layout of the SR latch

Table 1 SR latch truth table

S	R	Q	$\overline{Q}$
0	0	Latch	
0	1	0	1
1	0	1	0
1	1	Latch	

majority gate proposed here, will be reconfigured in the following sections in order to construct various useful gates and circuits.

3.1.1 SR latch

Producing various outputs in the proposed 5-input majority gate, we are able to design some useful gates and circuits. For example, the arrangement illustrated in Fig. 9 which outputs A+BC, could be used to design a SR latch. In [21–23] some designs and utilizations of SR latch are discussed.

A SR latch is an asynchronous element which has no control signal and it functions only based on states of S and R. SR latch is usually implemented by means of NAND or NOR gates. Truth table of SR latch is as Table 1 (The state, in which both S and R are 1, is disallowed because in this state the gate would be metastable. This state is assumed a Latch state in our design.).

Figure 10 shows the SR latch designed based on the proposed 5-input majority gate. Although the input R is not applied inversely, since the output is inverted, the gate functions correctly according to its truth table.

Since any change in the inputs of SR latch leads to immediate change in its output, a control signal is required. Hence, in order to convert a SR latch to a SR gate, an enable signal or a clock signal should be added. Since in level triggered flip-flops, input changes are applied to the circuit immediately, we have modified the circuit in order to become an edge triggered flip-flop (Fig. 11). Table 2 shows the operation of the level to edge converter part of the proposed SR gate.

Employing the proposed SR latch, D latch, JK latch and other useful circuits including memory cells and ALU blocks could be constructed on basis of our proposed gate.

3.1.2 One bit QCA full adder

Full adder is a widely used circuit which in QCA is realized using majority gate. In earlier full adder designs, 3-input majority gates were employed [4,5] however recently 5-input ones have been used in order to reduce the number of cells as well as occupied area in designs [7,15]. An efficient one bit QCA full adder is presented and implemented based on the proposed 5-input majority gate. It is produced utilizing 58 cells and is implemented in three layers based on multilayer implementation method [24,25]. The possibility of multilayer QCA has been examined in a robust previous work [24]. The inputs are applied in the upper layer. It uses three clock phases to generate the carryout and the sum. In Fig. 12 the layout of the proposed full adder is shown.

3.2 Fault tolerance analysis

Fault tolerant designs are able to continue their functionality in the presence of some faults. To assess displacement and misalignment tolerance [7,26], a 3-input AND gate based on our proposed gate is designed and cells A, B and C are displaced and misaligned in it. Figure 13 shows the possible defects which may occur for cell A (The green cells depict the possible locations of a displaced or misaligned A.). The obtained results are summarized in Table 3.

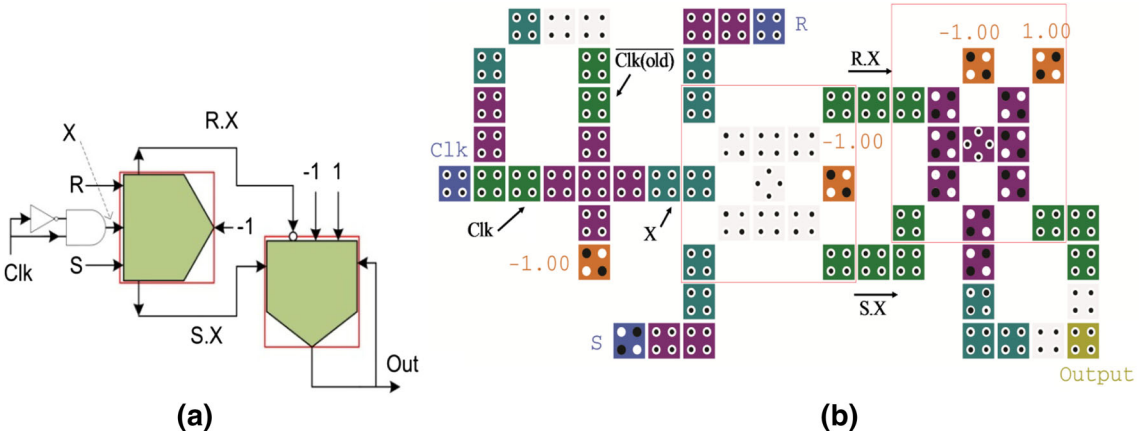

Fig. 11 Schematic and layout of the edge triggered QCA SR flip-flop

Table 2 Operation of the proposed rising edge triggered QCA SR flip-flop (Fig. 11)

Clk(old)	$\overline{\text{Clk(old)}}$	Clk	X = Maj (Clk, $\overline{\text{Clk(old)}}$, −1)
0	1	0	0 (not changed)
0	1	1	1 (input)
1	0	0	0 (not changed)
1	0	1	0 (not changed)

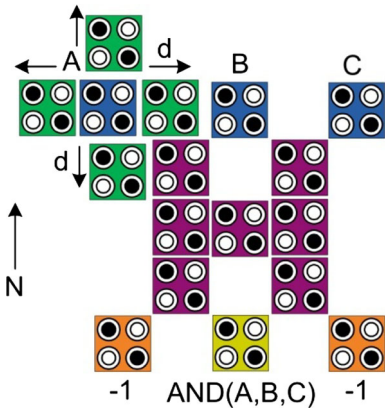

Fig. 13 Displacement and misalignment defects in the proposed 3-input AND gate

4 Results

4.1 Simulation results

The functionality verifications of the proposed gate and circuit are carried out using the QCADesigner bistable engine [27]. The following parameters are used for a bistable approximation: cell size = 18 nm, number of samples = 50,000, convergence tolerance = 0.0000100, radius of effect = 65.000000 nm, relative permittivity = 12.900000,

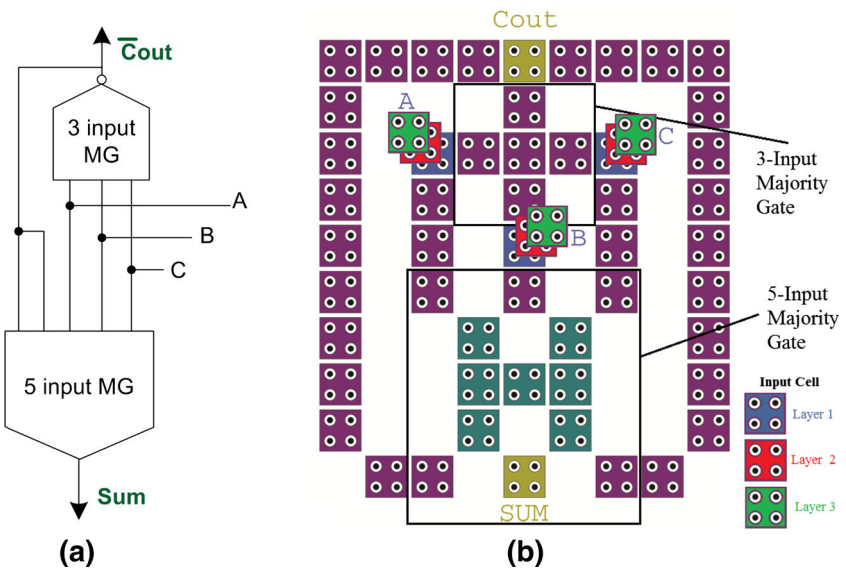

Fig. 12 Proposed QCA full adder, **a** schematic, and **b** layout

Table 3 Results of cell displacement and misalignment of cell A (C) and B, separately

Cell *C* behaves mirrorly similar to cell A in all directions			
Move *A* to West $0 \leq d \leq 5$	Move *A* to East $0 \leq d \leq 11$	Move *A* to North $0 \leq d \leq 5$	Move *A* to South $0 \leq d \leq 12$
Normal function	Normal function	Normal function	Normal function
Cell *B*			
Move *B* to West $0 \leq d \leq 11$	Move *B* to East $0 \leq d \leq 11$	Move *B* to North $0 \leq d \leq 14$	Move *B* to South $0 \leq d \leq 11$
Normal function	Normal function	Normal function	Normal function

clock high = 9.800000e-022 J, clock low = 3.800000e-023 J, clock shift = 0, Clock amplitude factor = 2.000000, layer separation = 11.500000, maximum iterations per sample = 100. Most of the mentioned parameters are default values in QCADesigner. For a clear view, simulation results of the function A + B.C, SR latch and SR gate are shown in Fig. 14. Figure 15 depicts simulation results of the 5-input majority gate, the one-bit full adder and 3-input AND gate constructed using the proposed gate.

4.2 Comparison results

The proposed SR latch and one bit QCA full adder are compared with the previously proposed ones and the results are illustrated in Tables 4 and 5, respectively. It can clearly be perceived that our circuits resulted in significant improvements in terms of cell count and area.

5 Conclusion

This paper presented a novel and expandable design of 5-input majority gate. The proposed majority gate can be

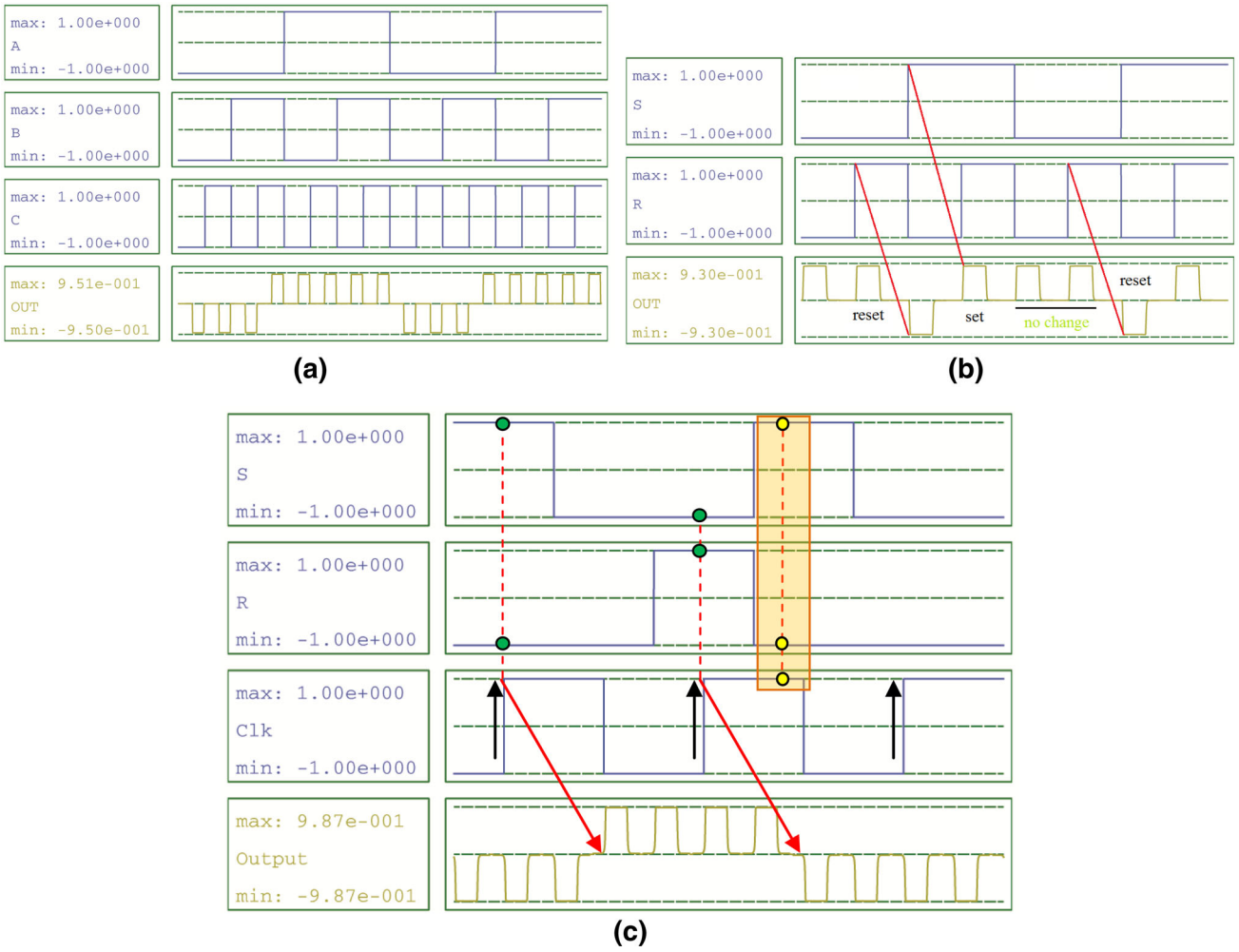

Fig. 14 Simulation results of **a** function A + BC, **b** proposed SR latch, and **c** proposed edge triggered SR flip flop (In the filled region, SR=10 and Clk=1, but the output is 0.)

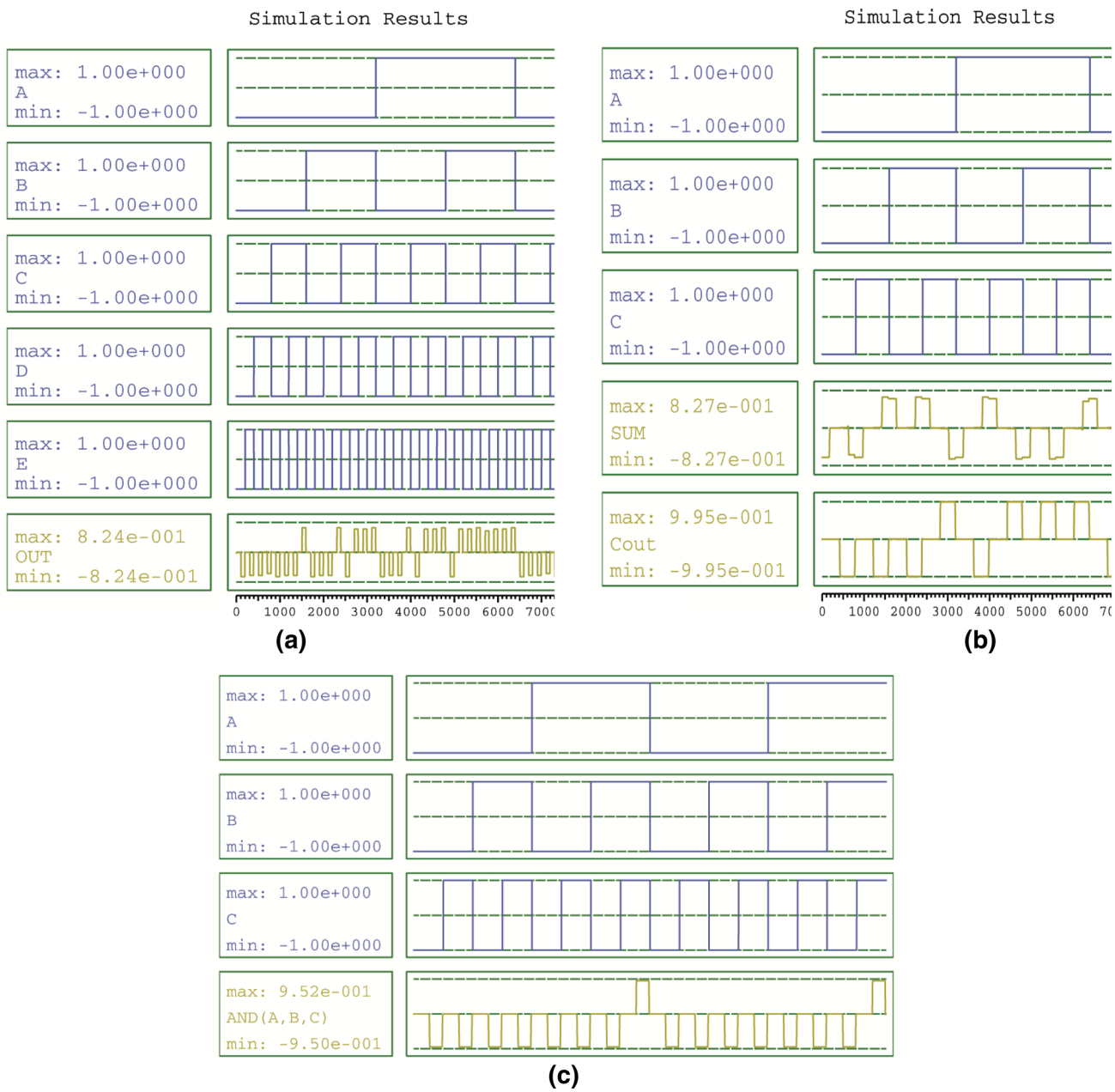

Fig. 15 Simulation result of **a** 5-input majority gate, **b** proposed one bit full adder, and **c** 3-input AND

Table 4 Comparison of QCA SR latch designs

	Area (μm^2)	Cell count	Delay
Previous design [22]	~200	67	6 clock phases
Proposed design (Fig. 11)	0.04	22	4 clock phases

Table 5 Comparison of QCA full adder designs

	Area (μm^2)	Cell count	Delay
Previous design [6]	0.17	145	5 clock phases
Previous design [5]	0.10	86	3 clock phases
Previous design [15]	0.04	73	3 clock phases
Proposed design (Fig. 13)	0.04	52	3 clock phases

used to construct more sophisticated QCA structures. Taking the advantages of the proposed majority gate, a SR latch, a SR gate (edge triggered) and an efficient one-bit QCA full adder were implemented. As it was apparent in results, the proposed full adder has some superiority over the previous designs and shows considerable improvements.

References

1. Lent, C.S., Tougaw, P.D., Porod, W., Bernstein, G.H.: Quantum cellular automata. Nanotechnology **4**, 49–57 (1993). doi:10.1088/0957-4484/4/1/004
2. Porod, W.: Quantum-dot devices and quantum-dot cellular automata. Int. J. Bifurcation Chaos **7**, 2199–2218 (1997). doi:10.1016/S0016-0032(97)00041-0
3. Lent, C.S., Tougaw, P.D.: A device architecture for computing with quantum dots. Proc. IEEE **85**, 541–557 (1997). doi:10.1109/5.573740
4. Tougaw, P.D., Lent, C.S.: Logical devices implemented using quantum cellular automata. J. Appl. Phys. **75**, 1818–1825 (1994). doi:10.1063/1.356375
5. Cho, H., Swartzlander, EarlE: Adder and multiplier design in quantum-dot cellular automata. Comput. IEEE Trans. **58**, 721–727 (2009). doi:10.1109/TC.2009.21
6. Zhang, R., Walnut, K., Wang, W., Jullien, G.: A method of majority logic reduction for quantum cellular automata. IEEE Trans. Nanotechnol. **3**, 443–450 (2004). doi:10.1109/TNANO.2004.834177
7. Roohi, A., Sayedsalehi, S., Khademolhosseini, H., Navi, K.: Design and evaluation of a reconfigurable fault tolerant quantum-dot cellular automata gate. J. Comput. Theor. Nanosci. **10**, 380–388 (2013). doi:10.1166/jctn.2013.2708
8. Kamrani, M., Khademolhosseini, H., Roohi, A., and Aloustanimirmahalleh, P.: A novel genetic algorithm based method for efficient QCA circuit design. In: Advances in Computer Science, Engineering & Applications, pp. 433–442. Springer, Berlin (2012) doi:10.1007/978-3-642-30157-5_43
9. Roohi, A., Khademolhosseini, H., Sayedsalehi, S., Navi, K.: Implementation of reversible logic design in nanoelectronics on basis of majority gates. In: Computer Architecture and Digital Systems (CADS), 16th CSI International Symposium on, IEEE, 2012. doi:10.1109/CADS.2012.6316410
10. Roohi, A., Menbari, B., Shahbazi, E., Kamrani, M.: A genetic algorithm based logic optimization for majority gate-based QCA circuits in nanoelectronics. Quantum Matter **2**, 219–224 (2013). doi:10.1166/qm.2013.1050
11. Sabbaghi-Nadooshan, R., Kianpour, M.: A novel QCA implementation of MUX-based universal shift register. J. Comput. Electron. **13**, 198–210 (2013). doi:10.1007/s10825-013-0500-9
12. Lu, Y., Lent, C.S.: Theoretical study of molecular quantum-dot cellular automata. J. Comput. Electron. **4**, 115–118 (2005). doi:10.1007/s10825-005-7120-y
13. Rahimi Azghadi, M., Kavei, O., Navi, K.: A novel design for quantum-dot cellular automata cells and full adder. J. Appl. Sci. **7**, 3460–3468 (2007)
14. Navi, K., Sayedsalehi, S., Farazkish, R., Rahimi Azghadi, M.: Five-input majority gate, a new device for quantum-dot cellular automata. J. Comput. Theor. Nanosci. **7**, 1546–1553 (2010). doi:10.1166/jctn.2010.1517
15. Navi, K., Farazkish, R., Sayedsalehi, S., Rahimi Azghadi, M.: A new quantum-dot cellular automata full-adder. Microelectron. J. **41**, 820–826 (2010). doi:10.1016/j.mejo.2010.07.003
16. Akeela, R., Wagh, M.D.: A five-input majority gate in quantum-dot cellular automata. In: NSTI Nanotech, vol. 2, pp. 978–981. (2011)
17. Toth, G.: Correlation and coherence in quantum-dot cellular automata. Ph.D. Thesis, University of Notre Dame, Notre Dame (2000)
18. Schulhof, G., Walus, K., Jullien, G.A.: Simulation of random cell displacements in QCA. ACM J. Emerg. Technol. Comput. Syst. (JETC) **3**, 2–16 (2007). doi:10.1145/1229175.1229177
19. Teodosio, T., Sousa, L.: QCA-LG: A Tool for the Automatic Layout Generation of QCA Combinational Circuits, pp. 1–5. Norchip, IEEE, Lisbon (2007). doi:10.1109/NORCHP.2007.4481078
20. Walus, K., Dysart, T.J., Jullien, G.A., Budiman, R.A.: QCADesigner: a rapid design and Simulation tool for quantum-dot cellular automata. Nanotechnol. IEEE Trans. **3**, 26–31 (2004). doi:10.1109/TNANO.2003.820815
21. Thapliyal, H., Ranganathan, N.: Reversible logic-based concurrently testable latches for molecular QCA. Nanotechnol. IEEE Trans. **9**, 62–69 (2010). doi:10.1109/TNANO.2009.2025038
22. Huang, J., Momenzadeh, M., Lombardi, F.: Design of sequential circuits by quantum-dot cellular automata. Microelectron. J. **38**, 525–537 (2007). doi:10.1016/j.mejo.2007.03.013
23. Dehkordi, M.A., Shamsabadi, A.S., Ghahfarokhi, B.S., Vafaei, A.: Novel RAM cell designs based on inherent capabilities of quantum-dot cellular automata. Microelectron. J. **42**, 701–708 (2011). doi:10.1016/j.mejo.2011.02.006
24. Gin, A., Tougaw, P.D., Williams, S.: An alternative geometry for quantum-dot cellular automata. J. Appl. Phys. **85**, 8281–8286 (1999). doi:10.1063/1.370670
25. Roohi, A., Khademolhosseini, H.: Quantum-dot cellular automata: computing in nanoscale. Rev. Theor. Sci. **2**, 46–76 (2014). doi:10.1166/rits.2014.1014
26. Momenzadeh, M., Jing, H., Tahoori, M.B., Lombardi, F.: Characterization, test, and logic synthesis of and-or-inverter (AOI) gate design for QCA implementation. Comput. Aided Des. Integr. Circuits Syst. IEEE Trans. **24**, 1881–1893 (2005). doi:10.1109/TCAD.2005.852667
27. QCADesigner Home Page. www.atips.ca/projects/qcadesigner