International Journal of Wireless and Mobile Communication for Industrial Systems
Vol. 2, No. 1 (2015), pp. 7-14
http://dx.doi.org/10.21742/ijwmcis.2015.2.1.02

A novel design of QCA based RAM cell

Trailokya Nath Sasamal[1*], Ashutosh Kumar Singh[2] and Anand Mohan[1]

[1] *Department of Electronics & Communication, NIT Kurukshetra, Kurukshetra, India*
[2]*Department of Computer Application, NIT Kurukshetra, Kurukshetra, India*

Abstract

Quantum-dot cellular automata (QCA) shows a new paradigm at nanoscale circuit design with high performance and low power consumption features, which possibly can substitute traditional CMOS technology. This work presents a rotated structure of conventional 3-input majority gate in QCA, which exhibits a symmetric structure that is suitable for a compact implementation of coplanar QCA digital circuits. To show the novelty of this structure, D flip flops and memory cell are proposed. The result shows that the proposed D flip flops are more superior over the existing designs. In addition, proposed memory cell is 33%, 79% and 20% more efficient in terms of cell counts, area and latency respectively, over the best design in this segment using conventional 3-input majority gate. Designs are realized and evaluated using QCADesigner 2.0.3.

Keywords: *Quantum-dot cellular automata (QCA). Memory cell. Majority gate. Digital design.*

1. Introduction

In traditional CMOS based VLSI technology, as size of the devices are shrinking, devices are expose to circuit noise and yield high leakage current[1]. Several nanoscale devices have been gained popularity in research community during recent years. These include technologies like quantum-dot cellular automata (QCA), tunneling phase logic (TPL), single electron tunneling (SET), and carbon nanotube (CNT). In this aspect, QCA could be a feasible competitive alternative, which promises extremely low power consumption with small dimension and high speed operation [2, 3]. In QCA, a cell binds two free electron and the logic values '0', '1' depends on position of electrons inside the quantum-dot cell, which are driven by Coulombic interaction. The binary information is transferred as a result of propagation of polarization between two cells due to the Coulombic interaction of electrons. In other way, there is no flow of current as in conventional CMOS. Hence, power dissipation due to change in logic and propagation does not add up to the total power dissipation [4].

Different QCA based circuits design and structures are discussed previously [516]. QCA based memory cell has been studied in [17-20]. In most of the work RAM cell are loop-based as it needs lesser clock zones. However, the designs are not well optimized. This work presents a modified majority gate and its applicability in low complexity coplanar memory cell with set/reset capability using the majority gate structure, which is superior in terms of cell count, area occupation and delay over the prior designs. Rest of the paper is organized as follows: Section 2 gives a review of QCA logic. In section 3, a 2:1 multiplexer and a memory cell are implemented using rotated 3-input majority gate. Simulated results of proposed designs and comparison to previous work are presented in section 4 and concluded in Section 6.

ISSN: 2205-8443 IJWMCIS

2. QCA preliminaries

In QCA a single cell is considered to construct each and every element (Computational and wires) of a circuit. Each cell consists of four quantum-dots at the corners and two of them contain free electrons. These electrons can quantum-mechanically tunnel between the four dots. Potential barriers of tunneling junctions are controlled by local electric fields. This field, siege electron movement or permits electron movement by simply raising or lowering potential barriers respectively. An isolated cell can settle in one of the three different states. Barrier lowering gives rise to a null state, where electrons are free to place at any dots. Remaining two states occur when barriers are raised. The cells in these states maintain a minimum energy. They are represented as P= +1 (logic 1) and P= -1 (logic 0) due to Coulombic interaction between electrons in a quantum cell [21], as shown in Fig. 1 (a).

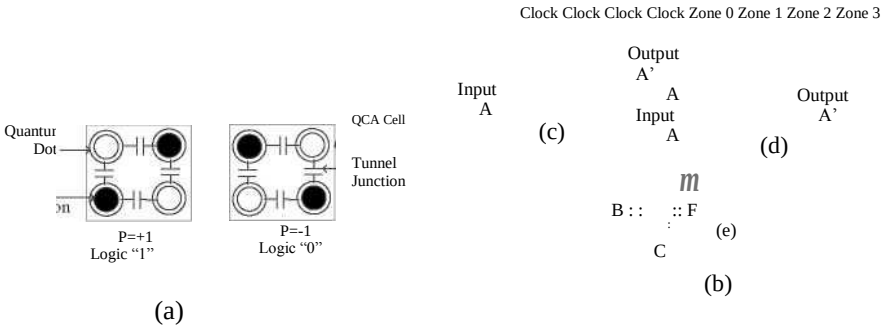


Figure 1. QCA (a) Two different polarization of Quantum-dot cell (b) QCA wire (c), (d) Two different realization of inverter (e) 3-input Majority gate

An inverter and majority voter (MV) gate are the fundamental gates that are used to construct any QCA gates and circuits. Wiring between two logic blocks is done by the cascade of Quantum cells, as shown in Fig.1 (b). Fig. 1 (c), (d) depict two different implementations of an inverter [22]. All QCA circuits needs proper clocking to control the flow of information, which also provides necessary power to drive the circuit.

To drive the input to the desired output, signals need to be passed through four clock zones. Clock signals for each zone are distinct and 90^0 phase shifted [23]. This clock zone provides the necessary electric field, which changes the potential barriers. So, clock zones enable the computation in sequential manner, i.e. when computation is going on in one zone, the previous zone must hold its outputs.

3. Proposed structures

3.1. Proposed 2:1 Multiplexer

A compact 2:1 multiplexer schematic is presented in Fig. 2 (a). Proposed multiplexer requires 3 MV, and 1 inverter in QCA implementation. This structure comprises only 18 quantum cells. In this structure, MV's in first level implements two AND gates that are driven by first clocking zone. The outputs of these MV's are fed to second level MV which is positioned in the second clocking zone. Select line 'select' is used to select one of the inputs, which also driven by first clock zone. QCA implementation of 2:1 multiplexer using majority gate is shown in Fig. 2 (b) that provides a valid output after two clock phases. It comprises only 18 cells that spread over an area of 0.02 pm2, which has outperformed previous works.

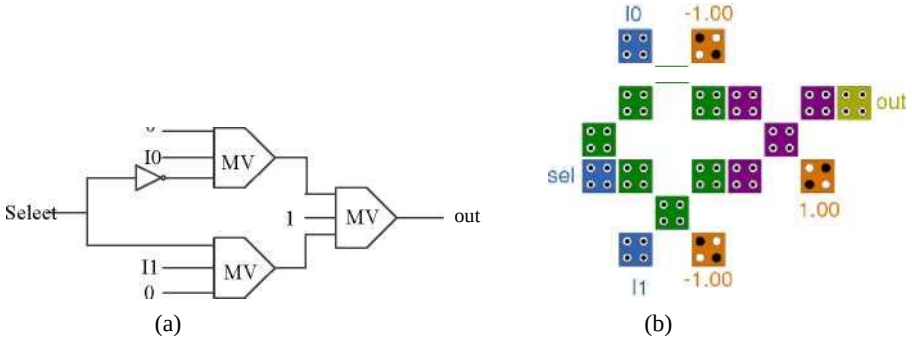


Figure 2. 2:1 multiplexer (a) Schematic (b) QCA layout

3.2. Memory cell

RAM cell is one of the essential components in many digital systems. Its performance is varied upon the complexity and input to output latency in QCA implementation. So optimization can be done in the selection of majority gates and proper clocking zone. In this work an efficient RAM cell is presented, as shown in Fig. 3, with set and reset ability. QCA layout of the proposed RAM cell is demonstrated in Fig. 4. It builds upon six majority gates (3 majority gates for each 2:1 mux). Signal *'Sel* is used as select line for the mux1 and signal *R/W* (Read/Write) is used as select line for mux2,as shown in Fig. 3. Mux2 operates on output of Mux1 and the output signal *'out'* of the memory cell. A clear view of the RAM cell operation is defined in Table 1.

Table 1. Operation of QCA based memory cell with set/reset ability.

Read/Write(R/W)	Select(Sel)	Set/Reset	Out(t) (Output)
1	1	X	Input
1	0	0	0(reset)
1	0	1	1(set)
0	X	X	Out(t-1)

For example, when *R/W='0'* the output of the circuit remains unchanged, i.e. *out*(t)=*out*(t-1). Output of the circuit sees the effect of input and set/reset signals by setting R/W='1'. Further, setting R/W='1' and *sel='Y* allow an input signal to be transmitted to the output. Similarly for select line *(sel)* ='0' the output of the circuit get changed according to set/reset signal. Output cell is driven by clock zone 0 and a valid output can be achieved after 5 clock phases.

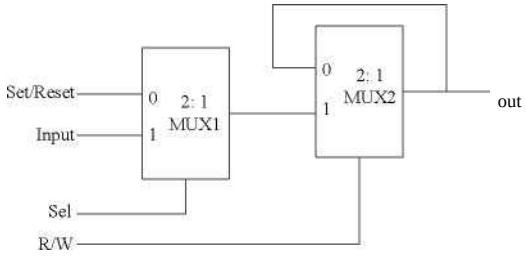


Figure 3. Schematic of compact memory cell with set/reset signal

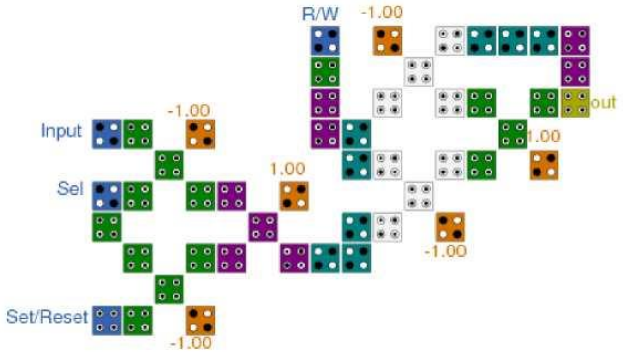


Figure 4. QCA layout of compact memory cell with set/reset signal

4. Results and Discussions

All the proposed circuits are simulated using the simulator QCA Designer-2.0.3 [24]. Simulation engine is set to coherence vector type in QCADesigner tool using the parameters as shown in Table 2.

Table 2. QCADesigner parameters for Coherence vector engine

Parameter	Value
Cell size	18 *18 nm^2
Relaxation time	1.000000e-015s
Time step	1.000000e-016s
Radius of effect	80 nm
Relative permittivity	12.9
Clock high	9.8e-22J
Clock low	3.8e-23J
Clock amplitude factor	2.000
Layer separation	11.5000 nm
Clock shift	0.000000e+000
Time step	1.000000e-016s
Total simulation time	7.000000e-011s

The input and output waveforms of 2:1 multiplexer are depicted in Fig. 5 (a). When select= '1' output follows input I_0 else follows I_1, after two clock phase delay. For better readability we have included only the clock zone 1 at which a valid output is expected. The comparison of 2:1 multiplexer with existing designs is shown in Table 3, by taking area, complexity and area-to-delay product (ADP). It is easily inferred from Table 3 that presented 2:1 multiplexer achieves a minimum ADP with reduced complexity.

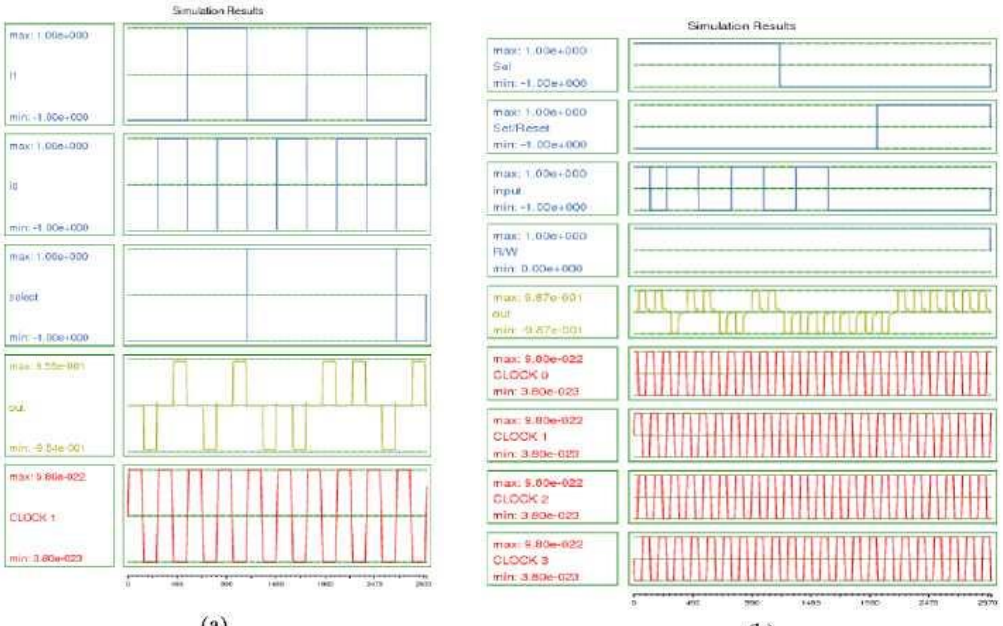
Table 3. Comparison of proposed 2:1 multiplexer with existing designs

2:1 Multiplexer	Area(gm^2)	Cell count	Delay	Clock Phases	ADP	Crossover $^{t}yp^{e}$
[10]	0.14	88	1	4	0.14	Co-planar
[11]	0.14	66	1	4	0.14	Co-planar
[12]	0.08	46	1	4	0.08	Multilayer

[13]	0.06	36	1	4	0.06	Multilayer
[14]	0.07	56	1	4	0.07	Co-planar
[15]	0.03	27	0.75	3	0.022	Co-planar
[16]	0.02	26	0.5	2	0.01	Co-planar
Proposed	0.02	18	0.5	2	0.01	Co-planar

Table 4. Comparison of proposed QCA RAM cell structure

QCA Memory Cell	Coplanar Crossover	Set/ Reset Ability	Area (pm^2)	Cell Count	Delay	Clock Phases	ADP	Majority Gate Types
[19]	yes	no	0.16	158	2	8	0.32	TMG*
[18]	yes	no	0.11	100	3	12	0.33	TMG*
	no	no	0.07	63	2	8	0.14	
[17]	no	yes	0.13	109	1.75	7	0.2275	TMG*
[20]	no	yes	0.08	88	1.5	6	0.12	TMG*, 5-Input Majority Gate
Proposed	no	yes	0.06	49	1.25	5	0.075	RMG#



*TMG: Traditional 3-Input Majority Gate
#RMG: Rotated Majority Gate

Figure 5. (a) Input and Output waveforms of 2:1 multiplexer (b) Input/Output waveforms of Memory cell with Set/Reset ability

In addition, Fig. 5(b) shows input and output waveforms of efficient RAM cell with *set/reset* ability. During normal mode, input data is propagated to the output after 1.25 clock cycles by activating both select and read/write line to '+1'. Similarly, by fixing *set/reset* line to '0' or '1' output line can be set or reset respectively after a delay of 1.25 clock cycles. So Fig. 5(b) confirms that the presented RAM cell provides expected outputs after first falling edge of clock 0.

It is worth noticing that the proposed Memory cell is fastest among all the existing structures. From Table 4, it is clearly perceived that the proposed memory cell with *set/reset* ability can be a suitable candidate for further complexity and latency analysis in future as a benchmark structure. This structure has outperformed all designs [17, 18, 19, 20] in terms of cell count, input to output delay and area occupation.

5. Conclusion

In this paper a modified 3-input majority gate structure was addressed. As memory cell is rudimental for most of the digital circuits, having a high speed and less complex memory cell is significantly important. To showcase the efficacy of the rotated structure, a 2:1 multiplexer and a new memory cell were introduced. All the designs inculcate coplanar non-crossover wires with enhanced QCA layout. Simulations using QCADesigner confirm that the presented designs using modified structure have outperformed all prior designs and shows significant improvements.

References

[1] R. Compano, L. Molenkamp, D.J. Paul, "Roadmap for Nanoelectronics", **(2001)**.

[2] A.O. Orlov, I. Amlani, G.H. Bernstein, C.S. Lent, G.L. Snider, "Realization of a Functional Cell for Quantum-Dot Cellular Automata", Science, vol. 277, pp. 928-930, **(1997)**.

[3] P.D. Tougaw, and C.S. Lent, "Logical devices implemented using quantum cellular automata", Applied Physics, vol. 75, pp. 1818-1824, **(1994)**.

[4] C.S. Lent, P.D. Tougaw, W. Porod and G.H. Bernstein, "Quantum cellular automata", Nanotechnology, vol. 4, pp. 49-57, **(1993)**.

[5] K. Navi, R. Farazkish, S. Sayedsalehi and M.R. Azghadi, "A new quantum-dot cellular automata full-adder", Microelectronics Journal, vol. 41, pp. 820-826, **(2010)**.

[6] S. Hashemi, M. Tehrani and K. Navi, "An efficient quantum-dot cellular automata full-adder", Scientific Research and Essays, vol. 7, pp. 177-189, **(2012)**.

[7] R.S. Nadooshan and M. Kianpour, "A novel QCA implementation of MUX-based universal shift register", Journal of Computational Electronics vol. 13, pp. 198-210, **(2014)**.

[8] A. Roohi, H. Khademolhosseini, S. Sayedsalehi and K. Navi, "A symmetric quantum-dot cellular automata design for 5-input majority gate", Journal of Computational Electronics, vol. 13, pp. 701-708, **(2014)**.

[9] T.N. Sasamal, A.K. Singh, A. Mohan, "Efficient design of reversible alu in quantum-dot cellular automata", Optik, vol. 127, pp. 6172-6182, **(2016)**.

[10] K. Kim, K. Wu, R. Karri, "The robust QCA adder designs using composable QCA building blocks", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, vol. 26, pp. 76-183, **(2007)**.

[11] V. Mardiri, C. Mizas, L. Fragidis and V. Chatzis, "Design and simulation of a QCA 2 to 1 multiplexer", In: The 12th WSEAS International Conference on COMPUTERS, Heraklion, Greece, pp. 511-516, **(2008)**.

[12] T. Teodsio and L. Sousa, "QCA-LG: A tool for the automatic layout generation of QCA com-

binational circuits", In: The 25th IEEE Norchip Conference, Aalborg, pp. 1-5, **(2007)**.

[13] S. Hashem, M. Azghadi and A.Z. Hosseini, "A novel QCA multiplexer design", In: International Symposium on Telecommunications, pp. 692-696, **(2008)**.

[14] V.A. Mardiris and I.G. Karafyllidis, "Design and simulation of modular 2n to 1 quantum-dot cellular automata (QCA) multiplexers", International Journal of Circuit Theory and Applications, vol. 38, pp. 771-785, **(2010)**.

[15] A. Roohi, H. Khademolhosseini, S. Sayedsalehi and K. Navi, "A novel architecture for quantum-dot cellular automata multiplexer", International Journal Computer Science Issues, vol. 8, pp. 55-60, **(2011)**.

[16] R.S. Nadooshan and M. Kianpour, "A novel QCA implementation of MUX-based universal shift register", Journal of Computational Electronics, vol. 13, pp. 198-210, **(2014)**.

[17] S. Hashemi and K. Navi, "New robust QCA D flip flop and memory structures", Microelectronics Journal, vol. 43, pp. 929-940, **(2012)**.

[18] M.A. Dehkordi, A.S. Shamsabadi, B.S. Ghahfarokhi and A. Vafaei, "Novel RAM Cell designs based on inherent capabilities of quantum-dot cellular automata", Microelectronics Journal, vol. 42, pp. 701-708, **(2011)**.

[19] K. Walus, A. Vetteth, G.A. Jullien and V.S. Dimitrov, "RAM design using quantum- dot cellular automata", In: Technical Proceedings of the Nanotechnology Conference and Trade Show, vol. 2, pp. 160-163, **(2003)**.

[20] S. Angizi, S. Sarmadi, S. Sayedsalehi and K. Navi, "Design and evaluation of new majority gate-based RAM cell in quantum-dot cellular automata", Microelectronics Journal, vol. 46, pp. 43-51, **(2015)**.

[21] P.D. Tougaw and C.S. Lent, "Logical devices implemented using quantum cellular automata", Journal of Applied Physics, vol. 75, pp. 1818-1825, **(1994)**.

[22] C.S. Lent and P.D. Tougaw, "A device architecture for computing with quantum dots", In Proceedings of the IEEE, vol. 85, pp. 541-557, **(1997)**.

[23] G. Toth and C.S. Lent, "Quasi adiabatic switching for metal-island quantum-dot cellular automata", Journal of Applied Physics, vol. 85, pp. 2977-2984, **(1999)**.

[24] K. Walus, T.J. Dysart, G.A. Jullien and R.A. Budiman, "QCA designer: a rapid design and simulation tool for quantum-dot cellular automata", IEEE Transactions on Nanotechnology, vol. 3, pp. 26-31, **(2004)**.

