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A comparative analysis and design of quantum-dot cellular automata memory cell architecture

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SUMMARY

Quantum-dot cellular automata (QCA) nanotechnology is considered as the best candidate for memory system owing to its dense packages and low power consumption. This paper analyzes the drawbacks of the previous QCA memory architectures and improves memory cell that exploits regular clock zone layout by employing two new clocking signals and a compact Read/Write circuit. The proposed layout is verified with the modified QCADesigner simulator and is analyzed by considering the noise effect. This design, occupying only a fraction of the area compared with the previous memory design, has superior performance. It is shown that the clock circuitry is very regular, helping manufacturability for physical implementation. Comparisons show that Read/Write latency of the proposed design is mitigated, the overall cell number, control cell and layout area are reduced (100%), and its performance against random charge noise is presented to be better. Copyright © 2010 John Wiley & Sons, Ltd.

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KEY WORDS: quantum-dot cellular automata; clock zones; memory cell; clock circuitry

1. INTRODUCTION

Quantum-dot cellular automata (QCA) is an emerging computing paradigm at the nanotechnology level [1, 2]. Unlike conventional CMOS technology using current to transfer binary information, QCA uses the positions of electrons in quantum dots to represent binary values 0 and 1 or store and transport information, whereas the positions of electrons are determined by Coulombic interaction. Some recent works show that the advantages of using QCA technology are smaller circuit size, faster switching speed [3], and less power consumption.

Originally proposed by Lent CS *et al.*, the QCA device had been initially demonstrated experimentally using metal-dot material [4] for this technology, although one major drawback existing in this fabrication is the need for cryogenic operation. Thus, a QCA device made from other materials and technology could be favored when focusing on room temperature operation [5–9], such as magnetic QCA and molecular QCA have been developed for its implementation. The recent work by Haider *et al.* has the reported room temperature operation of an atomic scale QCA cell using coupled Si dangling bonds [9], which provides an encouraging device fabrication scheme. In the meantime, other works in the QCA research area focus on logic and arithmetic designs and several QCA circuit architectures have been introduced [10–14]. Moreover, the literature [15] describes the modular design of multiplexer in terms of QCA unique design method. In fact, a digital system

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that is well suited to this emerging technology is the QCA implementation of large memories. However, memory designs in QCA present unique characteristics due to their clocking structures.

Much attention has been focused on the memory cell core (such as loop-based core [16], line-based core [17–19]) in the QCA devices and the results so far have been encouraging, but more work is needed on the simple architecture of the clock circuitry and peripheral circuit. The objective of this paper is the practical memory cell design of compact memory in QCA. The architectural design is based on two new clocking signal schemes to obtain more regular clock circuitry and compact construction, so that the memory cell helps to facilitate the fabrication if the QCA circuit soon becomes practical. Moreover, regular clock zones approve to construct larger word length memory architecture easily. The comparisons are performed based on different memory cell circuits; it is shown that the read/write latency of the proposed design is mitigated, the overall cell number and the layout area are reduced (100%). More analysis shows that it demonstrates a better performance against random charge noise.

The remainder of this work is organized as follows: In Section 2, some preliminaries about QCA memory design, such as device, crossover interconnects and Landauer-type clocking are presented. In Section 3, QCA clock circuitry and drawbacks of previous memory cell designs are analyzed. Section 4 shows the architecture design of the new memory cell. Section 5 presents analyses of simulation results and comparisons. Conclusions are drawn in the last Section.

2. PRELIMINARIES

2.1. QCA cells and interconnects

A QCA cell consists of four quantum dots and two excess electrons, whereas quantum dots are coupled by tunnel barriers in a square array (see Figure 1(a)). There are two possible ground state configurations for each cell corresponding to the two possible diagonal occupancies, these two states represent logic state 0 and 1, respectively. The QCA wire is formed by a beeline arrangement of QCA cells shown in Figure 1(b). The common inverter is built by arranging cells diagonally shown in Figure 1(c). The majority gate is implemented by five QCA cells arranged in the shape of a cross as shown in Figure 1(d), which is equivalent to a logic function $F\ (A, B, C) = AB + AC + BC$. One of its inputs can be used as a control input to make its function as a two-input AND or OR gate.

In QCA technology, there exist two special structures that are used to implement interconnects. One is coplanar wire crossing, the other is multi-layer crossing [10], both of which are shown in Figure 2. Coplanar wire crossing can be implemented with unrotated (90-degree wire) and rotated cells (45-degree wire). With this interconnect, it is possible to implement all the logic on a single QCA layer, there is no counterpart in silicon transistor technologies. Multi-layer crossing is constructed by adding more layers, but it is difficult for physical implementation [20]. Owing to this, the design presented in this study uses only coplanar wire crossing.

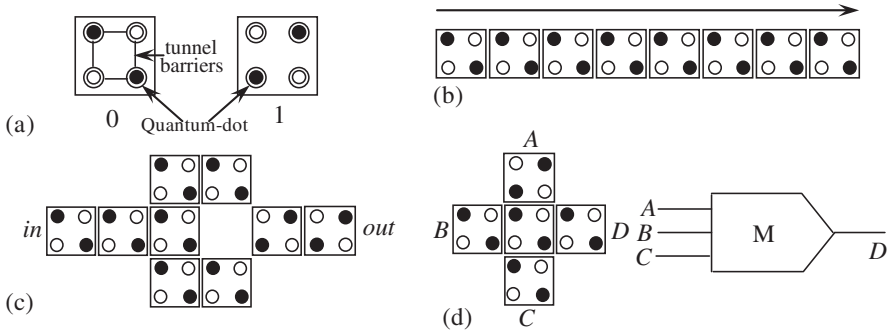

Figure 1. Basic QCA logic devices: (a) cell; (b) wire; (c) inverter; and (d) majority gate.

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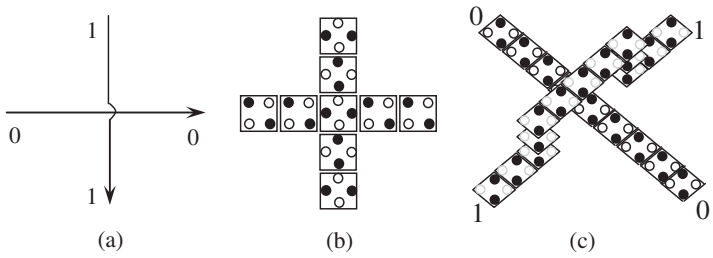

Figure 2. QCA wires crossings: (a) schematic diagram; (b) coplanar wire crossing; and (c) multi-layer crossing.

2.2. *QCA Landauer-type clocking*

The signal flow in an array of QCA cells is controlled by clocking signals, namely *Landauer-type clocking*. Clocking, supporting the synchronization of zone cells, plays an important role in the QCA circuits. Most previous QCA circuits are organized into four clock zones serially (clock 0, 1, 2, 3). An active clocking induces an electric field, polarizing the cell, latching their input values and starts driving other cells [1], which is widely used both for controlling information flow and designing sequential circuits. The cell numbers of one clock zone are not determined completely, but thermal fluctuations may set an upper limit. On molecular QCA, a single majority gate would function correctly in one clock zone and a wire of 50 cells would still operate correctly at room temperature [21]. The waveforms of the usual *Landauer-type clocking* are highly effective, implying that clocking relies on adiabatic switching principles to limit the dissipation of changing the state of a cell and operates in a serial fashion. Generally speaking, all types of clocking signals have four phases, namely: switch, hold, release and relax [1, 22]. During the switch phase, the tunnel barrier is gradually raised and a QCA cell polarizes to the neighbored input cell states. During the hold phase, the interdot tunnel barrier is held high to suppress electron tunneling. During the release and relax phases, the tunnel barriers are lowered, and a QCA cell remains unpolarized. However, in our study, two new clocking signals that are different from the conventional *Landauer-type clocking* signals and four phase shifters are employed, which are discussed in detail in Sections 3 and 4.

3. QCA MEMORY CELL ARCHITECTURE AND CLOCK CIRCUITRY ANALYSIS

3.1. *Memory cell review*

In this Section, the drawbacks of the previous memory cell are first presented, and then the importance of clock circuitry routing and Read/Write peripheral circuitry are highlighted. In memory technologies, there exist two famous types of architectures: parallel and serial architectures. A parallel architecture provides the substantial advantage of low latency because each memory cell processes its own bit, hence there is no additional delay in that bit when comparing to serial storage process in serial QCA memory cell design [23]. Thus in this paper, only parallel architecture is used to construct QCA memory cell or a larger structure mainly due to its advantage of process-in-parallel.

The pioneer work on QCA memory is reported in the literature [24], which adopts SQUARES to construct memory circuits with a module unit comprising a set of standard circuit elements; all these circuit elements occupy the same layout area. By SQUARES, it is very useful to construct a memory cell expediently, but these uniform architectures waste considerable layout area, and also the clock circuitry underlying the modular element is difficult to route due to its small and irregular clock zones. Walus [16] proposes a parallel memory cell based on loop operation. This memory cell architecture comprises eight QCA logic gates, five AND gates, one OR gate and two NOT gates, costing 158 cells. Its main advantage is that the stored bit keeps motion in memory loop ceaselessly, which is helpful to read operation at any time. However, we see that it needs six

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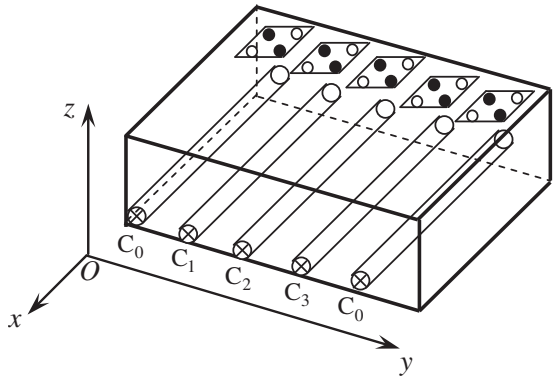

Figure 3. Schematic diagram of QCA clock wire.

control cells (fixed polarization cell); also data in each memory cell are stored using a closed QCA wire loop (four consecutive clock zones). The clock zones are also relatively short and irregular in this layout, causing clock circuitry routing problems and affecting its physical implementation.

Recently, literatures [17–19] proposed novel line-based parallel memory cell implementation. These architectures are based on unique logic operation of majority gate, namely that the majority gate can behave differently between wire and majority gate depending on new clocking signal phases. Three new clock zones and two new clock zones are added to these two memory cells, respectively, overcoming the limitation of a traditional unidirectional flow of logic signals in QCA. Compared with loop-based memory cell [16], line-based memory cells need less clock zones, hence memory cell is slightly simplified, and also the clock circuitry routing becomes easier than the previous design. However, peripheral Read/Write circuits of these architectures are complex, clock circuitries of this section and the entire memory cell are still difficult to fabricate despite the improvement compared to loop-based core. For example, from the layout in [18, 19], one can see that clock zones do not display a clear and regular partition. Moreover, these two kinds of memory cell cost many cells, control cells and layout areas. Thus the design of memory cell calls for further research, which is performed in this paper.

3.2. QCA clock circuitry

In Section 2.2, we refer to a detailed description of QCA clock signal. QCA circuits can be manipulated using an array of wires [25] buried in the substrate below the QCA cells, which is shown in Figure 3. Here, a time-varying, seven-phase clocking voltage could be applied to the wires, yielding regions in the device plane where the QCA cells are activated.

Each clocking wire creates a clocking field with moving active zones. In general, popular four clock zones are arranged adjacent to each other. Clock 0 signal, buried under the cells in clock zone 0, is generated by a clock signal generator, then three phase shifters are used to generate Clock 1, 2, 3 signals, respectively. As seen from Figure 3, electric field intensity E_z (limited to the vertical direction) formed by the clock signal modulate the tunnel barriers between quantum dots, leading to switching or releasing of QCA cell. In terms of physical design perspectives, clock zones are expected to be regular and relatively large for practical manufacturable clocking wires. However, in the previous memory cell designs, only memory cell cores satisfy this condition, the Read/Write circuit and overall structure is still complex in clocking wire arrangements.

4. PROPOSED MEMORY CELL DESIGN

The proposed six clock zones parallel memory cell is shown in Figure 4(a), which uses a serial Read/Write ($\overline{R}/W$) signal, a serial Data Input (I) signal, a parallel Enable (*EN*) signal (note that the physical location of stored bit is known in advance) and a parallel Output signal (*Mem*).

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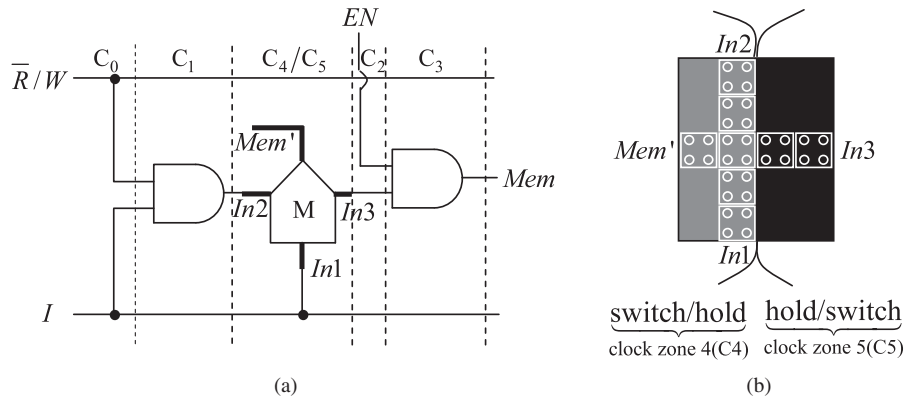

Figure 4. Proposed memory cell: (a) schematic diagram of memory cell and (b) memory cell core.

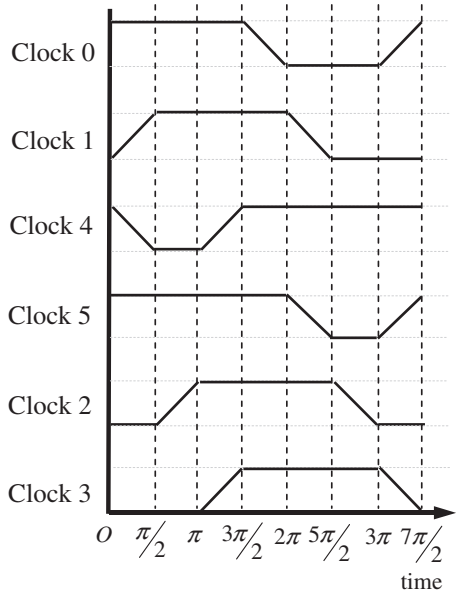

Figure 5. New four clock zones scheme and two additional clock zones signals (clocks 4 and 5).

It comprises two AND gates and one majority gate. The majority gate is the core of the memory cell, its input–output terminals are labeled with a thick black line and its layout is shown in Figure 4(b).

For the implementation of memory operation, two additional clock zones are also offered to the majority gate. As shown in Figure 4(b), the left part of the majority gate is arranged by clock zone 4, whereas the right part of the majority gate is arranged by clock zone 5. Waveforms of all the clock zones are presented in Figure 5. C_0, C_1, C_2 and C_3 are congeneric signals, which can be implemented by one new clock signal generator and three phase shifters, whereas C_4 and C_5 are two additional clock zones, which can be implemented by another new clock signal generator and a phase shifter. The proposed QCA memory cell introduces a two-step operation to process writing and reading. In step 1, clock zone 4 switches when clock zone 5 is holding, and write occurs. In step 2, clock zone 5 switches when zone 4 is holding and read occurs. With such an operation mechanism, the stored data moves back and forward between $In3$ and Mem', constituting the memory operation. First, $In1$ and $In2$ of the majority gate is given here,

$$In1 = I, \quad In2 = \overline{R}/W \cdot I \tag{1}$$

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When the two additional clock zones are applied in the memory cell core, inputs to the majority gate alternates between $(In1, In2, Mem')$ and $(In1, In2, In3)$, hence the memory cell presents a different operation as clocking changes. The detailed illustrations of the memory cell operation process are as follows.

(1) *Write operation*. During the write mode ($\overline{R}/W=1$), the left AND gate outputs the new value from I. At the same time, Data bit I is transferred to $In1$. Now the memory cell core starts to work. As shown in Figure 4(b), clock zone 4 is in the switch phase and clock zone 5 of memory cell core is in the hold phase (see Figure 5, C_4 from π to $3\pi/2$, C_5 from π to $3\pi/2$). In the meantime, C_1 is also in the hold phase, since the two adjacent clock zones 1 and 5 are in hold phase, so clock zones 4 can perform a successful switching. The four QCA cells $In1$, $In2$, $In3$ and Mem' form a majority gate, where cells $In1$, $In2$, $In3$ become the inputs and Mem' becomes the output of the majority gate. According to Equation (1) and the computation principle of majority gate, output Mem' of the majority gate would become $I(Mem'=I\cdot I+I\cdot In3+I\cdot In3=I)$ regardless of the value of $In3$. Thus a new data bit is written into the memory cell.

(2) *Read operation*. From $\pi/2$ to π, C_5 is in the hold phase whereas C_2 is in the switch phase, hence the stored value $In3$ is transferred to the right AND gate. The right AND gate is called an enable gate and operates independently from the rest of the circuit. In either read or write mode, the enable gate outputs the stored value (old bit value) when *EN* is 1. This shows that the memory cell is selected to be read. Otherwise, when *EN* is 0, the output is 0 which means that the memory cell is not selected to be read. During the read mode ($\overline{R}/W=0$), the output of the left AND gate is forced to output 0, where it rejects the new value from I. After a clock cycle (2π), clock zone 4 is in the hold phase and clock zone 5 of memory cell core is in the switch phase (see Figure 5, C_4 from 3π to $7\pi/2$, C_5 from 3π to $7\pi/2$). Similarly, the four QCA cells $In1$, $In2$, $In3$ and Mem' form a majority gate, where cells $In1$, $In2$, Mem' become the inputs and $In3$ becomes the output of the majority gate. Owing to C_4 keeps in hold phase (from $3\pi/2$ to 3π), $In1$, $In2$, Mem' hold data bit I. Now the output $In3$ of the majority gate would become $I(Mem'=I\cdot I+I\cdot I+I\cdot I=I)$. Once *EN* is 1, the memory cell is selected to be read, hence the new stored bit value is read out.

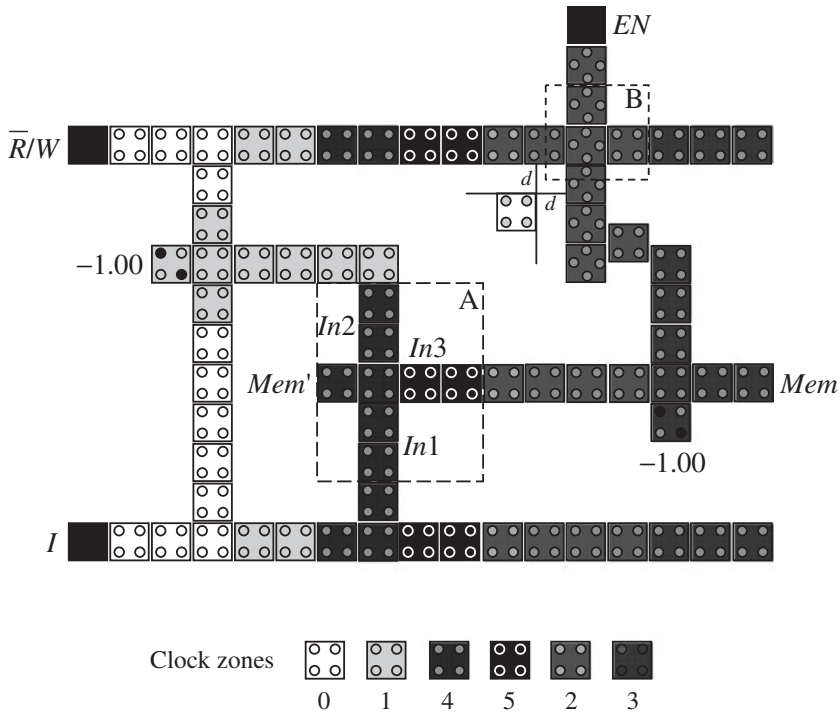

Figure 6. Layout of the proposed one bit memory cell.

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From the schematic diagram in Figure 4(a), we can see that the proposed memory cell is compact, costing less logic gates and clock zones. Moreover, one substantial advantage is that this design supports regular clock zones, leading to regular clock circuitry, C_0 to C_5 is partitioned clearly. Write and Read operations perform well through two new clocking signals and six clock zones (see Figure 5). Regular clock circuitry is helpful for manufacturing and fabricating a larger word length parallel memory architecture The layout of the proposed memory cell is shown in Figure 6, using 75 cells. We herein adopt different shades of gray (see Figure 6) to represent the different clock zones (clock zones 0, 1, 2, 3, 4, 5); full black boxes denote three input signals $\overline{R}/W$, I, EN, respectively. The memory cell core is labeled with a dashed rectangle A. In the meantime, some design rules are taken into consideration for obtaining optimal performance. That is, the minimum separation of two different signal wires is the width of two cells; also coplanar wire crossing presented in Figure 2(b) is employed in this layout, which is labeled with a dashed rectangle B. Moreover, one fixed polarity cell is placed near the intersection of coplanar wire crossing, which is discussed in the following section.

5. SIMULATIONS ANALYSIS AND COMPARISONS

5.1. Function simulation of the proposed memory cell

The logical correctness of the aforementioned design is checked with soft analysis, whereas the handcrafted layout is simulated with the QCADesigner tool [26], using coherence vector simulation engine. However, in QCADesigner clocking can only be simulated using conventional four clock zones, which does not meet the required clocking here. As the source code of QCADesigner is open, some modifications are made to the simulation software. In order to process six clock zones simulation, two new clocking signals are added to the simulator. Thus we integrate clock 0 and clock 4 signals description code writing in C++ into QCADesigner source code, and then compile it to form a modified software. The cell size parameter is chosen as $10\,\text{nm} \times 10\,\text{nm}$, while the 'radius of effect' parameter, which describes how far one cell will polarize its neighboring cells, is kept at 30 nm in order to encapsulate all the eight cells around it. All other parameters are kept at their default values in the simulator. The input and output waveforms of the memory cell is shown in Figure 7, with input vectors $\overline{R}/W = 00111000011$, $I = 01110011100$ and $EN = 101010101010$. We find that when C_2 is in the hold phase and EN is high, a read operation occurs. Two read operations and two write operations are observed in this case. The first read operation reads the old bit existed in the memory cell. At the same time, a write operation happens when $\overline{R}/W$ signal is high, data I is written into the memory cell. Then the second read operation reads out the new data bit '1' from I (new data bit emerges after latency $7T/4$, here T denotes clock period, $T = 2\pi$). It can be observed that *Mem* takes the value of I. In the meantime, the second write operation happens. Simulation has therefore shown that the logic and timing features of the proposed memory design perform well.

5.2. Analysis of noise effect in memory cell

The experimental simulation is performed without considering the effect of noise; we see that, as expected, the proposed memory cell architecture demonstrates correct operation and generates valid output. However, since the effect of noise is an important factor in circuit simulation, it is also true for QCA circuits. However, all the experimental verifications of the memory cell in the previous literatures do not consider noise effect. In order to consummate the memory cell designs, in this subsection all the memory architecture would be subject to more simulations in which the effect of noise is contained.

The representations of noise in QCA circuits differ from that in conventional technologies since Coulombic interaction dominants information flow in QCA. Generally speaking, noises in the QCA circuit refer to sneak noise and random charge. Sneak noise is created due to clocking phase shift [27] and lack of clocking symmetry. In this design, sneak noise problem has been solved by arranging the QCA cells and clock zones in such a regular and symmetrical way (see Figure 6),

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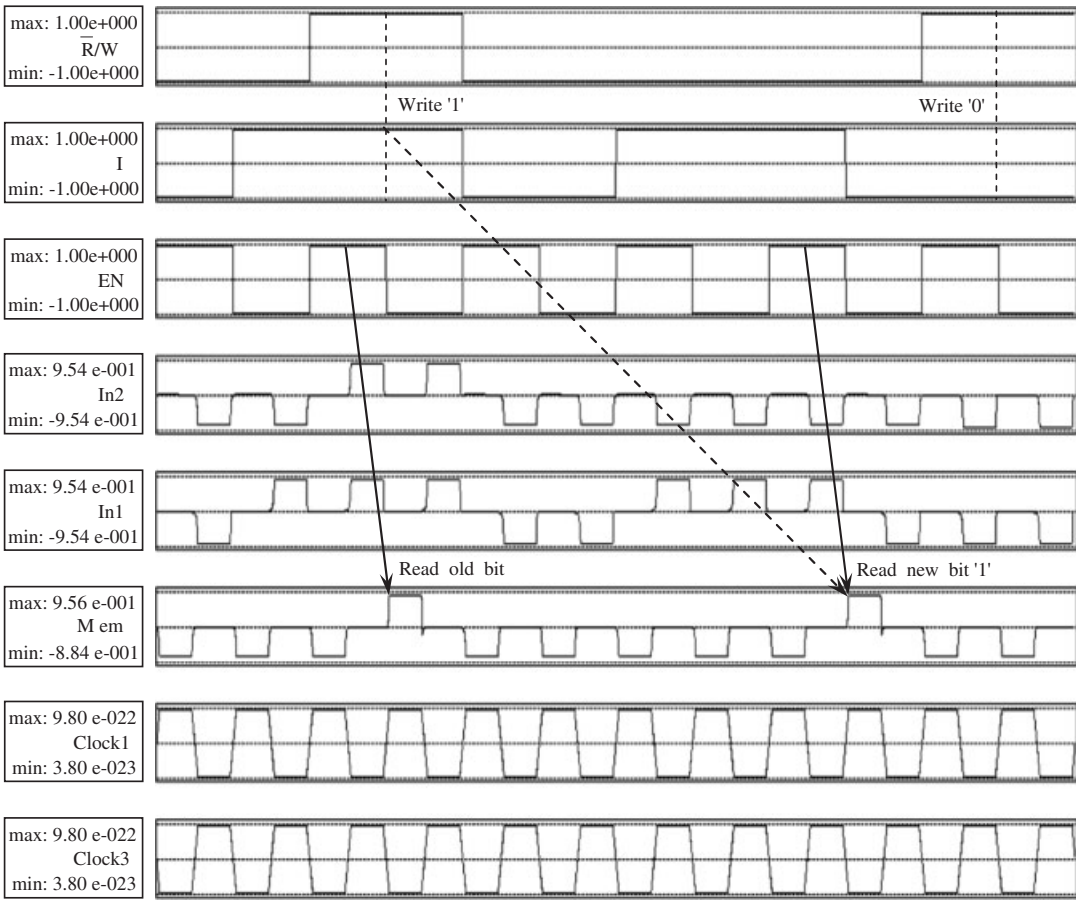

Figure 7. Simulation result of proposed memory cell.

that unwanted signal coupling is diminished, hence sneak noise has not been highlighted here. Instead, random charge may have great effect on the circuit performance and requires detailed analysis to determine how it malfunctions the memory cell. Random charge is equivalent to mobile electrons in QCA circuits, which is modeled with a fixed polarity cell in this paper. In Figure 6, d represents the distance between the horizontal wire and the fixed polarity cell or the vertical chain and the fixed polarity cell.

To see the effect of random charge noise on the performance of the memory cell architecture, assuming that QCA wire crossing subjects to noise effect, then we can obtain universal results about whether noise alters the performance of the memory cell since wire crossing is the weakest spot in QCA circuits. The experimental simulations are conducted by increasing d (vertical axis) in increments 1 nm and cell polarization 0.1(horizontal axis), respectively. The responses of memory operation are plotted for various values of d and cell polarization shown in Figure 8; the region above the curve represents that the memory cell has a successful operation (succeed) when noise exists, whereas the region below the curve represents an unsuccessful operation (fail) in the memory cell. It can be seen from Figure 8 that the further away from the intersection that the fixed polarity cell is, the less susceptible to noise this architecture becomes. This occurs because distant random charges generate weak Coulombic interaction energy to this circuit; clocking introduces some more stability to the Read/Write operation of memory cell to overcome this effect so that the transferring cells can correctly polarize *Mem* cell. Moreover, the results from Figure 8 also suggest that the more random charge (larger cell polarization), the more likely it is to provide incorrect Read/Write operation. Here, this occurs because the Coulombic interaction energy between fixed polarity cell and architectural cells increases as the random charge becomes more. In conclusion, noise certainly

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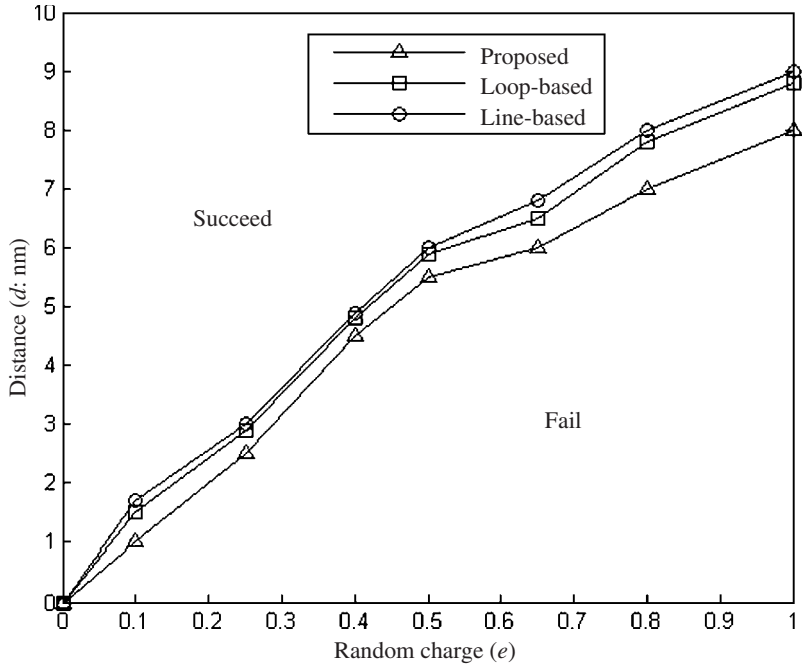

Figure 8. The response of Read/Write operation with noise effect.

Table I. Memory cell characters.

	No. of cells	Control cells	Clock zones	Clock circuitry
[16]	158	6	8	Complex
[17]	233	5	7	Moderate
[18]	173	4	6	Moderate
Proposed	75	2	6	Simple

introduces an effect on the memory cell. In the meantime, simulation results of other counterparts (previous loop-based and line-based) with noise effect are also plotted in Figure 8, we see that the proposed design demonstrates better phenomenon against effect of noise by comparison.

5.3. Performance comparisons of memory cells

In the previous two subsections, the proposed architecture has provided a new QCA design for the memory cell, and simulation and analysis of noise effect have been done to analyze the function of the proposed design. As there are some different designs about QCA memory cell, thus some similar parallel architectures (which refers to designs in [16–18]) are listed here for comparison with proposed design. The memory cell presented in this paper consumes less logic gates when implementing Read/Write and periphery circuit, so the cell and layout area are reduced by nearly 100%. Clock zones are consecutive and compact by only applying six clock zones (see Figure 4(a)). Thus clock circuitry in the proposed design is simpler and more regular than previous congeneric designs. Memory cell characters of different designs which have been compared are summarized in Table I.

Also, the memory capacity comparisons of different designs have been done. Some attention should be paid for the Read/Write operation, multi-period synchronization between clock zone 4, 5 and clock zone 0,1,2,3 must be performed. The total synchronization time is $7T/4$ in the proposed design, performing one read and one write operation, respectively. Memory cell capacities of reviewed parallel design are summarized in Table II. For example, the architecture in [16] performs

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Table II. Memory capacities.

	Read/Write latency	Read throughput	Write throughput
[16]	$2T/1.5T$	$1/2T$	$1/2T$
[17]	$2T/2T$	$1/2T$	$1/2T$
[18]	$T/2T$	$1/T$	$1/2T$
Proposed	$0.75T/1.75T$	$4/7T$	$4/7T$

one read and one write operation in two periods or clock cycles, hence both its read and write throughput is $1/2T$. Read and write bit are available after 8 clock zones and 6 clock zones, respectively, hence the latencies are $2T$ and $1.5T$. From the table, we see that only the Read throughput in [18] is slightly better than the proposed design. But our design has superior performance in terms of the overall performance.

6. CONCLUSION

This paper presents an improved QCA memory cell. The design employs two new clocking signals and compact circuit, using only two AND gates and one Majority Gate. The main advantage of this design is that regular clock circuitry and compact Read/Write circuits is available from this architecture. This design, occupying only a fraction of the area compared with the previous memory design, has a superior performance. As the clock circuitry is very regular, it helps manufacturability for physical implementation. The comparison of congeneric designs shows that the read/write latency of the proposed design is mitigated, the overall cell number, control cell and the layout area are reduced (100%), and also its performance against random charge noise is better. These improvements can help in the construction of larger word length memories and provide the guideline for real fabrication.

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