A 27-GHz Low-Power Push-Push LC VCO with Wide Tuning Range in 65nm CMOS

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***Abstract* — Push-push voltage-controlled oscillators (VCOs) achieve high oscillation frequencies by relying on the boosted second harmonic component of the oscillator. These VCOs however, typically require a high power to deliver a reasonable output swing. In this paper, we first derive an analytical expression that relates the amplitude of the second harmonic of an LC VCO to the C-V characteristics of its varactor. Then based on the results of the analysis, we present the design of a low-power and compact 27-GHz push-push VCO in 65 nm CMOS that exhibits a 28.5% tuning range while consuming 21 mW (including buffers) from a 1 V supply. At 27-GHz output, the VCO achieves a phase noise of –101 dBc/Hz at 1-MHz offset.**

I. Introduction

The design of high-frequency oscillators entails challenging trade-offs among several parameters including the phase noise, frequency tuning range, power consumption and chip area. The integration of high-performance mm-wave voltage-controlled oscillators (VCOs) into the low-cost digital CMOS technologies has been a subject of wide research interest [1–4]. The relatively low f_t frequency of CMOS process as compared to other technologies such as BiCMOS
and HBT, its higher flicker noise, and the limitations of interconnects and device parasitics are among major bottlenecks of the design of high-frequency CMOS VCOs. Several architectures have been proposed to address the aforementioned challenges [2–4].

The push-push VCO is a possible architecture that offers oscillation frequencies above the fundamental frequency of a conventional oscillator. In this architecture, the concept of harmonic amplification is used to constructively add the even-order harmonics of the VCO's fundamental frequency. In practice, the differential outputs of a CMOS LC VCO can be combined to cancel out the fundamental harmonic while amplifying the second-harmonic component and generating a single-ended output. This second-harmonic component is usually weak and typically a relatively significant power is required to bring it to an acceptable swing level. A recent work combines the outputs of two quadrature-coupled LC VCOs to generate differential outputs for a push-push VCO and achieves a two-fold increase in the amplitude of the output signal [1].

In this paper, we present an analytical approach to show that the magnitude of the second-order harmonic of the VCO output is a strong function of the nonlinearity of the C-V characteristics of its varactor. The analysis is supported by simulations to confirm this dependence. Finally, the results of this analysis are used as guidelines to design a wide tuning-range low-phase-noise push-push VCO operating at up to 30 GHz.

The paper is organized as follows: In Section II, the output frequency of the LC VCO with an accumulation MOS (AMOS) varactor is analyzed in large-signal regime and the amplitude of the second-order harmonic of the output is expressed in terms of the circuit parameters. Section III briefly overviews the characteristics of different AMOS varactors and compares the results of simulation against those of analysis. The design and simulation of a 27-GHz LC VCO based on this analysis is then presented in Section IV. Finally, concluding remarks are provided in Section V.

II. Second-Harmonic Generation

Consider the generic RLC circuit shown in Fig. 1, which models the tank of an LC VCO in the steady-state condition. The negative transconductance, $-g_{active}$, is the equivalent transconductance of the cross-coupled active devices that are typically used in such VCOs. In the steady state, the tank parallel loss, R_{tank}, and the equivalent negative active resistance, $-1/g_{active}$, cancel each other. The remaining circuit is a lossless LC tank with a variable capacitance that oscillates when excited (for example by an initial condition). The incremental charge stored on the varactor at any instance of time is given by $dQ = C(V)\cdot dV$.

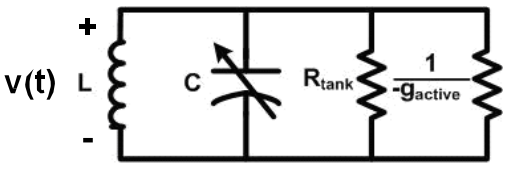

Figure 1. LC Tank Circuit

Thus, we have:

$$\frac{1}{L}\int V(t).dt = -\frac{dQ}{dt} = -C(V)\frac{dV}{dt} \qquad (1)$$

Note that there is no dC/dt term on the right-hand side of (1) which is due to the time-invariant nature of an AMOS

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varactor. Eq. (1) results in the following second-order nonlinear differential equation.

$$C.\frac{d^2V}{dt^2}+\left(\frac{dC}{dV}\right).\left(\frac{dV}{dt}\right)^2+\frac{1}{L}V=0 \qquad (2)$$

A nonlinear term is present in the above second-order differential equation. Therefore, the solution is not as straightforward as that of an LC resonator with constant passive elements. However, it can be shown that the solution is still periodic and thus can be represented by its Fourier series expansion [5]. We study the solution in the large-signal regime using this technique.

The C-V characteristics of an AMOS varactor can be modeled using [6]:

$$C(V) = C_{center} + K\cdot Tanh(\alpha(V_{DC} - V)) \qquad (3)$$

where C_{center} = ½ (C_{max}+C_{min}), $K = C_{min} - C_{center}$ (C_{max} and C_{min} are shown in the top diagram in Fig. 2), α is a varactor constant (in V^{-1}) that determines the slope of varactor capacitance versus voltage variation in its steep region, V_{DC} is the bias voltage and V represents the instantaneous voltage across the varactor. Eq. (3) can be approximated in its steep region by the linear function $C(V) \approx C_{center} + K\cdot\alpha\cdot(V_{DC} - V)$, which then results in:

$$C(V) = C_{center}+\alpha\cdot K\cdot(V_{DC} - V) = C_{bias} - \alpha KV \qquad (4)$$

where, C_{bias} is a fixed bias-dependant term (all the parasitic capacitances in the tank are included in C_{bias}). Expressing $V(t)$ (the output of VCO which is periodic) using the Fourier series expansion:

$$V(t) = \sum_{m=1}^{\infty} a_m \cdot \cos(m\omega t) \qquad (5)$$

Eqs. (1) and (5) can be combined and re-written as:

$$\frac{1}{L}\sum_{m=1}\frac{a_m}{m\omega}\cdot\sin(m\omega t) = \sum_{m=1} m\cdot\omega\cdot a_m \sin(m\omega t)\times \left(C_{bias} - \alpha K\sum_{m=1}^{\infty} a_m \cos(m\omega t)\right) \qquad (6)$$

Assuming the first three harmonics are dominant, Eq. (6) can be solved for a_1, a_2, and a_3 and the following expression is obtained for the amplitude of the second harmonic (a_2):

$$a_2 = \frac{\alpha.K.A^2}{3C_{bias}} \qquad (7)$$

where A is the peak amplitude of the oscillation across the LC tank. This equation demonstrates that the amplitude of the second-harmonic component is directly proportional to the slope of the varactor C-V characteristics (α) and inversely proportional to the fixed capacitances used in the tank. Therefore, a varactor with steep C-V characteristics, combined with a compact and low-parasitic layout, helps increase the amplitude of the second harmonic, and hence save on the power consumption.

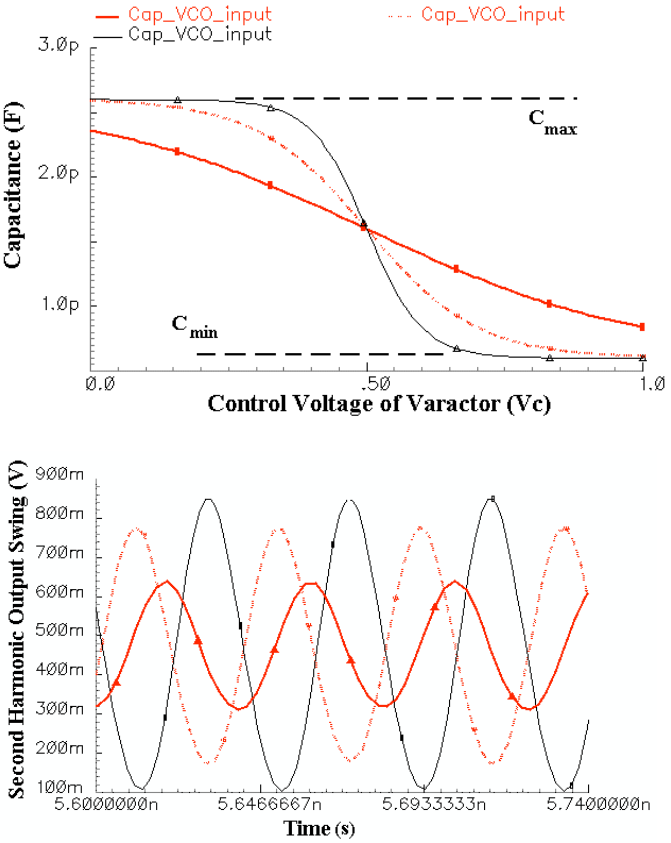

Figure 2. C-V characteristics of varactors with different slopes (αK) and similar C_{max}/C_{min} ratio (Top); Output swing at the second harmonic for different C-V characteristics (Bottom)

In the next section, a few varactor structures are examined to verify the analytical results.

III. MOS VARACTORS

In order to confirm the analytical results of the previous section, an LC VCO is simulated using *SpectreRF*. The varactor is modeled in *VerilogA*, using Eq. (3). From this modeling technique, the slope of the C-V curve in the steep region, parameter αK, is varied and the amplitude of the second harmonic at the output of the VCO (a_2) is observed. The results of these simulations are depicted in Fig. 2.

As can be seen from Fig. 2, a steeper C-V characteristics results in a larger output swing at the second harmonic of the LC tank (the fundamental term is cancelled as will be discussed in Section III). With this in mind, we revisit the C-V characteristics of AMOS varactors available in CMOS technology. For this work the following flavors of AMOS varactors are studied:

١) A thin-oxide AMOS varactor with Standard V_t (SVT)
٢) A thin-oxide AMOS varactor with Standard V_t in Deep NWell (SVT-DNW)
٣) A thin-oxide AMOS varactor with High V_t (HVT)
٤) A thick-oxide AMOS varactor

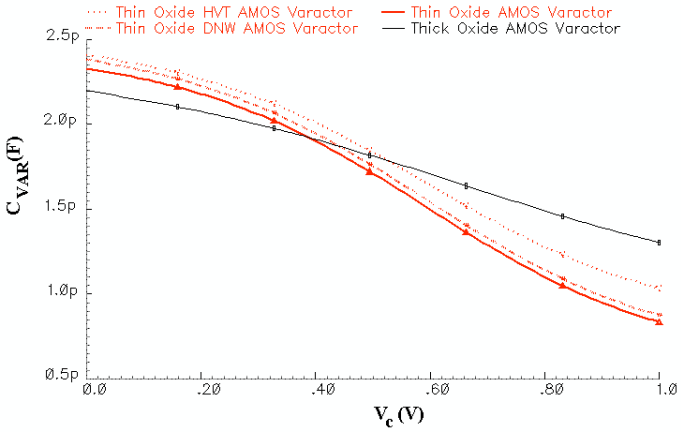

Figure 3. C-V characteristics for different varactors in CMOS process (W = 1.6 µm, L = 400 nm, Multiplier = 200)

The C-V characteristics of these varactors (capacitance C_{VAR} versus the control voltage V_c) are shown in Fig. 3. The thin-oxide AMOS varactor offers a steeper C-V characteristics which makes it a suitable candidate for harmonic amplification. It also offers a smaller parasitic capacitance and a larger capacitance ratio (C_{max}/C_{min}) that, respectively, result in a higher frequency and an increased tuning range of the VCO.

IV. Design and Simulation

The schematic of a cross-coupled push-push LC VCO designed in 65nm CMOS technology is shown in Fig. 4. To demonstrate the feasibility of integration into a low-cost digital process the use of low-threshold voltage (LVT) transistors and Deep-NWell devices is avoided. The tail-current source of the VCO is eliminated to increase the headroom for low-supply-voltage operation (1V). One advantage of this approach is the removal of the tail-current noise, which would otherwise fold back into the close-in phase noise of the VCO. The structure also eliminates the need for the tail current source, current mirror, and the associated bias circuitry. Furthermore, the increased oscillator swing due to the added headroom improves the phase-noise performance and boosts the second harmonic content quadratically, according to Eq. (7).

As discussed in the previous section, a thin-oxide AMOS varactor is used to provide a large tuning range. The value of the inductor is chosen as a compromise between the phase noise and the tuning range. To further reduce the parasitics, a 2-turn vertical (helical) inductor is designed, as depicted in Fig. 5, using the top three metal layers, which also saves the silicon area due to its compactness. The inductor has a third lead which is the center tap of the asymmetric inductor. The automatic sum of the VCO complementary outputs at the center tap suppresses the fundamental frequency of the VCO and amplifies its second harmonic.

Extracting the second harmonic at this node eliminates the need for bulky inductors [1], external bias-T [2] or otherwise long interconnects needed to prevent the second harmonic component from sinking to the supply in typical CMOS push-push VCOs. The inductor is designed and simulated using

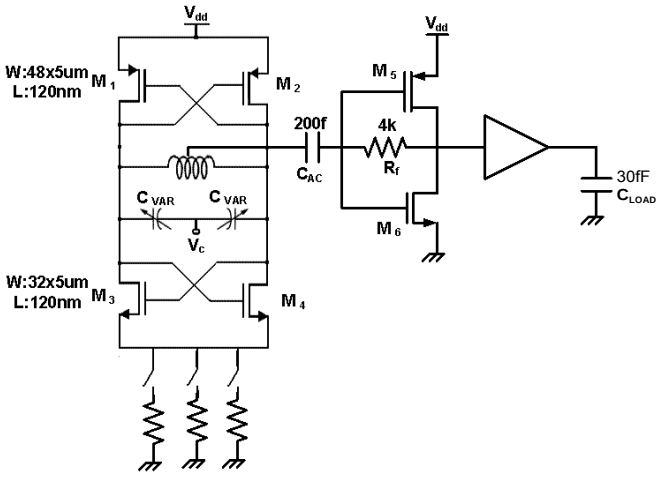

Figure 4. Schematic of 27-GHz push-push VCO and its output buffer

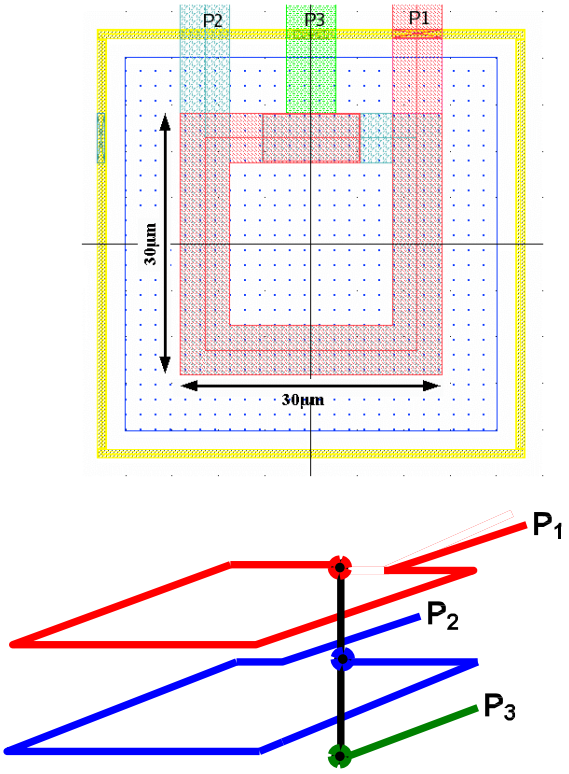

Figure 5. Layout of compact center-tapped asymmetric inductor (Top) Lateral view and via connections (Bottom)

Momentum (an electromagnetic simulator from Agilent EEsof electronic design automation). The simulated inductance and quality factor at 13.5 GHz (fundamental frequency of the LC tank) are L = 108 pH and Q = 7.5, respectively.

To amplify the second-harmonic component over a wide frequency range, the center-tap output of the inductor is AC-coupled to the input of a transimpedance amplifier with a feedback resistance of R_f = 4 kΩ. This configuration helps maintain proper operation of the circuit over process, temperature and supply voltage variations. It also avoids the use of tuned amplifier and the associated bulky passive components. A final two-stage CMOS buffer boosts the

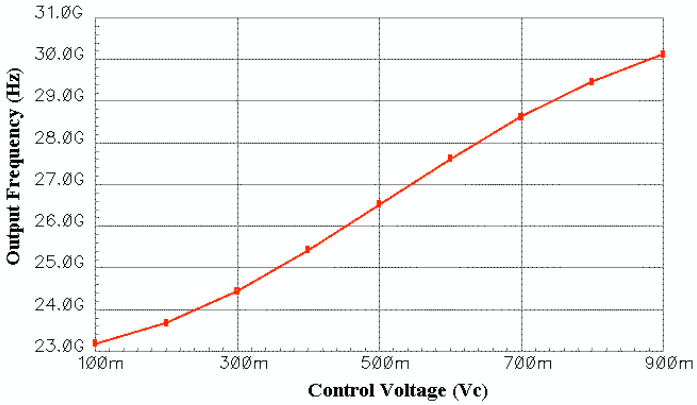

Figure 6. Tuning curve of the push-push VCO versus the control voltage

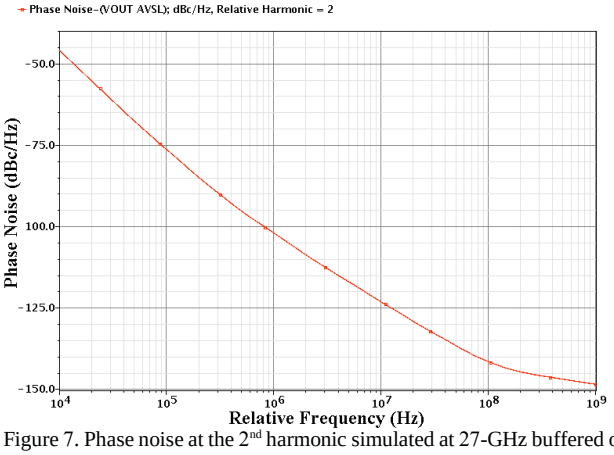

Figure 7. Phase noise at the 2nd harmonic simulated at 27-GHz buffered output

output to near rail-to-rail swing to drive the following stage, such as an on-chip mixer. The load assumed here is 30 fF.

The g_m of the active devices is mainly governed by the size of the NMOS and PMOS transistors since no explicit tail current source is present. Therefore, a set of programmable parallel switches is added to control the total resistance to the ground which in turn controls the g_m and power consumption. This scheme allows for a trade-off between noise and power consumption across the frequency band.

The leads of the inductor and routing metals are modeled using parasitic elements in *Momentum* and back-annotated into the schematic. The VCO core draws about 13 mA from a 1V supply. The tank oscillation at half the output clock frequency allows a broad tuning range of 23.2 GHz to 29.8 GHz at the output. The tuning curve of the VCO versus the control voltage is shown in Fig. 6. It was observed that as the control voltage moves from its center value ($V_{dd}/2$) towards the extreme ends (min or max) of the tuning range, the effective slope of the varactor's C(V) reduces, resulting in a reduced second harmonic content at the center tap of the inductor. This agrees well with the results of Eq. (7) and implies that design optimization for push-push VCOs must be
carried out at these extreme voltages to guarantee satisfactory swing levels at the output. In other words, there is a trade-off between the tuning range and the output swing at the doubled frequency. The oscillator exhibits a phase noise of –101 dBc/Hz at 1-MHz offset of a 27-GHz output (LC tank tuned at 13.5 GHz). Table I summarizes the performance of this VCO and compares it with the state-of-the-art.

TABLE I. Performance Summary and Comparison

Ref	Technology	f_{out} (GHz)	Power (mW)	Phase Noise (dBc/Hz)	Typical Tuning Range**
[2]*	0.35 µm	30.9	117	–102.3 @1 MHz	N/A***
[3]*	0.18 µm CMOS	29.9	27	–109 @1 MHz	0.7%
[4]*	0.13 µm CMOS	26.3	36.5	–92.6 @1 MHz	26.5%
This Work	65 nm CMO	26.7	21	–101 @1 MHz	28.5%

* Measured results.
** $100 \times (f_{max}/f_{min}-1)$
*** This is an oscillator with fixed output frequency.

V. CONCLUSION

The effect of AMOS varactor non-linearities on the amplitude of the second harmonic in CMOS LC VCOs is analytically studied. Using the results of this study, a 27-GHz push-push VCO is designed and simulated in a 65 nm CMOS technology. The VCO achieves a wide tuning range, calculated as ($100 \times (f_{max}/f_{min}-1) \approx 28.5\%$) while keeping an acceptable compromise between the power consumption (21 mW, including buffers), the output swing and the phase noise (–101 dBc/Hz at 1-MHz offset from 27 GHz). The use of a small and compact vertical inductor, the removal of bias currents, transmission lines and matching components, and finally avoiding LVT and DNW devices makes this VCO design a compact and inexpensive solution that is attractive for system-on-chip (SoC) implementations in general-purpose digital CMOS processes.

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