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A bilayer graphene nanoribbon field-effect transistor with a dual-material gate

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ABSTRACT

This paper introduces dual-material gate (DMG) configuration on a bilayer graphene nanoribbon field-effect transistor (BLGNRFET). Its device characteristics based on nonequilibrium Green's function (NEGF) are explored and compared with a conventional single-material gate BLGNRFET. Results reveal that an on-off ratio of up to 10 is achievable as a consequence of both higher saturation and lower leakage currents. The advantages of our proposed DMG structure mainly lie in higher carrier transport efficiency by means of enhancing initial acceleration of incoming carriers in the channel region and the suppression of short channel effects. Drain-induced barrier lowering, subthreshold swing and hot electron effect as the key short channel parameters have been improved in the DMG-based BLGNRFET.

1. Introduction

Nowadays, there is much excitement in the low-energy electronic properties of sp^2 carbon allotropes including graphene monolayers and bilayers [1–7]. Coupling of the two monolayer graphene sheets in accordance with AB (or Bernal) stacking is the most energetically favorable relative arrangement and has also been observed in crystalline graphite [8]. The bandstructure in the bilayer garphene represents hyperbolic dispersion at the six corners of Brillouin zone, so-called a Mexican hat structure [9,10]. It turns out that charge carriers in transport near Fermi level behave like massive quasiparticles with a finite density of state at zero energy.

The lack of a natural bandgap in pristine graphene reveals some challenges for using in electronic devices [11]. A simple way of opening an energy gap is by lateral quantum confinement which can be induced by patterning a few nm width graphene ribbons [11,12]. The graphene nanoribbons (GNRs) show a reciprocal relationship between the energy bandgap and ribbon width [13]. Typically, gaps larger than 1 eV can be achieved by the widths below 2 nm [14]. In existing device technologies, preparing GNRs associated with well-defined edges faces considerable fabrication challenges when the ribbon width approaches 1–2 nm [15]. It is shown that a gate-induced electric field, which is applied perpendicularly to a bilayer graphene (BLG) surface, opens a bandgap at the charge neutrality point [16]. First principle calculations confirm that both the strength of the electric field and the BLG width are efficiently able to modulate the observed energy gap [16,17]. Hence, using bilayers instead of monolayers can obtain larger gaps at the same width. It is worth mentioning that bandgap in such BLGs still is not comparable to its silicon counterparts leading to a meaningful distance between the on-off ratio of the both technologies. However, the usage of a new computational paradigm based on intrinsic negative differential resistance rather

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than classical approach can circumvent the raised problem in graphene FETs [18,19].

As device pitch shrinks and is particularly downscaled below 100 nm, short channel effects (SCEs) becomes considerably crucial in device characteristics [20]. To suppress these undesirable effects, some techniques such as different gate insulators, electrically-activated source extension and utilizing high-κ dielectrics have been presented [21–23]. Another interesting approach which is commonly used in well-known device designs is called "gate material engineering". Dual-material gate (DMG) structure of a conventional silicon MOSFET, silicon-on-insulator MOSFET (SOI-MOSFET), carbon nanotube field-effect transistor (CNTFET) and junctionless nanowire transistor (JNT) are some early examples of such work [24–27]. Appling the DMG configuration is an efficient approach to enhance immunity against SCEs. In this approach, two gate metals with different work functions, which are laterally merged together, are employed to minimize the sensitivity of source-side barrier from drain potential variation. It is found that this configuration not only reduces short channel effects but also improve gate transport efficiency. In general, carrier transport in MOSFETs starts with a low initial velocity and is gradually accelerated towards the drain end. Relatively slow carrier drift velocity in the channel near the source region can be increased by the DMG configuration resulting in higher average velocity. This is caused by adjusting the electric field distribution and potential profile along the channel. Although this configuration has recently been applied to a monolayer graphene FET [28], exploiting its advantages in bilayer garphene would make the device more reliable as mentioned before. In this paper, we present a dual-material gate bilayer graphene nanoribbon field-effect transistor which combines the advantages of a BLGNRFET with DMG configuration.

The paper is organized as follows: Section 2 introduces the device structure and geometry. In this section, the performed simulation approach incorporating Schrodinger and Poisson equations is described as well. Section 3 deals with a discussion on results and illustrations. Finally, concluding remarks are outlined in the last section.

2. Approach

The sketch of a double-gate BLGNRFET wherein each gate consisted of dual materials with different work functions is demonstrated in Fig. 1. The work function is defined as the separation between vacuum level and Fermi level. Here, the metals near source side have a higher work function over those near drain side, i.e., $\Phi_1=\Phi_3=4.7$ eV and $\Phi_2=\Phi_4=4.4$ eV. A 10-nm-long $N=12$ armchair-edge BLG surrounded by 1.5-nm top and bottom SiO_2 dielectric layers ($\kappa=3.9$) forms the channel region. Source and drain contacts are made from the extensions of the BLG channel. Albeit the channel material is dopant-free, the source and drain regions are uniformly doped with an n-type doping concentration of 0.01 dopant per carbon atom.

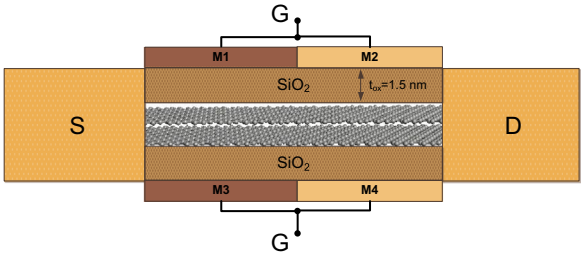

Fig. 1. Dual-material gate bilayer graphene nanoribbon field-effect transistor.

Tight-binding approximation is used to describe atomic details of the BLG channel [29,30]. This approach is a well-known model to obtain an effective Hamiltonian of the channel through fitting the band structure derived from ab initio calculations. The elements of the Hamiltonian matrix are composed of on-site potentials at the carbon atoms of a BLG unit cell and hopping parameters including nearest neighbor interactions.

In simulation procedure, there is a suitable coupling between bandstructure/density of state with the NEGF formulation for quantum transport and full 3D Poisson's equation for electrostatics [31]. Once the Hamiltonian and self-energy matrices incorporating boundary conditions from source/drain contacts are known, carrier concentration of the BLG channel is determined through computing the NEGF formalism and arranged in a density matrix. The concentration is entered into the Poisson's equation so as to calculate potential profile along the channel. The resultant representing the applied gate voltage and any change in the density matrix from a reference condition is thought of as a new input in the NEGF formalism. A self-consistent iterative scheme is performed until the results yield reasonably good convergence. In the whole simulation procedure, thermal conditions are assumed to be fixed at room temperature.

3. Results and discussion

This section evaluates the performance of the DMG configuration on the MOSFET-like BLGNRFET. In the following discussion, dual-material gate and conventional MOSFET-like BLGNRFETs are respectively abbreviated as DMG-BLGNRFET and BLGNRFET. Fig. 2 illustrates the

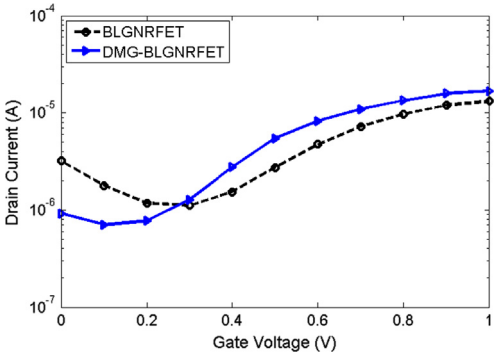

Fig. 2. Transfer characteristics of the simulated device structures at $V_{DS}=0.5$ V.

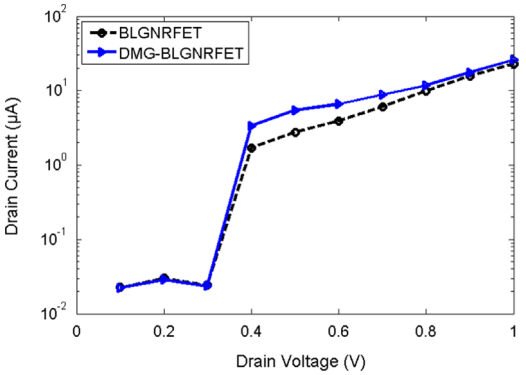

Fig. 3. Output characteristics of the BLGNRFET and DMG-BLGNRFET at $V_G=0.5$ V.

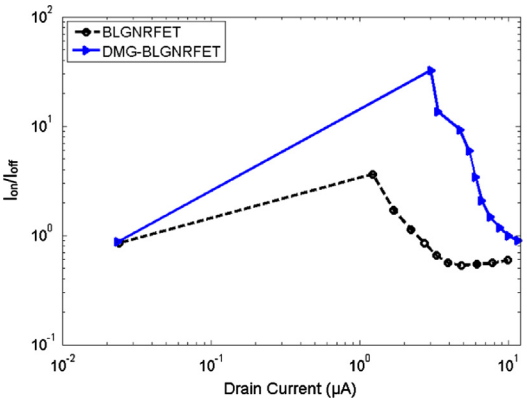

Fig. 4. I_{on} versus I_{on}/I_{off} for two structures is shown in log scale.

transfer characteristics of both the structures at $V_{DS}=0.5$ V. The work function difference induces a stronger electric field enlarging the bandgap near the source-side region of the channel and thereby decreases the BLG conductance in the off state. On the other hand, there is charge accumulation in the middle of the channel caused by the existing difference allowing the saturation current to reach higher values when the device operates at $V_G=V_{DS}=0.5$ V. The output characteristics of the BLGNRFETs confirm that the drain current in the DMG configuration achieves higher current level as well (Fig. 3). As shown in Fig. 4, this leads to provide a better on-off current ratio making the proposed structure potentially appealing in digital applications.

There are two quality measures for the switching behavior of electronic devices which are called intrinsic delay (τ) and power delay product (PDP). The intrinsic delay represents the time required to extract carrier charges from the channel when the device is switched from on to off state. This parameter is defined as $\tau=(Q_{on}-Q_{off})/I_{on}$ where Q_{on} and Q_{off} are the total carrier charges at on and off states, respectively. The latter, the power delay product, indicates the consumed energy per switching event and is calculated from PDP$=(Q_{on}-Q_{off})$ V_{DD}. The induced charge accumulation due to the work function difference is responsible for observing a slight increase in delay profile as shown in Fig. 5(a). On the other

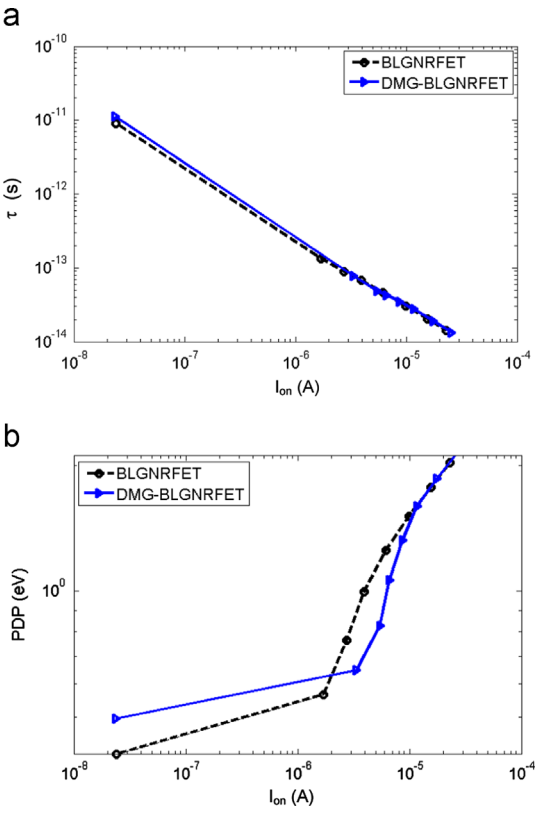

Fig. 5. (a) The τ and (b) PDP of the proposed DMG-BLGNRFET as a function of the on current, compared with those of the BLGNRFET.

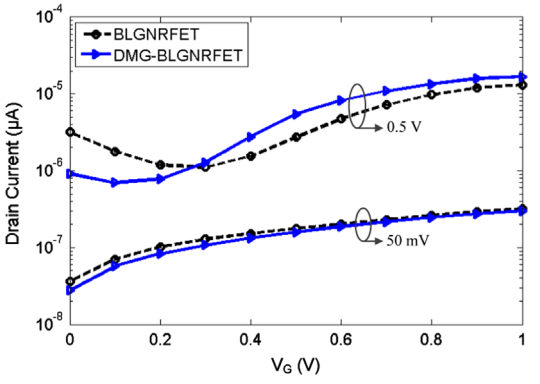

Fig. 6. I_D-V_G characteristics of the simulated device structures on log scale at $V_{DS}=0.5$ V and 50 mV.

hand, these charges in the DMG-BLGNRFET provide more robust transition between on/off states leading to lower dynamic power dissipation (Fig. 5(b)). This behavior is more obvious when the device operates at higher drain currents.

One of the important issues discussed in nanoscale transistors is short channel effects (SCEs) [32]. Achieving good electrostatic control by gate electrodes is a challenging problem as the channel length shrinks. In such dimensions, the variation of drain voltage modulates source-side potential barrier and thereby extra carriers independent of the gate voltage are injected into the

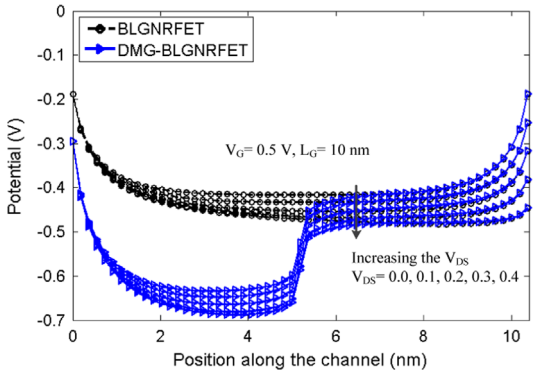

Fig. 7. Surface potential variation along the channel by means of increasing drain voltage where V_G is fixed at 0.5 V.

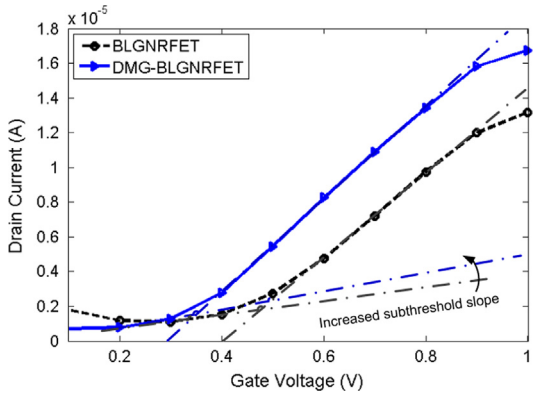

Fig. 8. Drain current for both the structures at V_{DS}=0.5 V.

channel region. This effect is known as drain-induced barrier lowering (DIBL). The ratio $\Delta V_{Th}/\Delta V_{DS}$ is accounted for DIBL values wherein the shift of threshold voltage (ΔV_{Th}) is caused by a variation of the drain-source voltage (ΔV_{DS}) [32]. Based on the results shown in Fig. 6, DIBL is calculated according to the following relationship:

$$\mathrm{DIBL} = (V_{Th}(V_{DS} = 0.5\ \mathrm{V}) - V_{Th}(V_{DS} = 0.05\ \mathrm{V}))/(0.5\ \mathrm{V} - 0.05\ \mathrm{V}) \quad (1)$$

The extracted results show DIBL values of 311 mV/V and 200 mV/V for the BLGNRFET and DMG-BLGNRFET, respectively. Fig. 7 shows the potential profile along the BLG channel. The DMG-BLGNRFET has an abrupt transition in potential profile resulting in charge carriers experience two different electrostatic potentials when travel all the way from source to the drain. Utilizing the metals with a higher work function near the source extension help control gate electrode over the channel region and prepares suitable screening from the drain potential variations.

Short-channel devices suffer from subthreshold current in subthreshold regime as well. For an ideal case, the drain current sharply decreases to zero when the gate bias falls below the threshold. Hence, enabling steeper subthreshold slope is favorable for low-power designs. Subthreshold swing is the voltage swept to drop the drain current by an order of magnitude and inversely equals to the subthreshold slope. Fig. 8 depicts the I_D–V_G characteristics of the

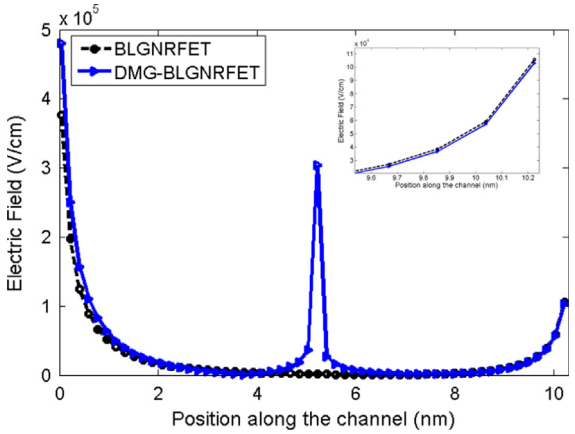

Fig. 9. Distribution of channel electric field for conventional and DMG structures at V_G=1 V and V_{DS}=0.5 V. The electric field profiles near the drain contact are magnified in the inset.

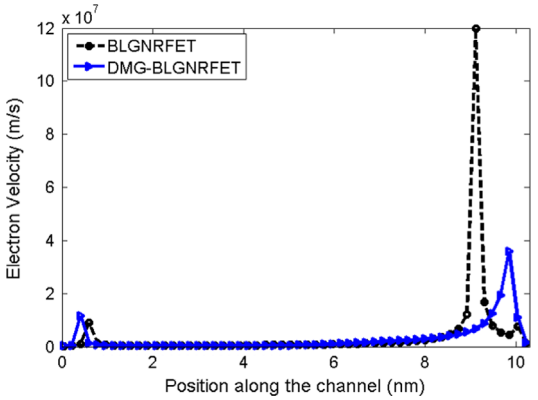

Fig. 10. Average electron velocity profiles of the BLGNRFET and DMG-BLGNRFET at V_G=V_{DS}=0.5 V.

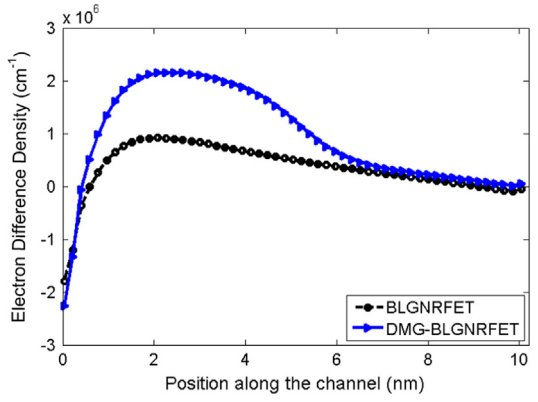

Fig. 11. Electron difference density of the BLG channel at V_G=V_{DS}=0.5 V. This difference is between the self-consistent valence charge density and the superposition of atomic valence densities.

both structures in the subthreshold regime. It is evident that the DMG-BLGNRFET exhibits a reduction in subthreshold swing compared to the BLGNRFET.

To explore the influence of the DMG configuration on device performance, the electric field distribution along the channel is shown in Fig. 9. The central peak caused by the step-like potential profile creates changes in both the adjacent electric field peaks. First, the additional electric field peak enhances the source-side channel field resulting in increased initial velocity of electrons when entering into the BLG channel from the source (Fig. 10). In conventional structures, low initial acceleration is a main reason for lowering carrier transport efficiency which is circumvented in the DMG-BLGNRFET. Secondly, the high channel electric field at the transition of the two gates not only leads to decrease the electric field peak at the drain end but also decelerate the average carrier velocity in the middle of channel. As shown in Fig. 11, a number of electrons are deviated and thereby accumulated underneath the interface and the source-side metals resulting in non-uniform transport towards the drain end. The ongoing electrons from the channel represent significant lower velocity which is a desirable trait for practical applications and improves hot electron effect.

4. Conclusion

The device characteristics of a novel DMG MOSFET-like BLGNRFET have been investigated. Due to the work function difference of the gate metals, an electric field peak is appeared in the middle of the BLG channel. This additional peak alters the electric field distributions near source and drain ends improving both carrier transport efficiency and hot electron effect. Furthermore, DIBL and subthreshold swing values of the DMG-BLGNRFET demonstrate better performance in comparison with those of the BLGNRFET.

The miniaturization of Si MOSFETs suffers from SCEs usually resulting in reduced on-off ratio [33]. Based on Dennard's scaling theory, the depletion depth should be scaled by the same factor as the lateral dimensions in order to maintain suitable controllability over the channel [34]. This is while the process is easily achievable in graphene FETs due to the extremely thin thickness. The DMG structure is able to further increase the on-off ratio by effectively manipulating the potential profile in the BLG channel. Exploiting this approach instead of aggressive scaling postpones fabrication challenges by reducing the probability of imperfections such as defects and roughness usually observed in narrow-width BLGs. Our simulation results indicate that achieving encouraging features such as higher on-off ratio and lower dynamic power in the DMG structure relatively fulfills its promise in digital electronics.

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