A digitally controlled PWM/PSM dual-mode DC/DC converter*

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Abstract: A digitally controlled pulse width modulation/pulse skip modulation (PWM/PSM) dual-mode buck DC/DC converter is proposed. Its operation mode can be automatically chosen as continuous conduction mode (CCM) or discontinuous conduction mode (DCM). The converter works in PSM at DCM and in 2 MHz PWM at CCM. Switching loss is reduced at a light load by skipping cycles. Thus high conversion efficiency is realized in a wide load current. The implementations of PWM control blocks, such as the ADC, the digital pulse width modulator (DPWM) and the loop compensator, and PSM control blocks are described in detail. The parameters of the loop compensator can be programmed for different external component values and switching frequencies, which is much more flexible than its analog rivals. The chip is manufactured in 0.13 μm CMOS technology and the chip area is 1.21 mm^2. Experimental results show that the conversion efficiency is high, being 90% at 200 mA and 67% at 20 mA. Meanwhile, the measured load step response shows that the proposed dual-mode converter has good stability.

Key words: digital power; PSM; ADC; digital proportion integration differentiation; DPWM; buck

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1. Introduction

With the rapid development of portable devices, the demand of high performance conflicting with the requirements of long running times and battery life. As a result, high conversion efficiency has become the key property for the power management of battery powered equipment. Since the load changes with time, the conversion efficiency should be kept high enough over a wide range of load current. Switching mode power supplies with PWM control are widely used due to their high efficiency. However, switching loss is the dominating loss and efficiency will decrease when a heavy load is supplied. PSM control maintains high efficiency at a light load by minimizing the switching frequency in order to reduce switching loss. Furthermore, PSM control has the advantages of better EMI performance than PFM[1]. So PWM/PSM dual-mode control is gaining increasing popularity in switching mode DC/DC converters.

Digitally controlled power converters are becoming more and more competitive than their analog rivals due to their inherent advantages, such as being programmable for different applications, robustness with noise and process variation, and the convenience of implementing advanced control schemes[2, 3]. In addition, while signal processing ability is rapidly increasing with technology scaling, analog circuit design is facing many more barriers in nanometer scale technology. With the support of EDA tools, digital control schemes can be synthesized, placed and routed automatically with minimum modification under different processes.

Based on digitally PWM mode control and PSM mode control, a digitally controlled PWM/PSM dual-mode buck converter is implemented in this paper. The converter works in PSM at DCM and in PWM at CCM. The digital PWM control loop is composed of a 5-bit differential ring-oscillator an ADC, a 10-bit DPWM and an IIR filter as loop compensator. Efficiency remains high over a wide load range by automatic mode switching.

2. Architecture of the digitally controlled PWM/PSM dual-mode DC/DC converter

Figure 1 shows the block diagram of the proposed digitally controlled PWM/PSM dual-mode DC/DC converter. The power inductor L and capacitor C are off-chip, forming a low pass filter, and the dashed rectangular blocks form the digitally controlled dual mode controller. The output voltage $V_{\rm OUT}$ is sampled by a sample network formed by resistors $R_{\rm F1}$ and $R_{\rm F2}$. The feedback voltage $V_{\rm FB}$ is fed to the input of the ADC and the comparator COMP. The PWM control loop contains an ADC, a digital compensator and a DPWM. The comparators in the ADC, over current comparator OCC and main control gate PSM&MODE make up the PSM control loop. The operation mode is chosen by mode switching. The power MOS MP and MN are driven by driver logic and zero current comparator ZCC, which helps to realize synchronous rectifier in DCM. The bandgap reference provides a reference voltage $V_{\rm REF}$ for the ADC and the bias current of the whole chip. The external clock signal CLK is 32 MHz.

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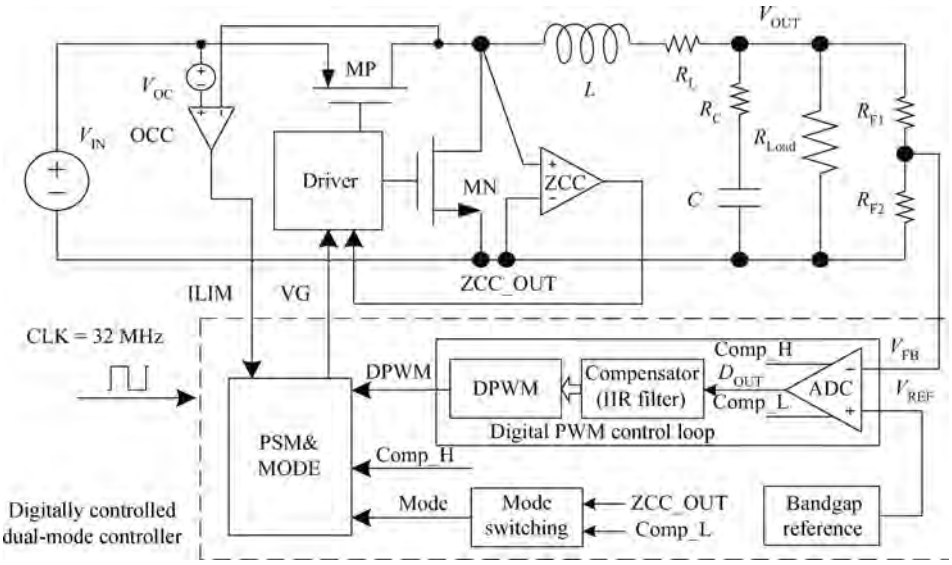

Fig. 1. Block diagram of the proposed digitally controlled PWM/PSM dual-mode DC/DC converter.

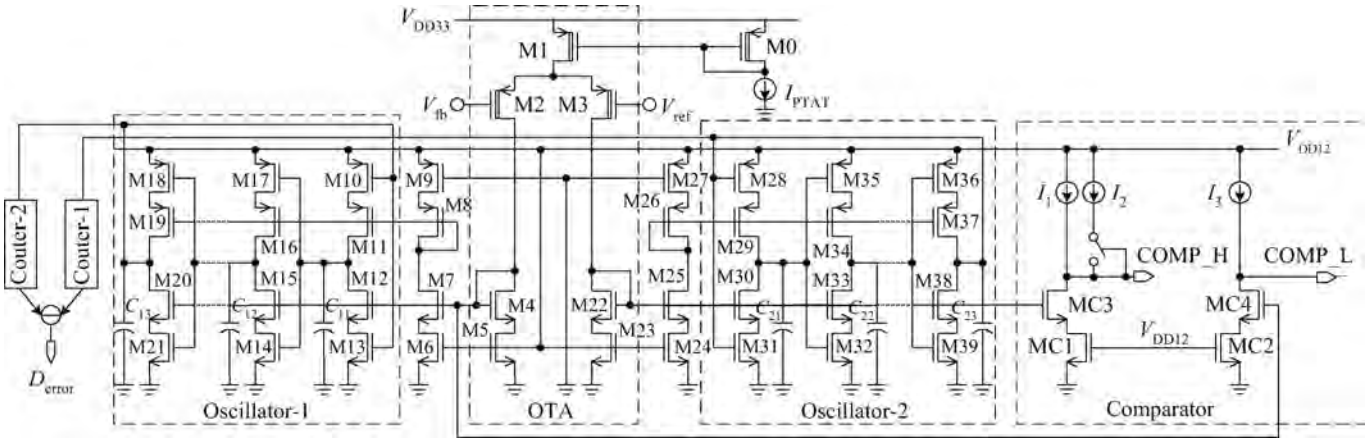

Fig. 2. Simplified schematic of a differential ring-oscillator ADC with a voltage comparator.

2.1. Design of the PWM control loop

The difficulty of digitally controlled PWM converter design is to minimize steady-state limit cycles while maintaining a high static accuracy. Limit cycles appearing in digitally controlled power converters are caused by the quantizing effect of the ADC and the DPWM. The resolution of the DPWM should be greater than that of the ADC to eliminate limit cycles[4]. In this paper, the ADC quantization bin size is chosen to be 15 mV, which means 8.13-bit resolution for a 4.2 V input. The DPWM is designed to be 10-bit resolution at a 2 MHz switching frequency, which needs 4.1 mV step for 4.2 V input.

2.1.1. Differential ring-oscillator ADC

The ADC is the key building block in a digital power converter. The main specifications are low power consumption, small area and small conversion delay. Windowed flash ADCs are used in fast response power converters since they have the advantage of a fast conversion speed, and disadvantages of mass analog design and high power dissipation. Delay-line ADCs' power and area consumption can be well-controlled but not for process or temperature impact. Although there have been several improvements in delay-line ADC design, the conversion linearity is still not good enough due to the nonlinearity relationship between the delay time and the supply voltage[5].

In contrast, ring-oscillator based ADCs can reach better linearity since the oscillation frequency of a ring oscillator is proportional to the supply voltage or current. The schematic of the proposed differential ring-oscillator ADC is shown in Fig. 2. It consists of OTA and two oscillators. M0–M3 are thick oxide transistors powered by V_{DD33} for a wider input range and the others are thin-oxide transistors powered by V_{DD12} for lower power consumption. The differential voltage between V_{FB} and V_{REF}, ΔV, is converted to differential current between M2 and M3, resulting in a differential frequency output by oscillator-1 and oscillator-2. Counters 1 and 2 record the cycle numbers of the oscillators during each sample period. In this work, the sample frequency is designed to be the same as the switching frequency, 2 MHz. The digital expression of voltage error D_{error} is obtained after subtracting the outputs of the two counters. Level shifters are eliminated compared to a voltage controlled oscillator (VCO) based ring-oscillator ADC since

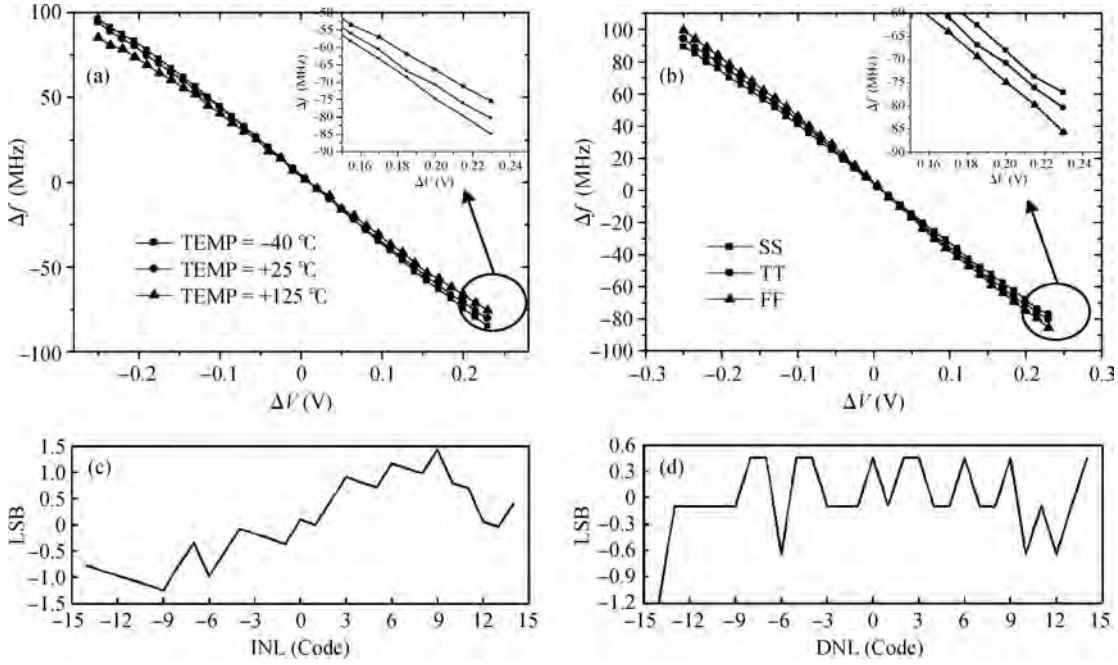

Fig. 3. Simulation results of differential ring-oscillator ADC. (a) Δf versus ΔV at different temperatures. (b) Δf versus ΔV at different corners. (c) Simulation result of INL. (d) Simulation result of DNL.

the voltages of each node can swing from power to ground. Additional comparators are designed by reusing the output of OTA. The outputs of the comparators are COMP_L and COMP_H, and their crossover voltages are lower and higher than $V_{\rm REF}$ by tens of mill volts, respectively. The outputs of the comparators, COMP_L and COMP_H, are designed for mode transition and PSM control, which will be described in detail in Section 3.

The current in M2 and M3 can be given approximately by

$$\begin{cases} I_{\rm M2} = \dfrac{I_{\rm M1}}{2} - \dfrac{V_{\rm fb} - V_{\rm ref}}{2}{\rm GM}, \\ I_{\rm M3} = \dfrac{I_{\rm M1}}{2} + \dfrac{V_{\rm fb} - V_{\rm ref}}{2}{\rm GM}, \end{cases} \tag{1}$$

where ${\rm GM} = \sqrt{2k'(W/L)M_{2,3}I_{\rm M2,3}}$, k' is a process dependent coefficient, and W/L is the width-length ratio of the transistor. The propagation delay of the ring oscillator is

$$\begin{cases} \tau_{\rm OSC1} = \dfrac{V_{\rm DD12}C_{\rm eq}}{2I_{\rm M2}}, \\ \tau_{\rm OSC2} = \dfrac{V_{\rm DD12}C_{\rm eq}}{2I_{\rm M3}}, \end{cases} \tag{2}$$

where $C_{\rm eq}$ is the total capacitance at the node of C11–C1N and C21–C2N which is connected to the MOS transistor's gate. The difference of frequency Δf is sampled by the two counters and subsequently the output of differential ring-oscillator ADC can be expressed from Eqs. (1) and (2) as

$$\begin{aligned} D_{\rm error} &= {\rm Int}(\Delta f T_{\rm s}) = {\rm Int}\left[\left(\frac{1}{\tau_{\rm OSC1}} - \frac{1}{\tau_{\rm OSC2}}\right)T_{\rm s}\right] \\ &= {\rm Int}\left[\frac{2\Delta V T_{\rm s}\sqrt{2k'W/LI_{\rm M1}}}{V_{\rm DD12}C_{\rm eq}}\right] \\ &= {\rm Int}(\Delta V K_{\rm ADC}), \end{aligned} \tag{3}$$

where $T_{\rm s}$ is the sample time interval, $K_{\rm ADC}$ is $2T_{\rm s}\sqrt{2k'(W/L)I_{\rm M1}}/(V_{\rm DD12}C_{\rm eq})$, ΔV is equal to $V_{\rm FB} - V_{\rm REF}$. Thus $D_{\rm error}$ is proportional to ΔV. $T_{\rm s}$ is designed to be equal to switching period, 0.5 μs. For a differential MOS pair operating in a strong inversion region, biasing with a proportional-to-absolute temperature (PTAT) current source relatively stabilizes the transconductance GM. The process variation can also be well controlled since process parameters influence $K_{\rm ADC}$ as the square root.

The relationships between Δf and ΔV are simulated at different temperatures and process corners by HSPICE, where $V_{\rm DD33} = 3.3$ V and $V_{\rm DD12} = 1.2$ V. The temperature and process dependence of $K_{\rm ADC}$ is a relative constant, which can be seen from Figs. 3(a) and 3(b). The variation of $K_{\rm ADC}$ as the temperature changes from −40 to 125 ℃ is less than 11.7%, and the variation of $K_{\rm ADC}$ as the process changes between TT and SS at 25 ℃ is less than 8%. Therefore, the nonlinearity of the ADC due to temperature and process variation is small. When the converter works in the steady state, the power dissipation of the ADC is 380 μW, which is small enough for power converters in portable devices. The resolution of the ADC is 5-bit and its sample rate is 2 MHz. The ADC LSB is 15mV and its input range is ± 384 mV around $V_{\rm REF}$. The simulated INL and DNL are shown in Figs. 3(b) and 3(c), respectively.

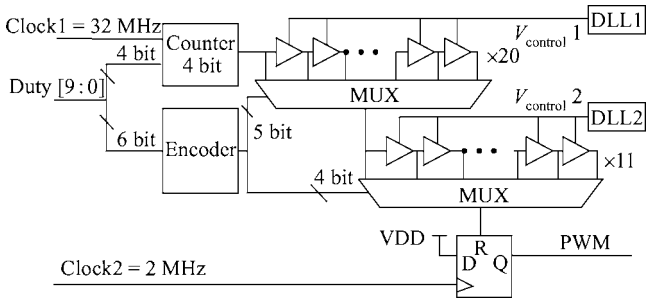

Fig. 4. Diagram of high resolution DPWM.

2.1.2. Hybrid DPWM

The time domain resolution of a DPWM is determined by the external clock period. For a given switching frequency, f_s, the external clock should be $2^n f_s$ to achieve n-bit resolution. The time resolution should be about 0.5 ns for a 10-bit DPWM in a 2 MHz switching converter, consequently a 2.048 GHz external clock signal is needed. However, a high frequency clock is quite undesirable to meet power and area constraints. Figure 4 shows the 10-bit hybrid DPWM module in the proposed 2 MHz digitally controlled DC–DC converter. By choosing a different combination of two different time intervals given by two DLLs, the time resolution can be enhanced extensively[6]. As shown in Fig. 4, Clock1 is used for the system clock and its frequency is 32 MHz, feeding from the off-chip crystal oscillator, and Clock2 is divided from Clock1 to 2 MHz as the switching control clock for the converter. Duty[9 : 0] is the 10-bit duty cycle control word and Duty[9 : 6] is used for 4-bit counter control, which is synchronized at 32 MHz in order to divide the switching interval 0.5 μs into 31.25 ns. The two delay lock loops (DLL), DLL1 and DLL2, are locked to the 32 MHz clock signal. The lower 6-bit of Duty[9 : 0] is used to select a correct delay path for the 2 stage delay lines, where the delay cells are the replication of DLL1 and DLL2, respectively. There are 11 delay cells in DLL1 and 12 delay cells in DLL2. So the minimum time resolution by choosing the proper path is $31.25(1/11-1/12) = 0.237$ ns, which is much smaller than the time resolution of each single DLL. Another 20 delay cells replicated from DLL1 and 11 delay cells replicated from DLL2 are used to cover the modulation range.

2.1.3. Digital compensator

Figure 5 shows the functional block of the digitally controlled voltage-mode control loop in PWM mode. For voltage mode buck converters, the loop response has a pair of poles, p_{r1} and p_{r2}, at the resonance frequency of the LC filter and a higher left half plane zero z_c caused by R_C and C. Thus the feedback loop will be more difficult to compensate since the phase margin should be guaranteed by extra phase shifting circuits.

There are two fixed poles in the digital PID compensator: p_1 is located at $z = 0$ and p_2 is located at $z = 1$. Another two zeros, z_1 and z_2, are added in digital compensator to compensate the complex poles at resonance frequency. The transfer function of digital compensator $C(z)$ is given by

$$C(z) = A\frac{z^{-2} + bz^{-1} + a}{z^{-2} - z^{-1}}, \tag{4}$$

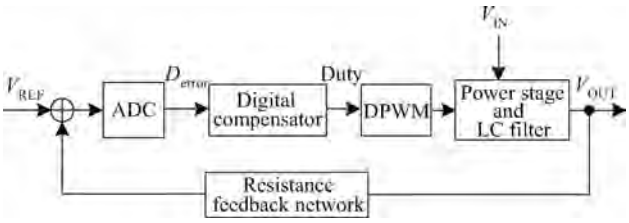

Fig. 5. Functional block of the digitally controlled buck converter.

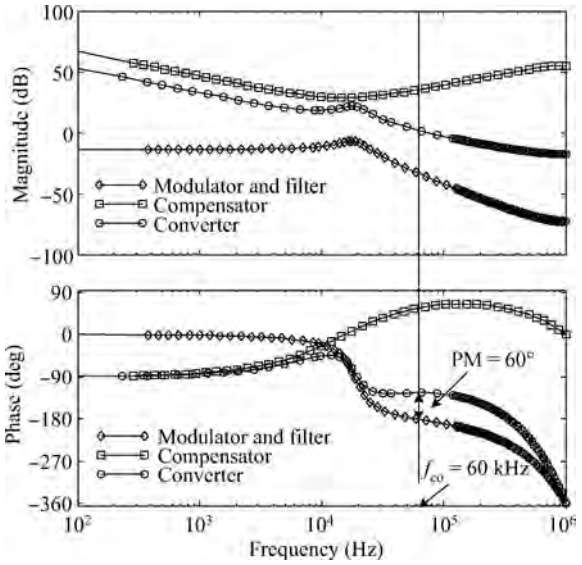

Fig. 6. Bode plot of the power stage of the buck converter.

where a, b are two programmable parameters to determine the two zeros' location and A defines the loop gain at DC. z_1 and z_2 are placed lower than p_{r1} and p_{r2} to guarantee pole zero cancellations with uncertain external components value derivation. The frequency responses of the compensator and the system control loop after compensation are shown in Fig. 6. As can be seen, the bandwidth of the control loop is 60 kHz and the loop gain is 46.6 dB at DC. The phase margin is designed to be about 60°.

The digital compensator is implemented by an IIR filter. A trade-off is made between precision and area in compensator implementation. The key parameter is the bit width of the compensator from architecture to circuit. Step response simulations are performed for an ideal infinite-precision model and a fixed-point structure. Then, the simulation results are compared to determine whether to decrease bit width or not after several iterations.

2.2. Automatic mode switching and PSM control

The mode transition point is set to be the boundary between CCM and DCM of the converter in order to simplify the design. Thus, the proposed digitally controlled buck converter operates in 2 MHz PWM mode in CCM and the converter transits into the PSM mode at a lower load. The detailed system control flowchart for mode transition is shown in Fig. 7(a). The converter enters the PWM mode after soft-start and then transition conditions determine whether mode transition occurs or not. The mode transition condition from PWM to PSM is that zero

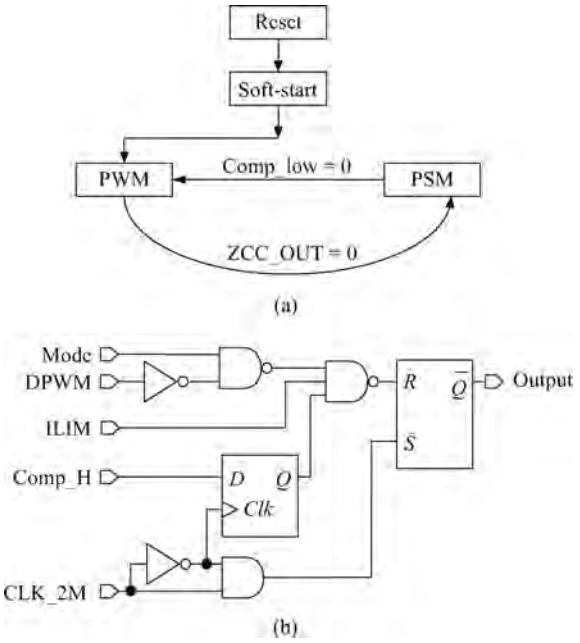

Fig. 7. Flowchart and schematic of mode transition. (a) System control flowchart for mode transition. (b) Simplified schematic of PSM & Mode.

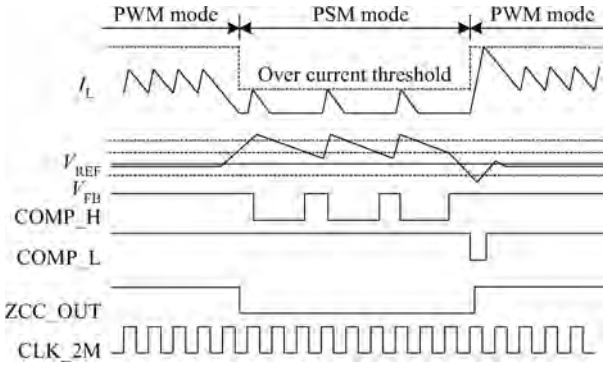

Fig. 8. Sketched waveform of mode transition.

current comparator, ZCC, outputs 0, which denotes DCM operation; but the mode transition condition from PSM to PWM is COMP_L = 0, which denotes that the output voltage is lower than reference voltage, in other words, the load current exceeds the maximum capability of the PSM mode converter. A different transition condition provides hysteresis characteristics for automatic mode switching. As a result, oscillation between PWM and PSM is eliminated, which would otherwise happen when the load current is close to the mode transition point. The converter will stay in the PWM mode when soft-started since the output voltage is lower than V_{REF}. Mode is the output of Mode Switching, where Mode = 1 means PWM operation and Mode = 0 means PSM.

The block PSM&Mode is designed to generate power device control signal VG at both PWM and PSM mode. Figure 7(b) shows a simplified schematic of PSM&Mode. With the help of an inverter and AND gate, the 2 MHz clock signal CLK_2M with a 50% duty cycle is changed into a pulse with same frequency but with a much shorter duty cycle. The RS

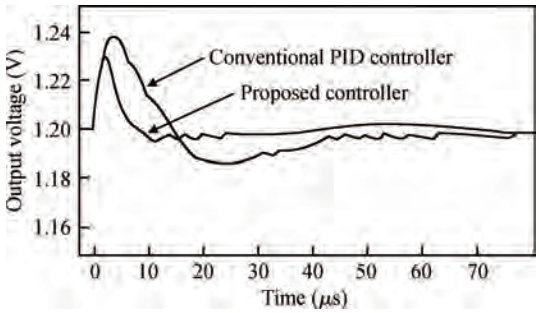

Fig. 9. Dynamic response to load step-down.

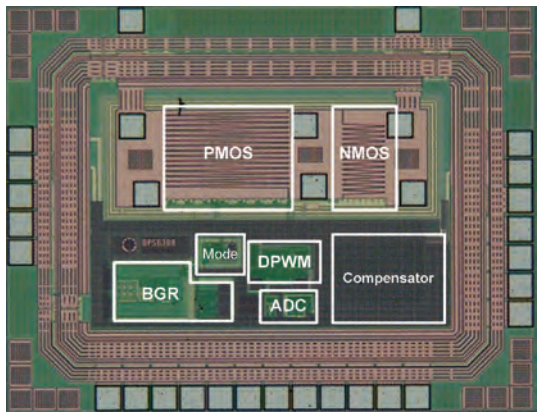

Fig. 10. Micrograph of the digitally controlled converter.

trigger is triggered at the rising edge of CLK_2M. Then, the RS trigger is reset when DPWM turns to zero at PWM mode. The switching cycle will be skipped at both PWM and PSM modes unless Comp_H = 1 at the falling edge of CLK_2M. The pulse width control signal DPWM is shielded, so the converter operates at PSM mode at this time. ILIM is the output of the over-current comparator. The RS trigger is reset when ILIM jumps to zero at PWM mode when the current in MP exceeds the predefined over-current threshold. The current limit value is decreased at PSM mode. So the RS trigger is set by clock signal CLK_2M and reset by ILIM at PSM mode when COMP_H = 1, thereby realizing peak current conduction mode PSM operation. V_{OUT} increases until COMP_H = 0, cycle skipping occurs and V_{OUT} decreases until COMP_H = 1 again. As a result, PSM mode control of the PSM control signals act on the power devices to make them operate in the normal on-off state. The sketched waveforms of mode transition are shown in Fig. 8 to demonstrate the auto mode switching strategy. Hysteresis characteristics are designed for COMP_H to avoid noise interference, as shown in Fig. 2.

The controller will skip several cycles and operate nonlinearly in order to improve its dynamic characteristics by skipping pulses instead of reducing the duty-cycle linearly, especially during load current step-down. When the output voltage is high enough to trigger COMP_H to 0, switching cycles are skipped and the power device is kept off until output voltage falls back to trigger COMP_H to 1. Dynamic response is improved compared to a conventional PID controller, as shown in Fig. 9.

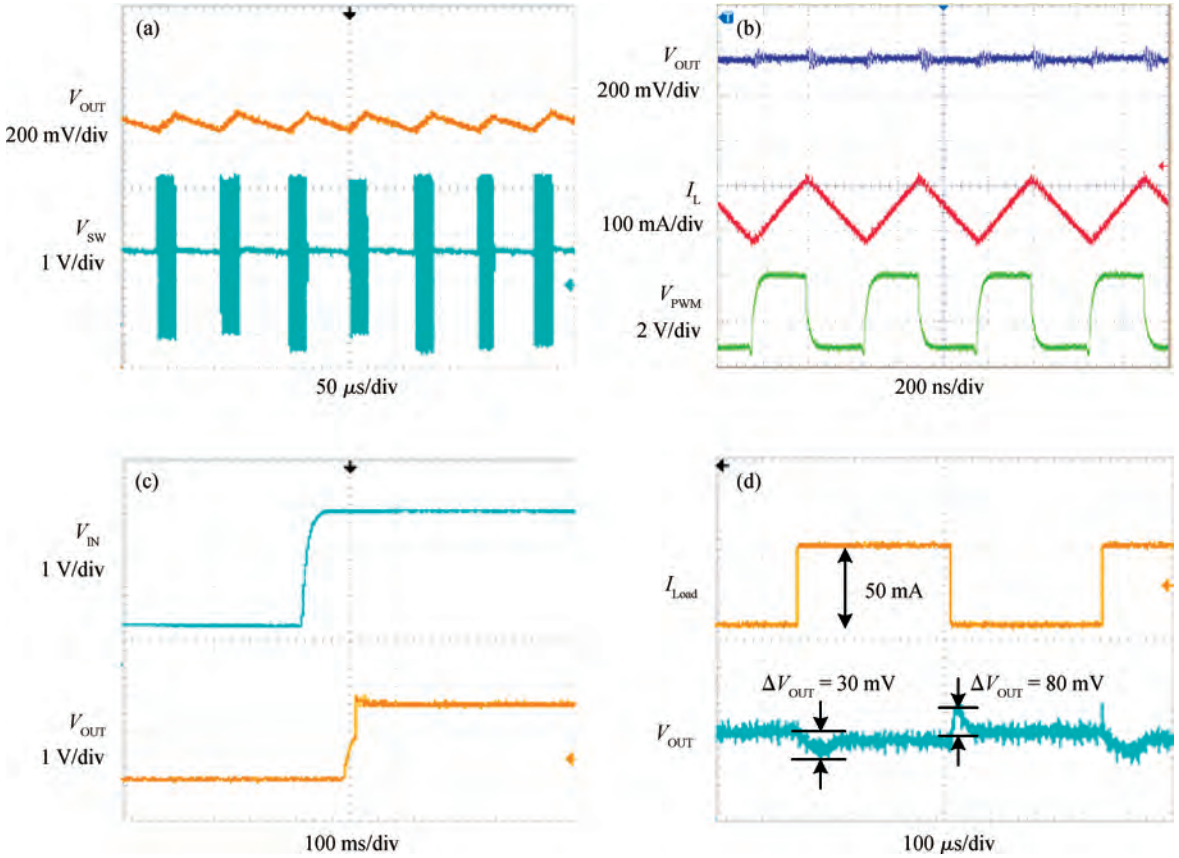

Fig. 11. Measured waveforms. (a) V_{OUT} and V_{SW} waveforms in PSM mode. (b) V_{out}, I_L and V_{PWM} waveforms at PWM mode. (c) V_{in} and V_{out} waveforms at soft-start. (d) Load step response waveforms.

3. Experimental results

The digitally controlled PWM/PSM dual mode buck converter is fabricated in a 0.13 μm CMOS technology with 1 poly and 8 metal layers. The chip micrograph is shown in Fig. 10 and the die area is 1.21 mm^2, including pads and ESD protection circuits. The digital compensator is realized following digital circuit design flow and the other blocks are custom designed.

Figure 11(a) shows waveforms in PSM mode when V_{IN} = 3.3 V, V_{OUT} = 1.2 V and I_{Load} = 20 mA. The output voltage ripple is about 100 mV, which is a little bigger but does not affect load because of the low load operation speed. Figure 11(b) shows measured waveforms in PWM mode when I_{LOAD} = 300 mA. It can be seen the converter is steady in the 2 MHz PWM mode and the output voltage ripple is about 80 mV, including high frequency spikes. The waveforms in Fig. 11(c) give the soft-start waveform when V_{IN} rises from 0 to 3.3 V, where V_{OUT} can start up smoothly from zero to the designed value. The load step response waveform is given in Fig. 11(d). The load current step is 50 mA. The undershoot and overshoot are about 30 mV and 80 mV, respectively, which are within 1% of the final voltage value. As shown in Fig. 12, the maximum efficiency is high at 90% at about a 200 mA load current and efficiency can be kept at 67% at 20 mA. Finally, Table 1 shows the performance summary of this work. Compared to Ref. [8], the light load conversion efficiency is lower, because the quiescent current is higher due to more accurate DPWM resolution and the saturation region operation of ADC oscillators in this work. Light load efficiency can be improved in further work by decreasing the quiescent current and turning off unused blocks completely in PSM mode, such as the DPWM and the ADC. So the control mode will be similar to traditional analog converters in PSM mode. As a result, high efficiency comparable with its analog rivals will be obtained.

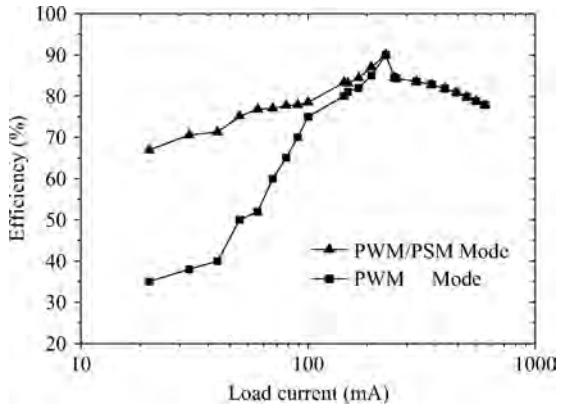

Fig. 12. Measured conversion efficiency.

4. Conclusion

Digitally controlled power converters have many inherent advantages, such as , such as being programmable for different applications, robustness with noise and process variation, and

Table 1. Performance summary.

Parameter	Ref. [8]	Ref. [9]	This work
Technology	0.25 μm CMOS	3.3 V CMOS	0.13 μm CMOS
External LC filter	$L = 10$ μH, $C = 47$ μF	$L = 10$ μH, $C = 10$ μF	$L = 3.3$ μH, $C = 22$ μF
Power device	Integrated	—	Integrated
Input voltage (V)	5.5–2.8	3	3.3
Output voltage (V)	1.0–1.8	1.25	Set by resistors, $V_{\rm REF} = 0.6$ V
External clock frequency (MHz)	—	—	32
Switching frequency (MHz)	0.5–1.5	1	2
DPWM resolution	10-bit (5-bit hardware and 5-bit digital dither), 32 ns @ 1 MHz PWM	10-bit	10-bit, 0.48 ns @ 2 MHz PWM
ADC sample frequency (MHz)	0.5	—	2 (Synchronized with switching frequency)
ADC resolution	LSB = 16 mV, quantization window = 80 mV	LSB = 15 mV	LSB = 15 mV, 5-bit
Load range (mA)	0–400	800	0–600
Quiescent-current (μA)	4	—	400
Efficiency (%)	92 @ $I_{\rm LOAD} = 189$ mA 80 @ $I_{\rm LOAD} = 20$ mA	90 @ $I_{\rm LOAD} = 300$ mA	90 @ $I_{\rm LOAD} = 200$ mA 67 @ $I_{\rm LOAD} = 20$ mA
Chip area (mm^2)	2	0.16	1.21

the convenience of implementing advanced control schemes. Meanwhile, the circuit is easily to realize with the support of EDA tools under different processes. In order to maintain high efficiency over a wide load range, a digitally controlled dual-mode buck converter is designed and implemented in a 0.13 μm 1P8M CMOS process. The measured results show that the converter can work in PSM or PWM, depending on the load current. The efficiency is up to 90% when $I_{\rm Load} =$ 200 mA and light load efficiency is kept at 67% when $I_{\rm Load} =$ 20 mA. The proposed digitally controlled dual mode DC/DC converter is well suited for SoC integration as a power management unit (PMU) because of its high efficiency and good process compatibility.

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