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Design and Comparison of Array and Tree Multiplier Using Different Logic Styles

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Abstract*—The main objective of this project work is to design and simulate simple, suitable and reliable multipliers for DSP processors. Multipliers are one of the most important arithmetic units in Microprocessors and DSPs and also a major source of power dissipation. Reducing the power dissipation of multipliers is a key to satisfy the overall power budget of various digital circuits and systems. In this project, 8x8 and 16x16 Array and Tree multiplier architecture is designed by using full adders of various logic styles. The fundamental units to design a multiplier are adders. The various types of adders designed in our project are Hybrid full adder logic, DVL logic, 14 transistor logic, TFA adder logic, SPL adder logic. The main objective of our work is to calculate the average power and delay of 8x8 and 16x16 multipliers. The design of full adder for low power is obtained and the low power units are implemented on the proposed multiplier and the results are analyzed for better performance. The designs are done using TANNER S-EDIT tool and are simulated using T-SPICE. The multiplier architectures are designed using the three better above said full adders and the results are compared so that we can obtain a better multiplier design.

***Index Terms*— Multipliers, Hybrid Full Adder Logic, TFA Logic, DVL Logic, SPL Logic, 14 T Logic.**

I. INTRODUCTION

The basic building blocks of arithmetic circuits in digital signal processing systems are adders, registers, and multiplier. Among these components, the multipliers are the most area, time, and power consuming components. Hence, there have been many researches in the past and in present as well to optimize the multiplier architecture. The speed of multiplication operation is increased using several schemes such as Wallace-tree [3] and Dadda [4] multipliers. The array multiplier is the simplest architecture and is most suitable for VLSI implementation because of its high degree of regularity. The multiplier circuit is a core component of most of the present day digital signal processors. Therefore, the demand for multiplier-performance improvement is increasing. Multipliers are a major source of power dissipation. Reducing the power dissipation of multipliers is key to satisfying the overall power budget of various digital circuits and systems. In this paper, power reductions for multipliers are explained and power comparisons of array and Wallace tree Multipliers are obtained for power reduction various adder logics were used. The adders are implemented in multipliers for the excellent reduction of power and the transistor count.[1]

This paper is organized as follows: In section 2 the different adder logics were discussed. In Section 3 deals with the design of multiplier architecture. In section 4 the simulation results of adders and multipliers are discussed. Section 5 the multipliers were compared. Section 6 experimental results and conclusion are discussed from this we can obtain a better multiplier for filter design.[4][5]

II. ADDER LOGICS

Addition is the most common and often used arithmetic operation on microprocessor, digital signal processor, especially digital computers. Also, it serves as a building block for synthesis all other arithmetic operations. Therefore, regarding the efficient implementation of an arithmetic unit, the binary adder structures become a very critical hardware unit. The adder logics we discussed in this paper are as follows.

A. Hybrid Full Adder Logic

Hybrid Full Adder cell, which contains the 26 transistors, utilizes a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding two series PMOS and two series NMOS transistors respectively [3]. Here hybrid Full Adder Cells, which were reported to have better performance than others, are reviewed and analyzed.

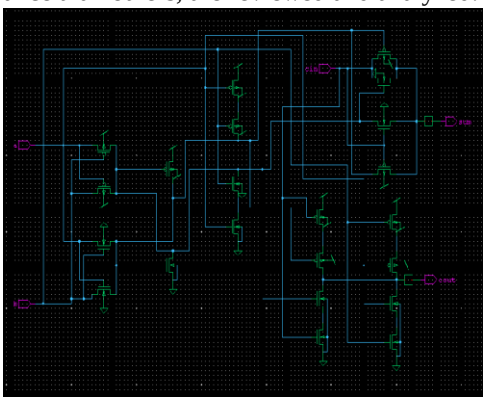

Fig 1. Hybrid Full Adder

The adders considered in this work were designed using traditional implementing methods, i.e. they use only transistors and no input capacitors are used. Hybrid-CMOS design style utilizes various CMOS logic style circuits to build new full adders with desired performance. Lowering the number of transistors can inherently lead to smaller occupied area, higher speed and lower power consumption.[8]

B. DVL ADDER LOGIC

The DVL full adder illustrated in Figure 2, uses 23 transistors for the realization of the adder function. DVL was developed to improve the characteristics of double pass transistor logic which was designed to have the logic level high signal passed to the load through a p-transistor and the logic level low drained from the load through an n-transistor.

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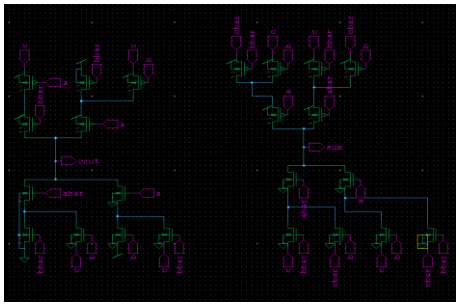

Fig 2 Dual Value Logic(DVL)

C. Transistor Adder Logic

Our new improved 14T[8] adder cell requires only 14 transistors to realize the adder function shown in Fig. 3. It produces the better result in threshold loss, speed and power by sacrificing four extra transistors per adder cell. Even though the transistor count increases by four per adder cell, it reduces the threshold loss problem, which exists in the SERF by inserting the inverter between XOR Gate outputs to form XNOR gate.[7]

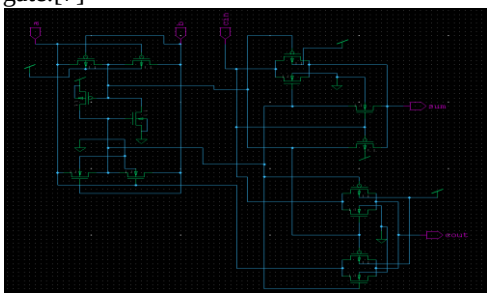

Fig 3 Transistor Full Adder

D. TFA Adder Logic

Transmission function logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a PMOS transistor and an NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic "1" or "0", respectively when they are turned on simultaneously. Thus, there is no voltage drop problem whether the "1" or "0" is passed through it. It contains the 20 transistors.

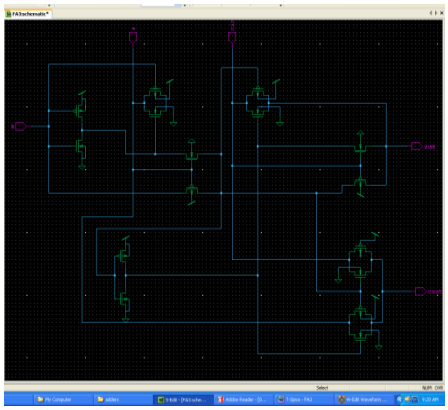

Fig 4 Transmission Function Full Adder

E. SPL Adder Logic

Single-ended pass transistor logic (SPL) and complementary pass transistor logic (CPL) are advocated for low energy arithmetic functions [8][9]. The main reason is that arithmetic functions are based on many XOR gates, and passtransistor logic enables efficient implementations of XOR gates. . CPL and SPL methods (named PTL below) contribute to energy minimization by the small number of pass transistors, which are usually NMOS, and produce very compact and regular designs. Another advantage of PTL is that Vdd-to-GND paths, which may lead to short-circuit energy dissipation, are eliminated. The drawback is the degradation of voltage swing to one VTH away from the supply. Voltage swing restoration buffers are required, increasing transistor count and energy dissipation. On the other hand, we charge the internal nodes to the lower voltage and thus reduce the charge amount and energy dissipation.[5]

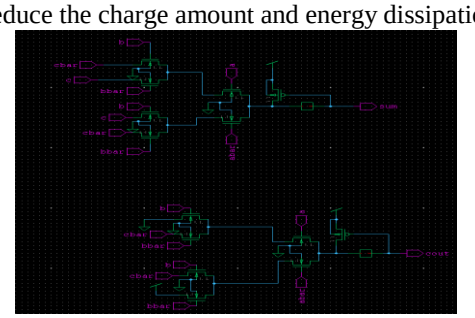

Fig 5 Single Ended Pass Transistor Logic

III. MULTIPLIER DESIGN

The multipliers play a major role in arithmetic operations in digital signal processing (DSP) applications. The present development in processor designs aim at design of low power multiplier. So, the need for low power multipliers has increased. Multiplication represents a fundamental building block in all DSP tasks. Due to the large latency inherent in multiplication, schemes have been devised to minimize the delay. Two methods are common in current implementations: regular arrays and Wallace trees. Previous gate-level analyses have suggested that not only are Wallace trees faster than array schemes, they also consume much less power.

A. ARRAY MULTIPLIER

An Array multiplier [8] is very regular in structure. An n bit Array multiplier has n x n array of AND gates to generate partial products, n x (n-2) full adders and n half adders. Each partial product bit is fed into a full adder which sums the partial product bit with the sum from the previous adder and a carry from the less significant previous adder.The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand.

a) ARRAY MULTIPLIER USING HYBRID FULL ADDER

Braun's multiplier is an n × m bit parallel multiplier and generally known as carry save multiplier and is constructed with m × (n-1) adders and m × n AND gates. The Braun's

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multiplier has a glitching problem which is due to the ripple carry adder in the last stage of the multiplier [8] [9]

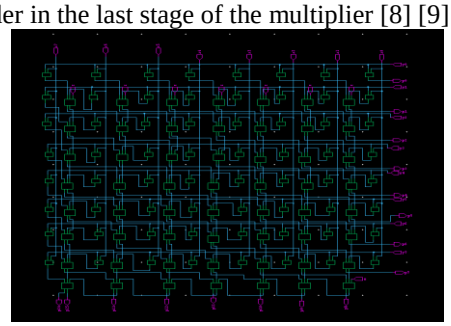

Fig 6 8x8 Array Multiplier Using Hybrid Full Adder

To perform N -bit by N-bit multiplication the N-bit multiplicand A is multiplied by N-bit multiplier B to produce product. The unsigned binary numbers A and B can be expressed as:

$$A = \sum_{i=0}^{n} Ai2^{i} \quad \text{.....(1)}$$

$$B = \sum_{j=0}^{m} Bj\,2^{j} \quad \text{----(2)}$$

The product of A and B is P and it can be written in the following form

$$P = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} A_i B_j 2^{(i+j)} \quad \text{-----(3)}$$

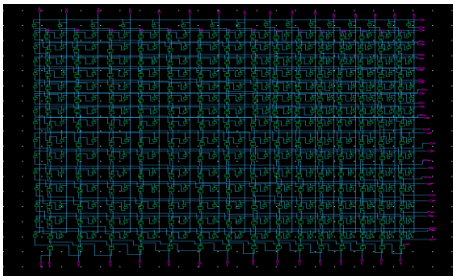

Fig 7 16x16 Array Multiplier Using Hybrid Full Adder

b) ARRAY MULTIPLIER USING 14 T ADDER

In the Carry Save Addition method, the first row can be designed with either Half-Adders or Full-Adders. We have to multiply two bits (one partial product) each from X and Y. If the first row of the partial products is implemented with full adders, then the third input i.e. Cin will be considered ‗0'. The carries of each full adder can be diagonally forwarded to the next row of the adder [8][9].

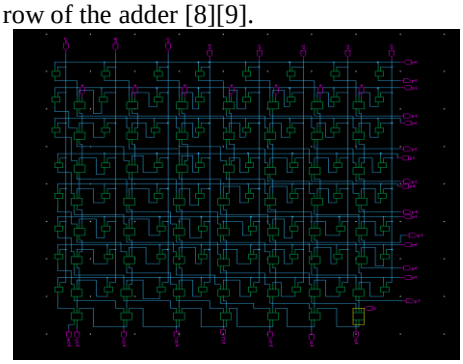

Fig 8. 8x8 Array Multiplier Using 14 Transistor Adder.

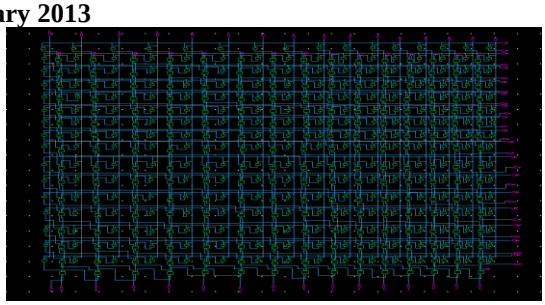

Fig 9. 16x16 Array Multiplier Using 14 Transistor Adder

c) ARRAY MULTIPLIER USING TFA ADDER

A Transmission Function Full Adder (TFA) based on the transmission function theory is shown in Fig 1(d). It has 16 transistors. The power consumption of this structure is 12µw. However, it suffers from insufficient driving power due to the pass transistors.

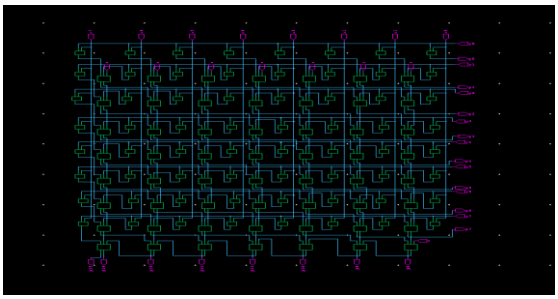

Fig 10. 8x8 Array Multiplier Using Transmission Function Adder

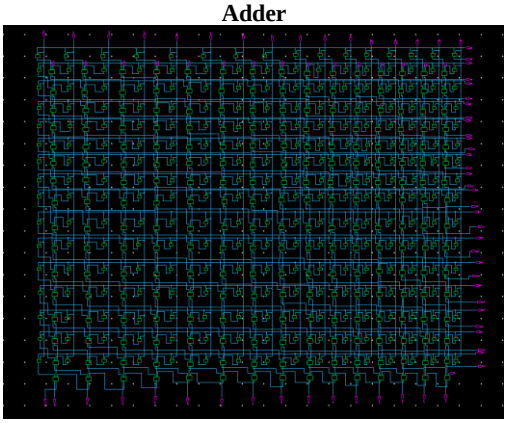

Fig 11 16x16 Array Multiplier Using Transmission Function Adder

Therefore, a similar circuit as that of TFA and 14 T[8]used, but fully exploit the available XOR and XNOR outputs from Module I to allow only a single inverter to be attached at the last stage.

B. TREE MULTIPLIER ARCHITECTURE

For real-time signal processing, a high speed and throughput Multipliers-Accumulator (MAC) is always a key to achieve high performance in thedigital signal processing system. That high speed is achieved through this well-known Wallace tree multiplier. Wallace introduced parallel multiplier architecture to achieve high speed. Wallace Tree

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algorithm can be used to reduce the number of sequential adding stages[2].

a) TREE MULTIPLIER USING HYBRID FULL ADDER

The advantage of high speed becomes an enhanced feature for multipliers having operand of greater than 16 bits. The Wallace tree was being constructed using carry save adder to reduce an Nrow bit product matrix to an equivalent two row matrix that is then fed into carry propagating adderto sum up those rows of bits and to produce the product. The carry save adders are those conventional full adders [11] in which carries arenot connected and three bits of inputs are taken in and two bits are given as output.

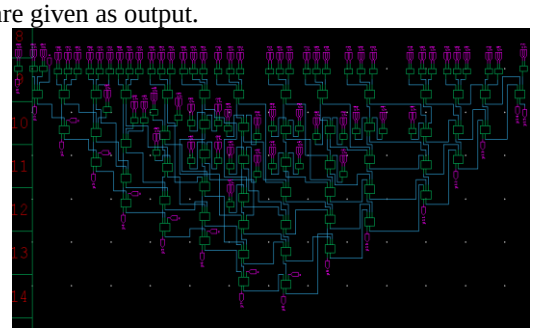

Fig 12 8x8 Wallace Tree Multiplier Using Hybrid Full Adder

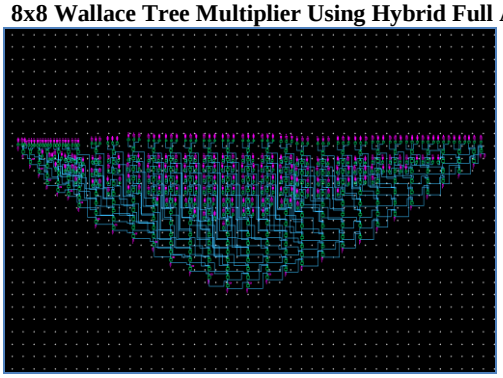

Fig 13 16x16 Wallace Tree Multiplier Using Hybrid Full Adder

b) TREE MULTIPLIER USING 14T ADDER

Generally the Wallace tree construction has many ways to implement. One way among them is considering all bits in a column and producing two bits as output for that column.

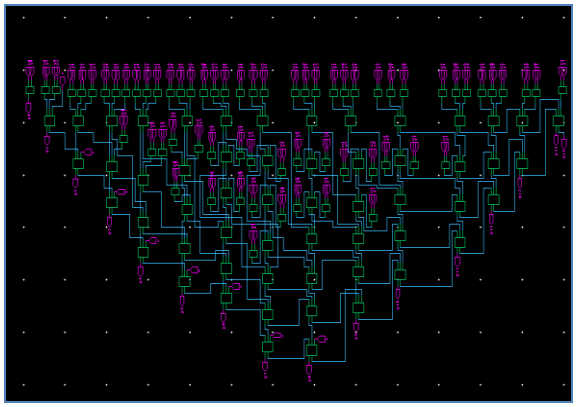

Fig:14 8x8 Wallace Tree Multiplier Using 14t Adder

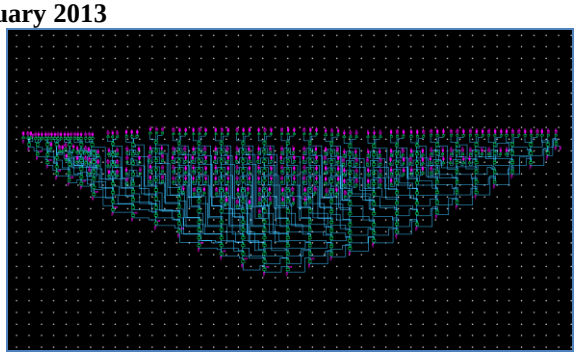

Fig 15 16x16 Wallace Tree Multiplier Using 14t Adder

c) TREE MULTIPLIER USING TFA ADDER

The main disadvantage of Wallace tree multipliers is its irregular structure, making layout difficult and all adder blocks are active regardless of multiplicand size. Delay is log (n). The Wallace tree multiplier has irregular interconnection which in turn occupies more area on the wafer [3], [4], [5] and needs greater cell interconnection wiring. Since an interconnection plays an important role in IC technologies this factor makes Wallace tree inappropriate for certain circuits [6], [7].

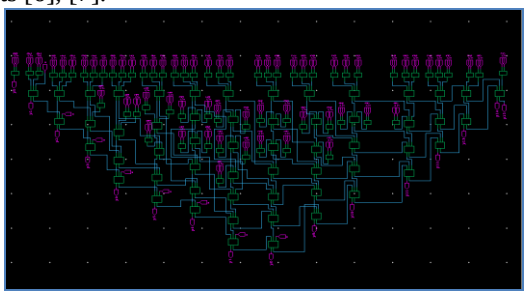

Fig 16 8x8 Wallace Tree Multiplier Using TFA Adder

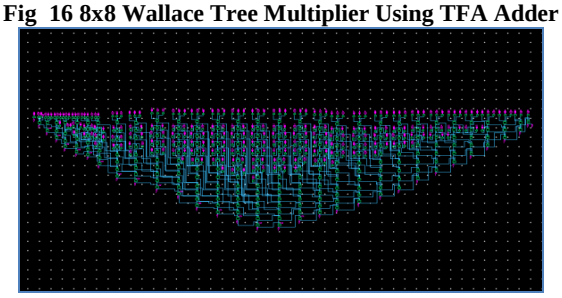

Fig 17. 16X16 Wallace Tree Multiplier Using TFA Adder

IV. POWER COMPARISON

Table I: Power Comparison of Array Multipliers

S.No	Type Of Adder	8x8 array multiplier	16x16 array multiplier
1	Hybrid full adder	4.2170e^-002 watts	1.98e^-001 watts
2	TFA adder	7.18e^-002 watts	4.39e^-002 watts
3	14 transistor	5.434e^-002 watts	3.68e^-002

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	adder		watts

Table II: Power Comparison of Wallace Tree Multipliers

S.no	Type of adder	8x8 wt	16x16 wt
1	Hybrid full adder	4.071e^-002 watts	1.86e^-001 watts
2	TFA adder	5.936e^-002 watts	3.62e^-002 watts
3	14 transistor	4.984e^-002 watts	2.57e^-002 watts

V. RESULTS AND DISCUSSION

The three different full adder logics are hybrid, TFA, 14T. It has been observed that Hybrid full adder logic design style exhibit better characteristics as compared to other design styles. Hybrid full adder logic can be considered to be the best logic design style with respect to all parameters of multiplier architectures.

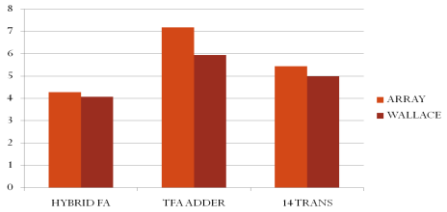

Fig 18. Power Comparison of 8x8 Multiplier Architectures

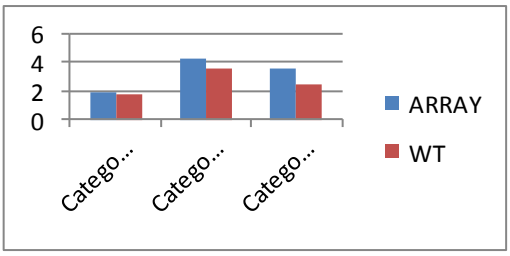

Fig 19. Power Comparison of 16X16 Multiplier Architectures

The designs are done in TANNER SEDIT 12.0 tool and the simulations are done and the power results are obtained in the TANNER TSPICE 12.0.The power comparisons of different units in the existing design and proposed designs are shown in Fig 6.1 to Fig 6.4 and the multiplier power comparison is given in Fig 6.3 and 6.4.

VI. CONCLUSION

In this project the 8x8 and 16x16 array and tree multipliers based on three different logics were designed and the power results were compared. The three different full adder logics are hybrid, TFA, 14T. It has been observed that Hybrid full adder logic design style exhibit better characteristics as compared to other design styles. Hybrid full adder logic can be considered to be the best logic design style with respect to all parameters of multiplier architectures. So, Hybrid logic style can be used where portability and high speed is the prime aim. By using the three different logics the 8x8 and 16x16 array and tree multipliers were designed and the results were shown in table 6.1 to 6.3 Moreover, as our structure is based on regular array structure and the layout will be more suitable for VLSI design. It is worthwhile to mention that our proposed design is more suitable for filter designs.

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